LP3910 Evaluation Kit

National Semiconductor
Application Note 1598
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LP3910 Overview

The LP3910 is a complete power management IC designed for HDD-based Portable media players. It contains a dual source (adapter/USB) linear charger for a single cell Li-Ion / Li-polymer battery, 2 low noise low dropout (LDO) regulators, 2 integrated step down DC-DC buck converters, 1 buck-boost converter with a variable output load voltage range. Other features include, 8 interrupt sources with IRQ request line, power-up/down sequencing and power routing.

The various IC parameters and functions are programmable and configurable through a 400 KHz I²C compatible interface.

Evaluation Kit Overview

The LP3910 Evaluation Kit is based on a modular system, where the actual evaluation board is connected to the PC via a USB – I²C interface board.

The kit supports complete functional evaluation of the LP3910 circuit. The evaluation kit consists of:

- LP3910 evaluation board
- USB Interface board
- USB Interface cable
- CD including the following:
  - Evaluation software for PC
  - LP3910 datasheet
  - Manual document (this document)
  - USB Interface reference material

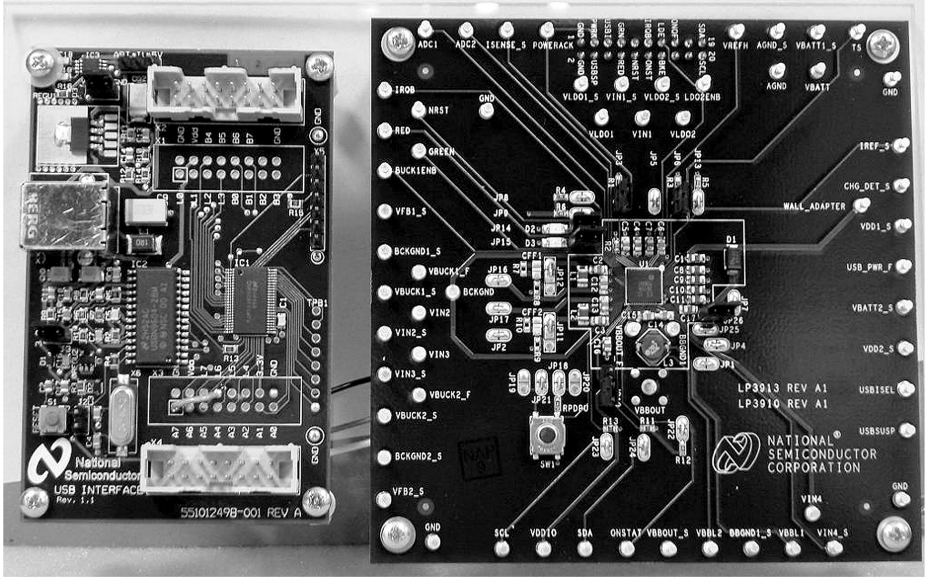

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FIGURE 1. LP3910 Evaluation Kit: USB 1²C Interface (Left); LP3910 Eval Board (Right)

Evaluation Kit Setup

Please use ESD protection to prevent any unwanted damaging ESD events!

The LP3910 Evaluation Board should be connected to the USB interface board as shown in Figure 1.

Connect this setup to the USB port of a PC using the included USB cable. When the USB board is plugged in for the first time, the operating system prompts for “New hardware found” and installs the USB driver. If this does not happen, try unplugging and plugging in the cable again.

LP3910 evaluation software can run directly from the delivered CD by double clicking its icon. However, we recommend that it be copied to the PC’s hard disk and run from there.

The software runs on WinXP and Windows 2000. Please note: Win XP OS administrator rights may be required to run the software.

Cautionary Notes

Always disconnect the USB cable from the board when changing the supply jumper setting (H1 jumper described on page 9). Failure to do so may stop the USB board from responding.

If the USB board shown is not responding or the software hangs up, press the reset button on the USB board, or disconnect the USB cable for 5 seconds. Details of the operation of the USB interface board can be found in the accompanying USB interface manual.

The evaluation software allows control of all registers necessary to control the device. Several slider control interfaces are provided for selecting a range of values for the cases of charge current, and minimum voltage setting. Buttons are provided for switching between two values, to enable or disable certain sections, or to turn on and off certain sections.

Direct Register Programming (described on pg. 5) should only be used for debugging purposes.

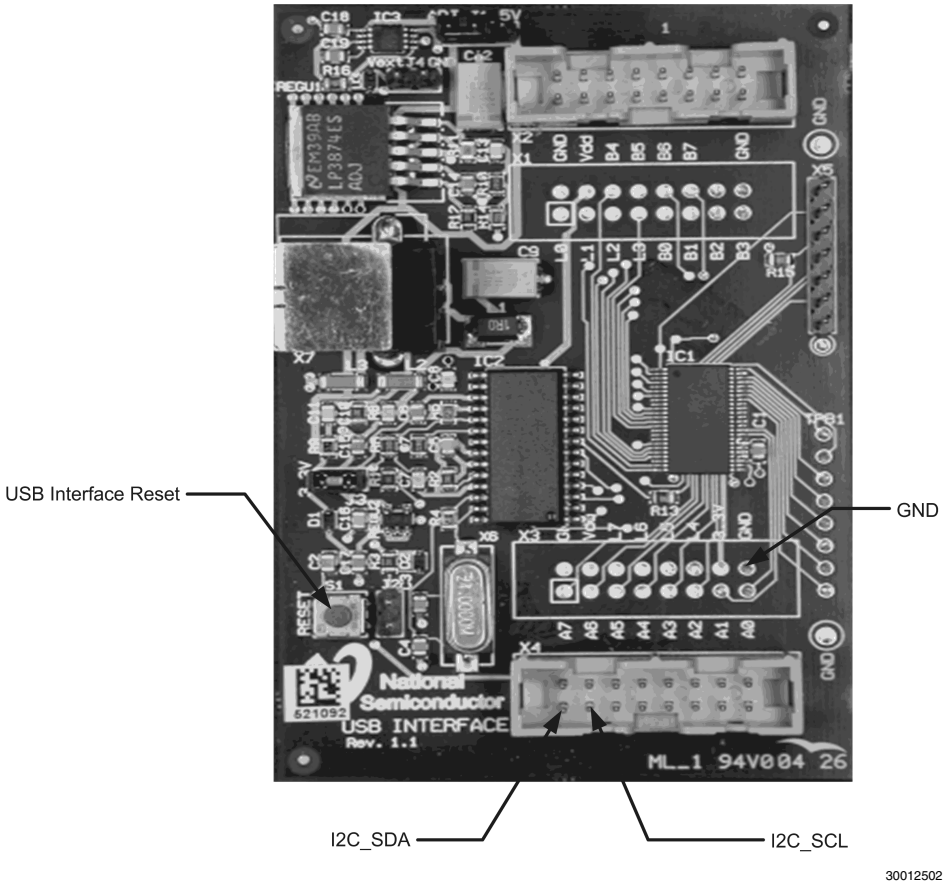

FIGURE 2. USB Interface Board

Getting Started

The LP3910 can be put into active mode of operation via 4 different methods:

1. Battery insertation — Voltage between 2.5 and 6.0 V applied to the VBATT pin of an unpowered evaluation board.
2. Rising / Falling edge detection on ON/OFF pin (Pressing ON/OFF push button). This will be configured for the customers prior to shipping.
3. AC adapter Charger Insertion (AC adapter / power supply (4.5-6V typical) connected to CHG_DET referenced to AGND)
4. USB Insertion (USB power / Power supply (4.4-5.5V) connected to USBPWR pin referenced to AGND).

For a quick start, simply connect a power supply / Battery (3.6V typical) to VBATT pin referenced to AGND. All jumpers should be shorted except for JP19 & JP20 on the LP3910 Evaluation board.

For a quick verification of a clean power up, measure the Vrefh band gap voltage (1.223V typical). For an accurate reading of these voltages, please set the input impedance of the DMM to > 10 GΩ. The set up is now ready to be controlled through the provided GUI (Graphical User Interface) described in the following sections.

For more information on powering up the LP3910 through a charger adapter or USB please refer to the “Powering the LP3910 Board” section in this manual or the LP3910 datasheet provided in the LP3910 Evaluation Kit CD.

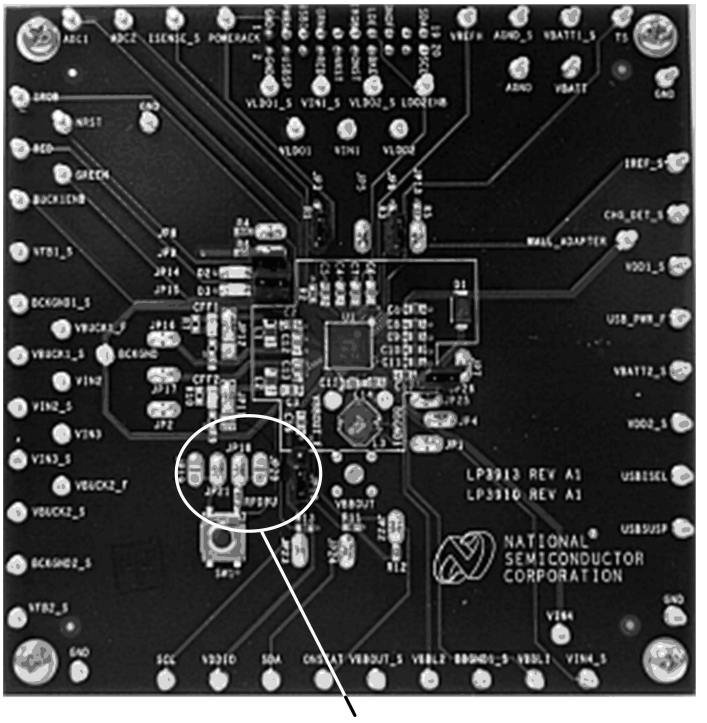

FIGURE 3. Getting Started

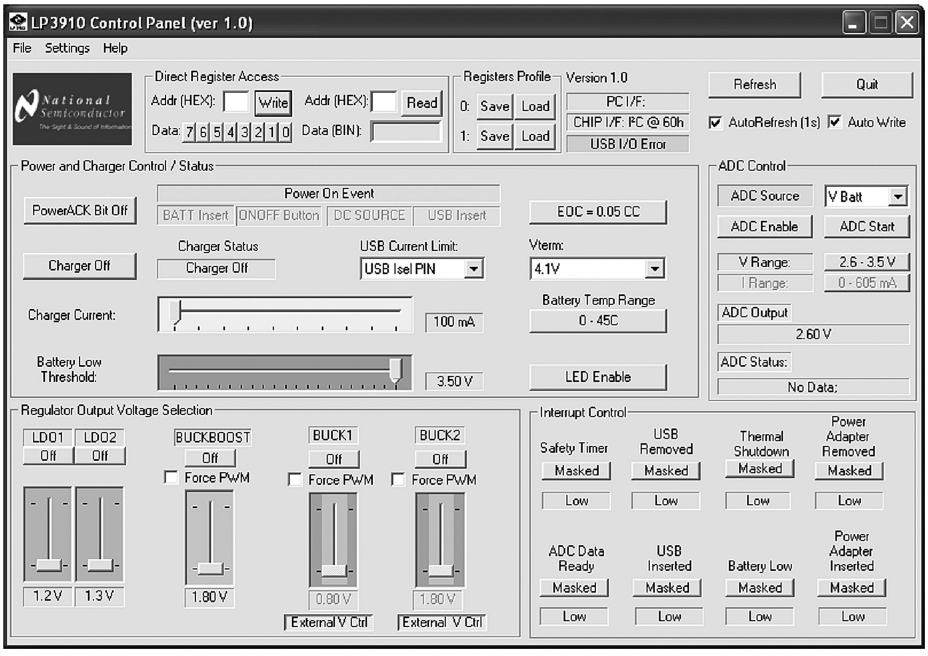

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FIGURE 4. LP3910 Evaluation Software User Interface

Using the Evaluation Software

REGISTER INTERFACE (DIRECT WRITE AND READ)

A register control established through an I²C compatible serial interface allows the user to directly program the registers by writing to, and reading from, the memory map registers. This provides the user with added flexibility in controlling the different functions of the LP3910. However, we caution the user to use this function only for debugging purposes because sending wrong values could damage the part. Sliders and buttons provided below will accomplish the same commands in a more interactive way, and is also less prone to mistakes.

Using the Register Controls

Direct Register Access (left section of Fig. 5) is divided into two parts: Direct Register Write on the left and Direct Register Read on the right. To write to a specific register, simply type the register address in hexadecimal into the box, set the value through the specific bit buttons, and click “Write”. To read a value in binary, type in the register address in hexadecimal into the box on the right and click “Read”.

For example, to turn on the Buck-Boost regulator and set its output voltage to 2.0V can be done by typing in the number 7 into the “Addr (HEX):” box, clicking binary placeholder numbers 5 and 2, and then clicking store. The register should reflect the stored value (00100100) assigned when the user clicks the button “Read.” Please note that the same function could be more easily implemented through the graphical interfaces, and is in the users’ best interest use Direct Register Access only when necessary.

The register profile interface allows the user to save all his/her settings for use at a later time. The GUI is programmed to accommodate saving two sets of profiles.

If the IC changes state and/or if the user assigns a new value to a register, the GUI may not reflect those changes if the AutoRefresh button is not enabled. By hitting the Refresh button, the user will manually renew the GUI so that it reflects the most current state of the IC.

The AutoRefresh check box refreshes the GUI every second to ensure that it mirrors the current state of the chip. The checkbox is on by default so that the user can constantly monitor the status of the IC. Similarly, the AutoWrite check box will enable the signals generated from using the sliders or buttons to be sent to the chip. The check box is on by default, and should be unchecked if the user wishes not to change the settings on the chip.

The Quit button allows the user to exit the program.

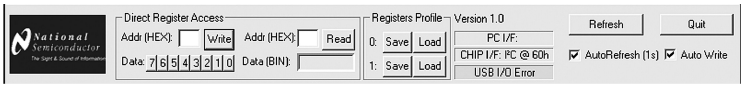

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FIGURE 5. Register Interface

REGULATOR OUTPUT VOLTAGE SELECTION

The output voltages of all the LDO’s, buck-boost, buck converters can be programmed through I²C control registers by simply moving the slider. Buck 1 and LDO 2 can also be hardware enabled or disabled via the Enable pins.

The user can also force the buck-boost and bucks into PWM mode. Clicking the “Force PWM” check box on the GUI forces the respective regulator to stay in PWM mode even in the case of a light load (PFM mode). Forced PWM will be disabled by clicking the “Force PWM” check-box again.

The buck converters have a slider interface to provide an adjustable output voltage. This function becomes grayed out when the user clicks the “External V Ctrl” button underneath the slider interface, which enables the user to use external resistor divider network for setting the Bucks output voltage. Force PWM mode is not recommended when a battery is powering the system.

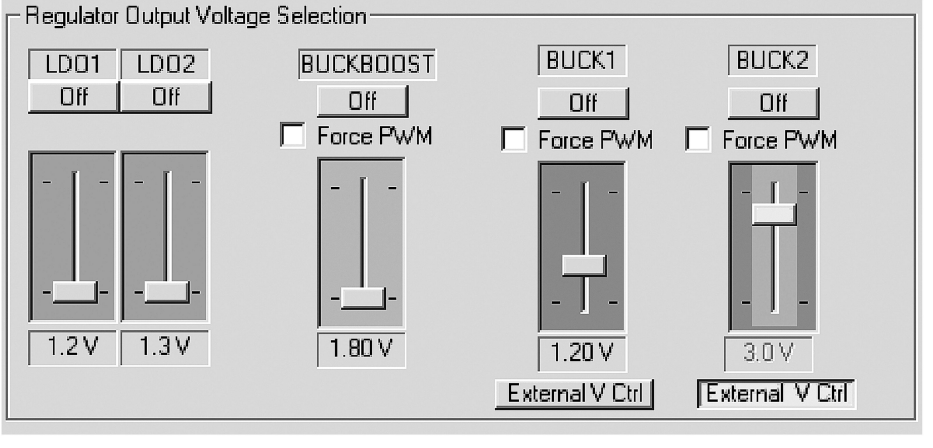

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FIGURE 6. Regulator Output Voltage Selection Interface

BATTERY CHARGER INTERFACE

Power Events

The PowerACK Bit button serves as a Power Acknowledgement ("Power ACK") confirming the power on request initiated by the ONOFF pin. Normally, the system processor sets the PowerACK bit (D4) in the PON register (reg 0x00) or the POWERACK pin within 64ms to register the power on event. If this button is OFF, it disables the power, sends the IC into standby, and waits for a power on event.

The four read only boxes shown in figure 6 under the "Power On Event" banner (Batt Insert, ON/OFF Button, DC SOURCE, USB Insert) indicate the source of the external power on event. If one of the boxes lights up green, it indicates that the LP3910 was powered up by that corresponding power on event. For example, a voltage applied on the VBATT pin will cause the "BATT Insert" box to light up green. Note that this interface only tells the user what caused the chip to power on, and does not necessarily reflect the current status of the battery, ONOFF button, wall adapter, or USB power.

Charger Control and Status

In case the AC adapter charger and the USB charger are both inserted, the USB is disabled from charging the battery via power routing. If the AC Adapter is removed, USB battery charging will take over.

The USB may only charge at three discrete values – 100mA, 500mA, and 800mA. The user may also set the Current Limit to "USB Isel PIN" to control the current limit through hardware.

If the user opts to use the USB ISEL Pin, a logic 0 applied to the pin will limit the current to 100mA and a logic 1 applied to the pin will limit the current to 500mA. The Charger Current slider will prevent the user from selecting a value higher than the current limit.

NOTE: Due to the current limitations of the USB standard, the system will encounter some problems when it is charging the battery in low current mode (i.e. 100mA). Unfortunately this will be too low because it powers the USB interface board as well.

To circumvent this problem, simply power the USB PWR pin on the Evaluation PCB externally with a 5V supply to emulate a normal USB supply.

To prevent the battery from charging, the user can simply press the Charger Off button, which will disengage the chargers.

The Charger Status display reflects the current state of the charger (Charger OFF, Pre-qualification charging, full rate CC or CV charging, Charge Cycle Complete, End-of-Charge/ Topoff, or Safety Timer Expired). Please note that in order to get a real time value of all registers, AutoRefresh mode must be enabled on the LP3910 GUI.

The Charger Current slider limits the amount of current that is provided to charge the battery after the IC needs are met. The value should not exceed a value greater than the power adapter can provide.

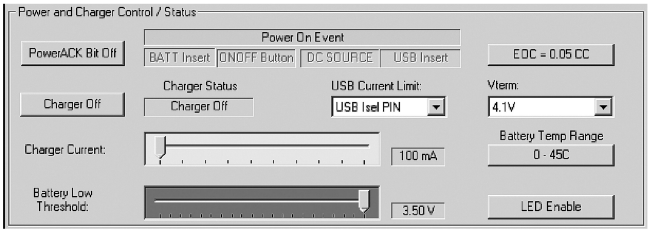

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FIGURE 7. Battery GUI Interface

ADC CONTROL

The ADC control panel allows the user to measure the battery voltage, charger current, ADC1, or ADC2.

The panel should be set to measure the battery voltage by default. To change this setting, click on the dropdown menu next to “ADC Source” and select the corresponding item.

To measure a value, the user must make sure that the “ADC Enable” button is depressed, and then click on “ADC Start.” Subsequent measurements require the ADC Start button to be clicked again.

When measuring the battery voltage, the user may select the range that the ADC will measure. By default, the range of the ADC output will be between 2.6 - 3.5V. The user may select a range of 2.6 - 4.4V by clicking on the button. The battery voltage range that the ADC is currently measuring will be displayed on the button.

Correspondingly, the control panel can also show the battery charge current by measuring the voltage on the Isense pin. The voltage is converted through software to display a charge current in mA if “I batt charge” is selected from the ADC Source box. Irange be selected to measure 0 - 605mA, or 0 - 1100mA.

Force PWM mode is not recommended when a battery is powering the system.

The user may also wish to apply a voltage on the external ADC1 or ADC2 pins. The voltage applied must be between 1.225 and 2.45V to avoid data overflow.

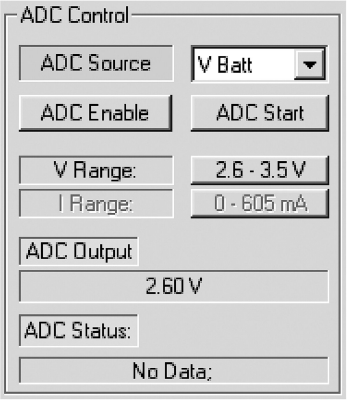

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FIGURE 8. ADC Control Interface

INTERRUPT CONTROL

The LP3910 generates an IRQB interrupt request bit. The pin is an open drain output which transitions from a high to a low when either of the following events occurs.

1. Interrupt 0 – AC adapter has been detected.
2. Interrupt 1 – AC adapter has been removed
3. Interrupt 2 – USB Power has been detected.
4. Interrupt 3 – USB power has been removed.
5. Interrupt 4 – The Battery Low indicator is the most critical and the value required to indicate that the battery is low must be set correctly. If the Li-ion is discharged beyond its minimum limit it can be permanently damaged.
6. 5 – If the IC becomes too hot, a thermal alarm is indicated.
7. Interrupt 6 – The ADC generates an interrupt request upon completion of a data conversion.
8. Interrupt 7 – End of charger indicator; this timeout will occur within 10 hours of inserting a charger.

When an IRQ is made the corresponding IRQ [7-0] bits is set in the register. If the Auto-refresh button is checked, the GUI constantly polls the register-file so that it interrogates the register status for a change of events. If this interrupt is masked, even if the status bit toggles, the interrupt will not be reflected on the IRQB pin.

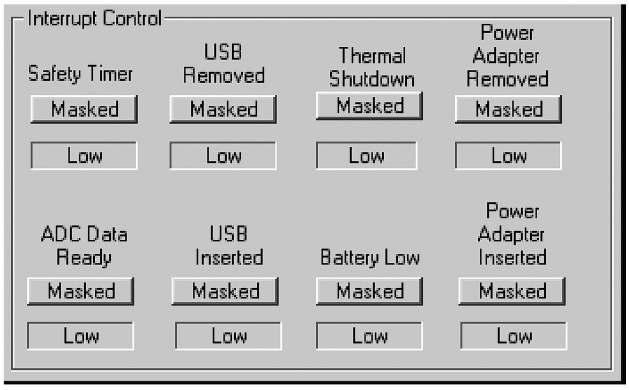

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FIGURE 9. Interrupt Control Interface

Using the Evaluation Hardware

POWERING THE LP3910 BOARD

We recommend that the user power the LP3910 through external power supplies. In case no external power supply is available (as for showroom purposes), the USB board shown in Figure 2 can also be used to power the chip. Please note that this option is NOT recommended, as the USB power output is limited and also encounters a drop across the USB interface card.

External supply

The LP3910 Evaluation board can be powered using a battery as described in previous sections. Simply apply the voltage to the VBATT pin.

A charger/wall-adapter or USB power can also be used to power the system. To power the chip using an AC adapter, simply connect the adapter/power supply (4.5-6V typical) to the pin labeled CHG_DET, which is referenced to AGND/AGND_M. Similarly, connecting an external USB power / power supply (4.5-5.5 typical) to Pin USBPWR referenced to AGND/AGNDM will power the board.

In the case that both the AC charger and USB charger are connected, the AC adapter will have priority and the USB charger will be disengaged. If a battery is connected, the charger will provide power to the system and will also charge the battery based on the charger parameters set by the user. For more information on how the charger operates please refer to the “Battery Charger Interface” section in this manual and the “Power Routing” section of the LP3910 datasheet.

USB Interface Board Supply

In the case that both the AC charger and USB charger are connected, the AC adapter will have priority and the USB charger will be disengaged. If a battery is connected, the charger will provide power to the system and will also charge the battery based on the charger parameters set by the user. For more information on how the charger operates please refer to the “Battery Charger Interface” section in this manual and the “Power Routing” section of the LP3910 datasheet.

NOTE: If there is no battery, VDD from the USB board should NOT be connected to the USB_PWR or WALL_ADAPTER pin. The IC performance is unknown and unsupported without a battery.

If a battery is in place, it is possible for the user to connect the VDD of the USB board to either USB_PWR or WALL_ADAPTER. However, this option is recommended because computers not supporting USB 2.0 specifications will not be able to provide more than 100 mA of current and the USB Interface Card will also draw auxiliary power.

The USB interface card can provide the following voltages :

- 5V from USB Board output -On the USB board, H1 (red circle) needs to be set to 5V.
- 3.8V - Can be selected by software, as shown in Figure 9. H1 jumper needs to be set at ADJ.
- 3.0V (Default) - Can be selected by software. H1 jumper needs to be set at ADJ.

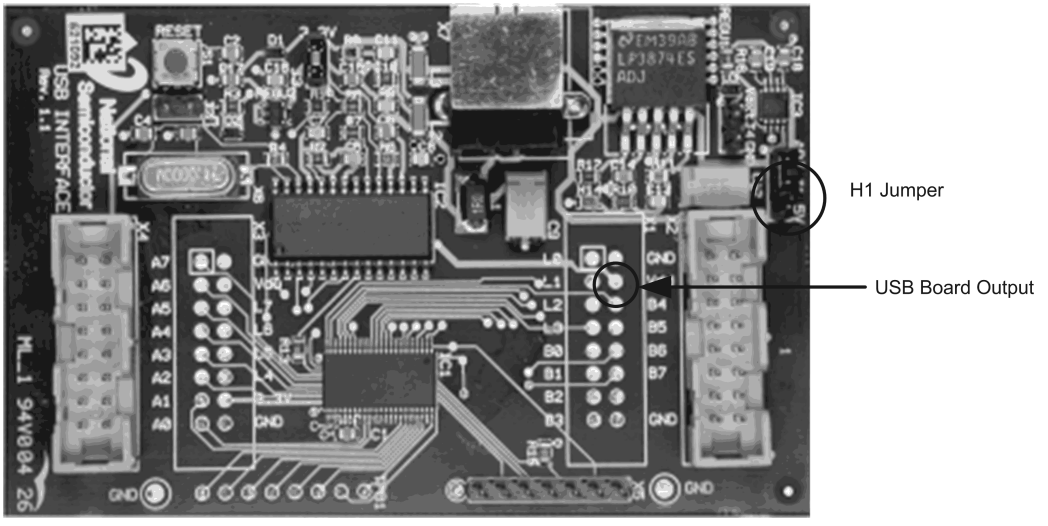


FIGURE 10. USB Interface Settings

FIGURE 11. USB Regulator voltage select

LP3910 HARDWARE BLOCK DESCRIPTION

The evaluation board is fully populated including the LP3910.

The LP3910 evaluation board is designed to allow the user to test each function independently as well as in the system. Jumpers 1-2, 5, 7, 16-17 as described in the Jumper table allow the VDD and GND path of each of the blocks to be separated from the rest of the blocks. To look at each of the blocks, follow the instructions below:

1. Start with all the jumpers connected.
2. Use the provided GUI to disable the desired block.
3. Remove the connecting jumpers based on the jumper table to isolate the power and ground planes of the block under test.
4. Connect a power supply (4.5 - 6V) to the input of the desired block referenced to its corresponding ground.
5. Enable the block and proceed with normal testing.

For accurate voltage measurements, Kelvin connection test points have been provided on the Interface Board with a "*_S" suffix. For example for an accurate measurement of Buck1 output voltage, the voltmeter should be connected between pins labeled VBUCK1_S and BCKGND1_S.

The output voltage of the Low dropout regulators can be accessed at the 'Turrets' (VLDO1 and VLDO2) referenced to AGND. These are marked on the silk screen of the evaluation board.

The output voltage of the two Buck Regulators can be accessed at the 'Turrets' VBUCK1, VBUCK2 referenced to BCKGND1_S, and BCKGND2_S. Similarly, the Buck Boost regulator output can be accessed at BBOUT referenced to BBGND.

The Li-ion battery is connected to turret terminal (+) VBATT referenced to AGND.

The supply voltage for the charger can be connected to turret WALL_ADAPTER referenced to AGND.

Resistive Pull-ups

The two I^2C compatible signals SDA and SCL can be accessed externally via turrets I^2C SCL, and I^2C SDA. Both lines are pulled up via 1.5K resistors R2, R3.

The ONSTAT Open Drain pull-up of 22K resistor is required; this I/O indicates that the status of the debounced state of the on off pin is connected to the hard switch SW1.

The IRQB Open Drain pull up of 22K resistor is required; this I/O is for the active low interrupt request.

The NRST Open drain pull up of 22K resistor is required; this I/O is an active low reset which is issued to the host controller during standby mode.

The POWERACK pin is described in the jumper configuration table.

External Control Resistor Divider

Each of the Buck Switch Regulators has the option to be externally compensated through the external resistive feedback network shown in the figure below. If the user wishes to have the chip internally compensated with factory programmed settings, then a 0Ω resistor should be placed across R14 for Buck 1 and R11 for Buck 2.

Table 1. Jumper Settings

The following table describes the jumpers on the Board:

JUMPER	PURPOSE	NOTE
JP 1, 2, 7	These jumpers connect different ground planes to the analog ground plane. JP1 connects the Buck Boost ground to AGND. JP2 connect the Buck ground to AGND JP 7 connects the analog ground plane to the digital ground plane.	JP1 allows the Buck Boost separated isolated ground plane to be connected to the analog ground point to prevent circulating high return currents flowing around the board. JP2 allows the buck isolated ground plane to be connected to a common ground point to prevent high circulating current flowing around the board. JP7 allows analog ground to be separated from the other ground planes.
JP 3	By enabling the pull-up resistor on the PowerAck pin this allows the IC to be powered ON via Hardware.	This allows the PowerAck pin to be pulled high to VDD. Pressing the ONOFF switch turns the IC on. Removal of the jumper permits SW to enable this pin and power the IC on internally.
JP 4, 5, 16, 17	These jumpers allow different supply voltages to be connected to VDD.	JP4 connects Vin Buck Boost to VDD. .JP5 connects Vin of the LDOs to VDD. JP 16 connects Vin to Vin Buck1. JP 16 connects Vin to Vin Buck2.
JP 6	This jumper connects the TS pin to a 100K resistor.	By having a 121K resistor connected to the thermistor sense pin, this mimics the thermistor inside a Lithium ion battery.
JP 8, 9, 22	These allow pull-ups for IRQB, NRST, and ONSTAT	Pull-ups are necessary for these open drain active low signals. IRQB is for interrupt requests, NRST is the reset during Standby mode, and ONSTAT is the debounced version of the ONOFF pin.
JP 10	This connects VDDIO to the output of Buck 2 or to VDD	VDDIO is connected to VDD for test purposes. If VDDIO is connected to the VBUCK2, the part must be on for I^2C commands to be sent.
JP 11,12	This allows the buck converter feedback loop to be used in two configurations.	Even though compensation and feedback circuit does exist internal to the IC, the user has the flexibility to adjust the Buck output voltage via external Resistor divider and compensation feedback network. More details are given below.
JP 13	This connects the 121kΩ resistor to the IREF pin.	The internal bias generator needs an external 121kΩ resistor because it is stable across temperature. Do NOT remove this jumper.
JP 14, 15	This connects the LEDs to the CHG and STAT pins	These jumpers should only be removed if the user wants to force the LEDs to turn off.
JP 18-21	These jumpers allow different configurations of the ONOFF button	The default setting is with JP18 and JP21 enabled, and JP19-20 disabled. The user should only install only one pair at a time (JP18&21 or JP19&20)

The output voltage of the buck regulator can be set to two different voltages by two, three pin jumpers JP11 and JP12.

JP11 shorted pins 1, 2: R8= 100kΩ, R9= 174kΩ, 0.1uF compensation cap — VOUT=1.37.V

JP11 shorted pins 2, 3; External feedback circuit and compensation circuits are disabled. (Default)

JP12 shorted pins 1, 2; R10= 100kΩ, R11= 174kΩ, 0.1uF compensation cap —VOUT=1.37V

JP12 shorted pins 2, 3; External feedback circuit and compensation circuits are disabled. (Default)

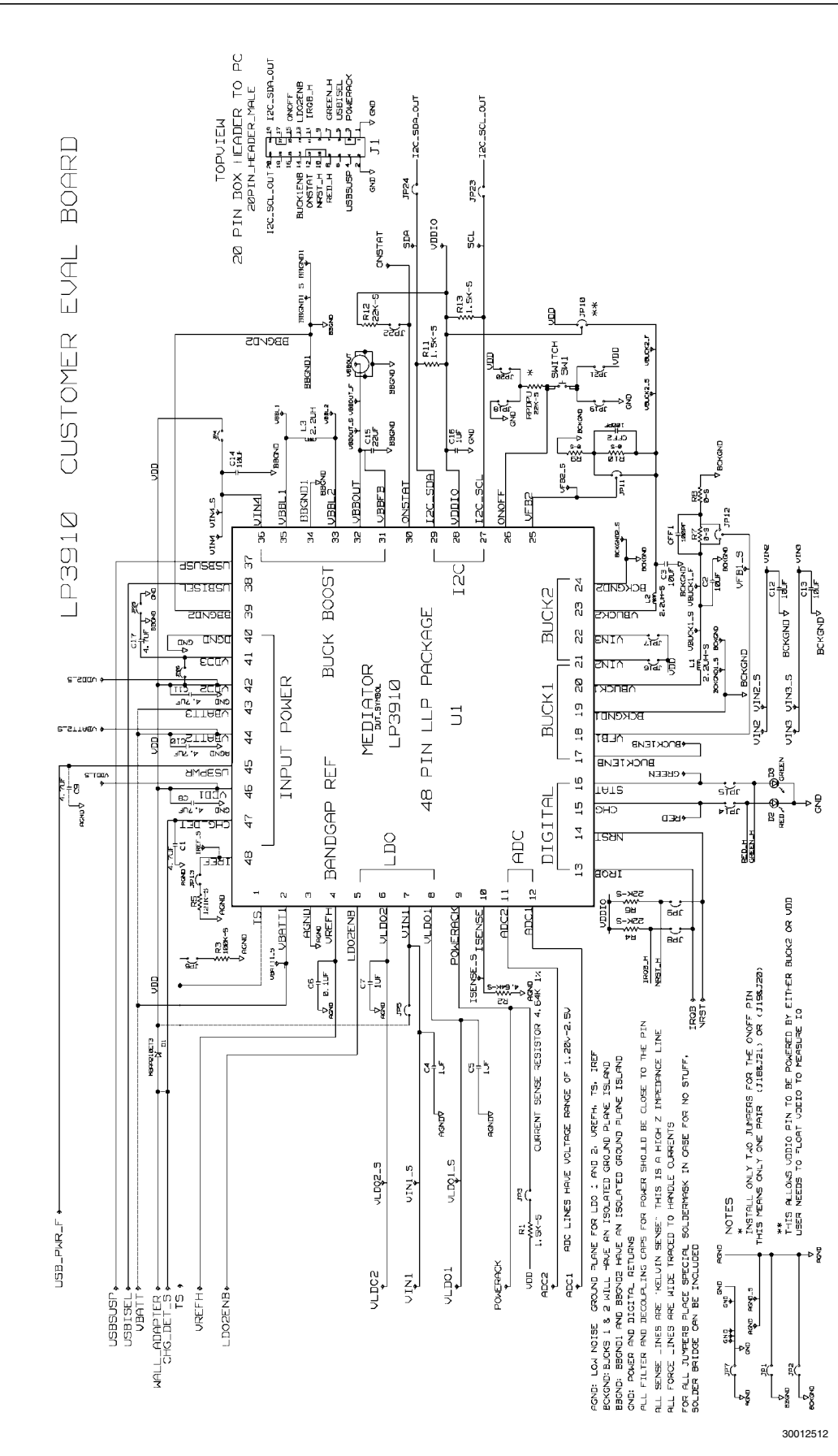


FIGURE 12. LP3910 Evaluation Board Schematic

PCB Layout Considerations

The evaluation board layers from top to bottom are:

1. Top, component side
2. Ground plane
3. Mid signal section
4. Bottom, solder side

For good performance of the circuit, it is essential to place the input and output capacitors very close to the circuit and use wide routing for the traces allowing high currents.

Sensitive components should be placed far from those components with high pulsating current.

Decoupling capacitors should be close to circuit's V_{IN} pins. Digital and analog ground should be routed separately and connected together in a star connection.

It's good practice to minimize high current and switching current paths.

LOW DROP OUT REGULATORS

Place the filter capacitors very close to the input and output pins. Use large trace width for high current carrying traces and the returns to ground.

BUCK REGULATORS

Place the supply bypass, filter capacitor, and inductor close together and keep the traces short. The traces between these components carry relatively high switching current and act as antennas. Following these rules reduces radiated noise.

Arrange the components so that the switching current loops curl in the same direction.

Connect the buck ground and the ground of the capacitors together using generous component-side copper fill as a pseudo-ground plane. Then connect this back to the general board system ground plane at a single point. Place the pseudo-ground plane below these components and then have it tied to system ground of the output capacitor outside of the current loops. This prevents the switched current from injecting noise into the system ground. These components along with the inductor and output should be placed on the same side of the circuit board, and their connections should be made on the same layer.

Route noise sensitive traces such as the voltage feedback path away from the inductor. This is done by routing it on the bottom layer or by adding a grounded copper area between switching node and feedback path. To reduce noisy traces between the power components, keep any digital lines away from this section. Keep the Feedback node as small as possible so that the ground pin and ground traces will shield it from the SW or buck output.

Use wide traces between the power components and for power connections to the DC-DC converter circuit to reduce voltage errors caused by resistive losses.

Buck Boost: Same as above.

For the sense lines, make sure to use a Kelvin contact connection.

ELECTRONIC LOADS

Electronic loads can be used to mimic Li-ion battery. However Electronic loads may create instability within the LP3910 preventing accurate programming currents and voltages. If however, an electronic load is needed for verification, it should be set in “constant resistance mode”.

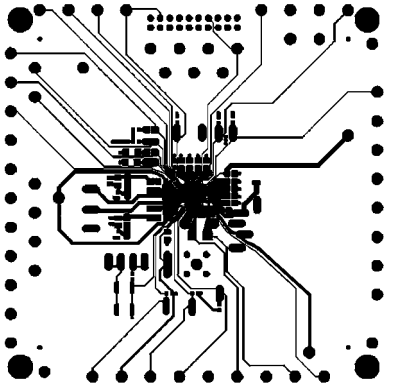
List of Main Components for LP3910 Evaluation Board

Reference Designator	Value, Size, Tolerance	Description	Vendor/Type
C1, C8-11	4.7uF,16V, X7R 0805	ECJ-2FB1C475K	Panasonic
C2,C3,C12,C13,C14	10uF, 16V, X7R 0805	EMK212BJ106KG-T	Taiyo Yuden
C15	22uF, 16V, X7R 0805	Buck Feed forward Capacitor GRM21BR60J226ME39L	TDK
C4,C5,C7,C16	1uF, 16V 0805	GRM21BR71C105KA01L	TDK
C6	0.1uF, 16V, 0805	Vref output capacitors GRM219R71C104KA01D	TDK
CFF1, CFF2	100pF, 0603	C1608C0G1H101J	TDK
R7-R10	TBD, 0805 / 0402	Feedback resistors to buck converter	Manufacturer's choice
R2	4.64K resistor for Isense	MCR03EZPFX464	1Rohm
R1,R11,R13	1.5K, 0402 Digital pull resistors	RC0402FR-071K5L	Yageo America
R3	100K, 0402	TS pin resistor RC0402FR-07100KL	Yageo America
R5	121K 0402	RC0402FR-07121KL	Yageo America
R4,R6,R12,RPDPU	22K 0603	Pullup resistors RC0603JR-0722KL	Yageo America
L3	2.2 uH @ I sat 2A	Buck boost inductor NP04SZB 2R2N	TaiyoYuden
L1,L2	2.2 uH @ I sat 1.2A	Buck filter, and USB filter CBC2518T2R2M	Taiyo-Yuden
D1	2A	Chg_in protection diode MBRA210ET3	On Semiconductor
D3	Green LED	SML-LX1206GC-TR	Lumex
D2	Red LED	SML-LX1206IC-TR	Lumex
SW1	Soft touch switch	KSC321J	Canon
U1	6x6mm 48 LLP package	Power management IC	National Semiconductor

Gerber Files

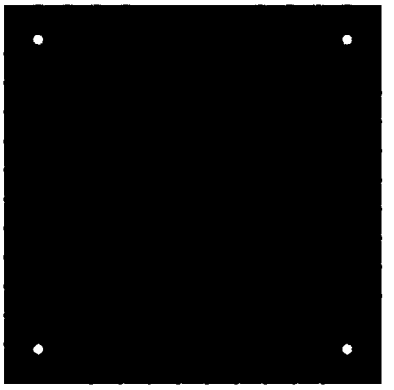
The LP3910 is a four layer board. Below are the Gerber files for the board. The accompanying CD has the Gerber files in Cadence allegro format.

LP3910 CUST EVAL REVA1
TOP
07/06



30012513

LP3910 CUST EVAL REVA1
BOTTOM
07/06



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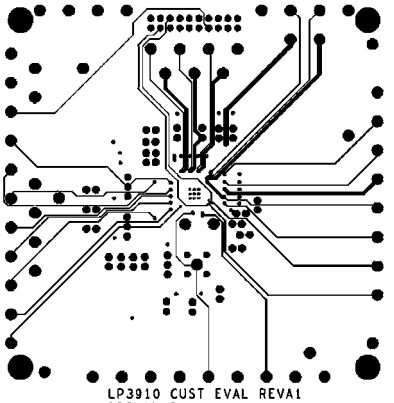
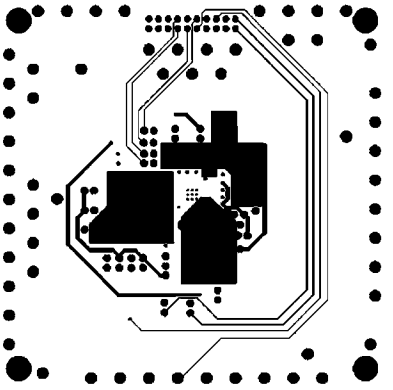


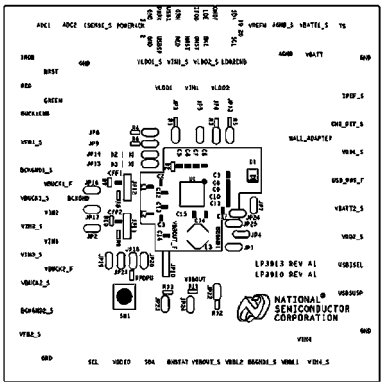
LP3910 CUST EVAL REVA1
SIGNAL_2
07/06

30012515



LP3910 CUST EVAL REVA1
SIGNAL_3
07/06

30012516



LP3910 CUST EVAL REVA1
SILKSCREEN TOP
07/06

30012517

Notes

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