Powering FPGAs Using LM201xx PowerWise® Synchronous Buck Regulators

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The LM201xx PowerWise® synchronous buck regulators are full-featured products, capable of delivering up to 5A of continuous output current. The devices in the family operate from input voltages between 2.95V and 5.5V and convert down to outputs as low as 0.8V. The integrated low RDSon FETs enable a very efficient power supply solution for the multiple rails required to power a FPGA. All of the devices are current-mode controlled providing excellent line regulation and load transient response, and require only two external components for compensation. They feature precision enable, soft-start, tracking, UVLO, OVP, over-temp protection, and PGOOD. The soft-start pin can be used with a capacitor to control start-up inrush current or with an external voltage source to track or sequence multiple supplies. All devices can start into a pre-biased output without discharging it, and they have a diode emulation mode for higher efficiency at light loads. The devices are differentiated by output current capability (3A, 4A, and 5A), frequency (500 kHz, 1 MHz, and 1.5 MHz), and synchronization mode (free-running, sync-in, sync-out, and external resistor adjust). Based on the supply requirements of the FPGA design, an appropriate combination of devices can combine to create a small, efficient, and complete solution.

FPGA Power Supply Requirements

There are several high performance FPGAs currently on the market such as the Xilinx Virtex and Spartan series, and the Altera Cyclone and Stratix series. All of these require multiple power rails including the FPGA core, the I/O, as well as additional rails for powering clocks, PLLs, transceivers, and other circuitry. The core voltage in FPGAs can currently be as low as 0.9V with the current demand for this rail being highly dependent on the utilization of the FPGA. FPGA manufacturers offer power estimation software which assists users in identifying their power needs based on the performance requirements of the design. The I/O rail can also have demanding power needs depending on the number of I/O registers employed in the FPGA design. Most of the latest generation FPGAs have internal POR circuitry which can eliminate the need for power rail sequencing. Select FPGAs specify input inrush currents for particular power-up sequences and others require sequencing rails to avoid start-up or latch-up problems. Start-up time requirements for FPGA rails are varied ranging from 100-200 us at the fastest and 50-100 ms at the slowest.

Example FPGA Power Supply Design

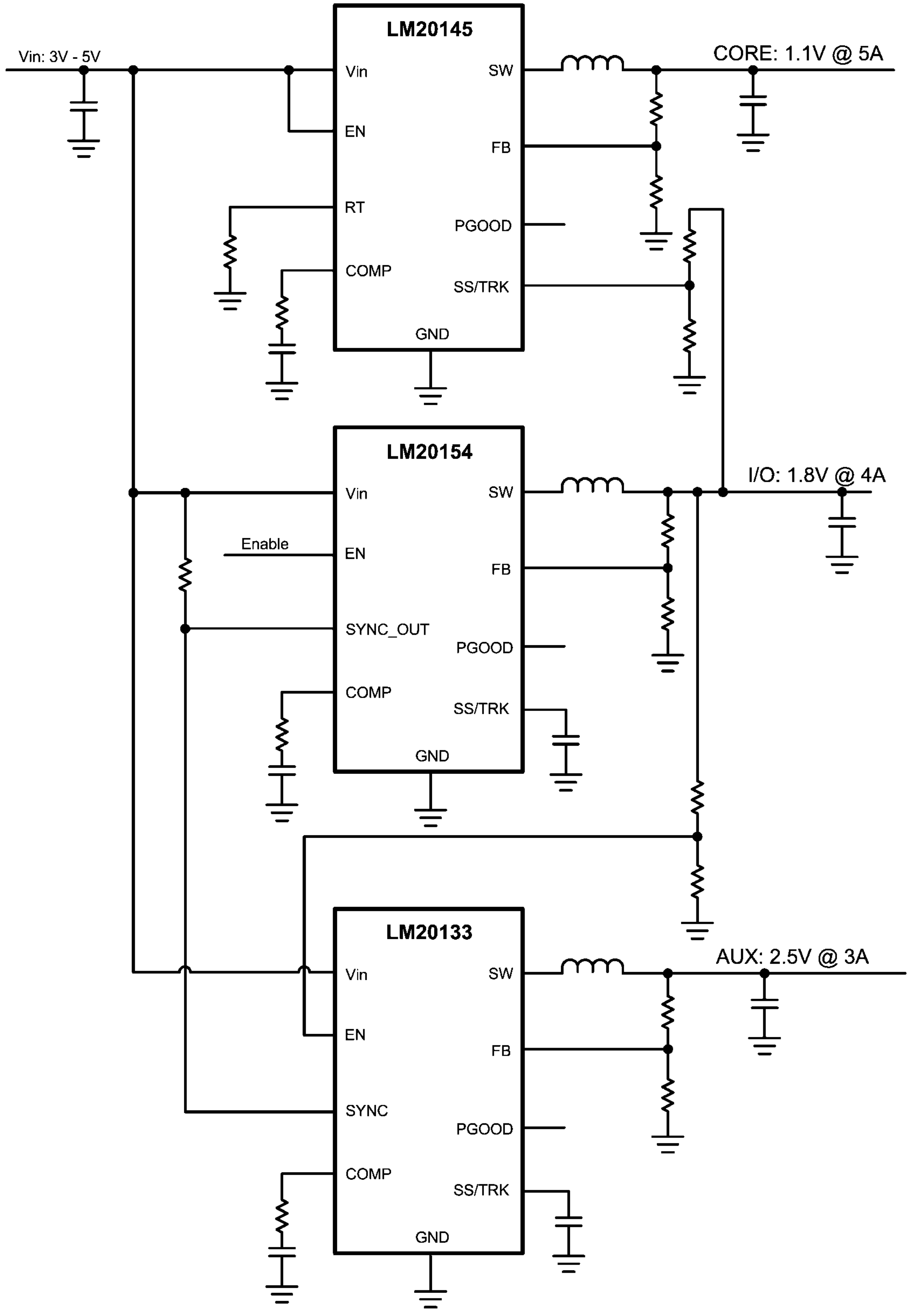

FIGURE 1. Example FPGA Power Design

For the purposes of illustration, an example FPGA power supply design is shown in block diagram form in *Figure 1*. This design features a LM20145 supplying a core voltage of 1.1V capable of delivering up to 5A, a LM20154 supplying an I/O voltage arbitrarily chosen as 1.8V capable of delivering up to 4A, and a LM20133 supplying an auxiliary rail of 2.5V at 3A. Output voltage rails can regulate within 1.5% over temp and are also easily scaled by a resistor divider between the output and the FB pin. All of the devices are packaged in a slim exposed pad TSSOP-16 package enabling a compact power supply design. Additionally, they are pin-to-pin compatible so output current capability can be easily scaled to the FPGA design's power requirements simply by choosing different devices in the family.

Design Features

One of the features highlighted in this design is the many useful frequency synchronization options available. The LM20145 has a resistor adjustable frequency which can be tuned to keep switching noise within a particular spectrum. The LM20133 is a sync-in part which can be synchronized to an external clock signal to achieve the same effect. In this case the LM20133 is synchronized to the sync-out signal coming from the LM20154 which has the added benefit of synchronizing the two parts 180° out of phase. This reduces input ripple current on the input power supply and can thus reduce the input capacitor requirements. *Figure 2* shows an example of input ripple current reduction using out of phase converters.

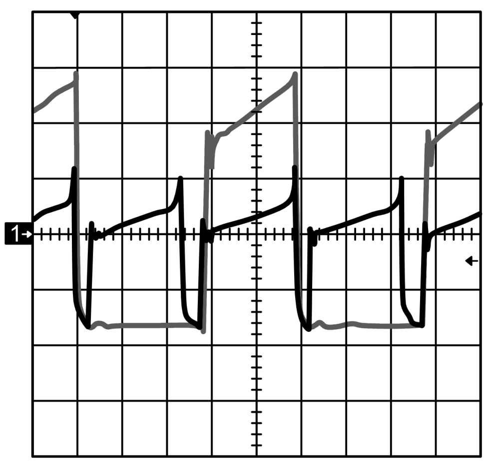

FIGURE 2. Input Capacitor Current Comparison of LM20134/LM20154 (out of phase) and LM20154/LM20154 (in phase) based Buck Regulators

All of the devices have flexible sequencing options as shown in *Figure 3*. In the example design, the LM20145 is "tracked" off of the I/O rail by using the SS pin with a resistive voltage divider. This type of sequencing, known as simultaneous sequencing, allows the voltage difference between the two rails to be minimized which can eliminate parasitic conduction paths between the two rails. The precision EN pin on the LM20133 allows it to be sequentially sequenced by the LM20154 using a voltage divider from the I/O rail. Another method for sequencing involves attaching the PGOOD pin of one part to the EN pin of another. In that case the second part will enable when the output of the first has reached 94% (typ) of its final value.

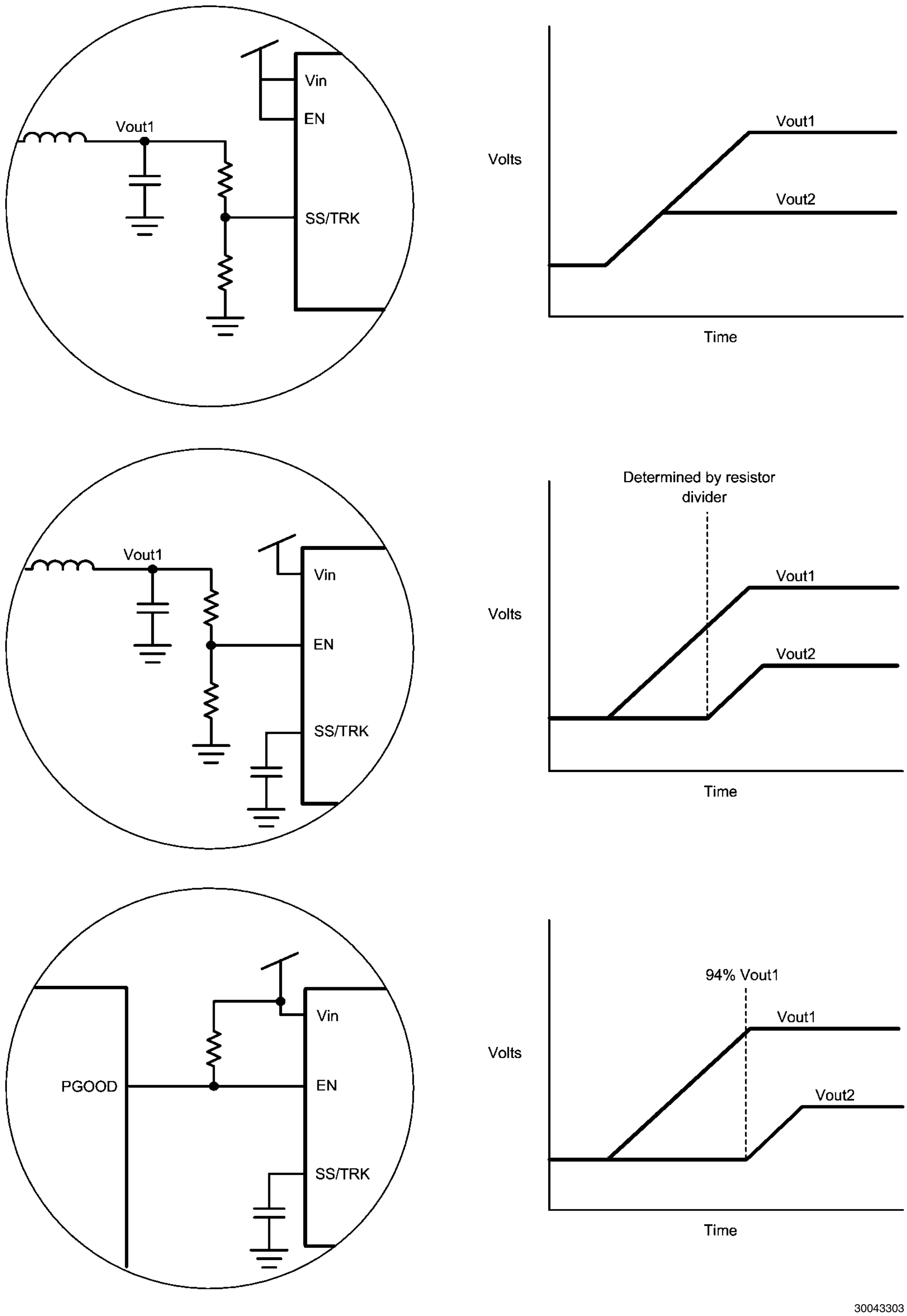

FIGURE 3. Multiple Sequencing Options

Conclusion

The LM201xx family offers a full range of features and options enabling a FPGA designer to fully customize their power solution to meet the system application needs. Full details of the many options and useful features of the entire LM201xx family can be found in the product datasheets at www.national.com/switcher.

Notes

For the most current product information visit us at www.national.com

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