National Semiconductor

450001

Comlinear

High-Performance Analog and Mixed-Signal Products

Operational Amplifiers
Variable Gain Amplifiers
Buffer Amplifiers
Analog Multiplexers
Analog-to-Digital Converters
Serial Digital Drivers

1995 DATABOOK SUPPLEMENT
Quick Reference Index

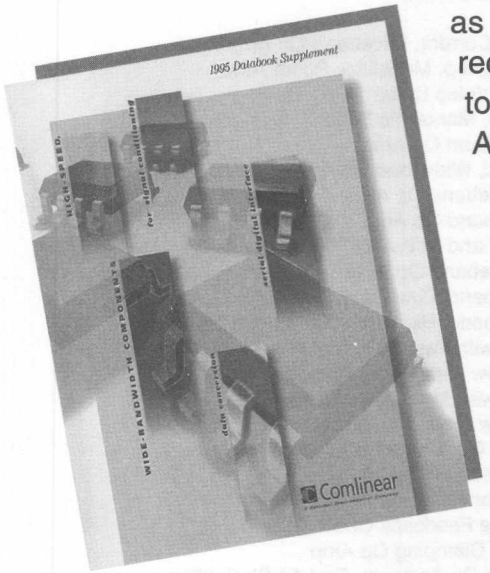
INDIVIDUAL DATASHEETS *supporting the following products are available by contacting your nearest National Semiconductor sales office. In North America, please contact the National Semiconductor Customer Response Group at 1-800-272-9959. For other locations, please refer to the offices listed on the back cover.*

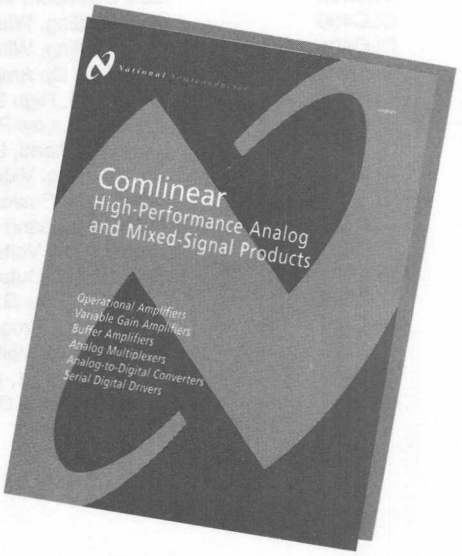
PART NUMBER	DESCRIPTION
CLC103	Fast Settling, High Current, Wideband Op Amp
CLC110	Wideband, Closed-Loop, Monolithic Buffer Amp
CLC114	Quad, Low-Power, Video Buffer
CLC115	Quad, Closed-Loop, Monolithic Buffer
CLC200	Fast Settling, Wideband Op Amp
CLC206	Overdrive Protected, Wideband Op Amp
CLC207	Low Distortion, Wideband Op Amp
CLC220	Fast Settling, Wideband Op Amp
CLC231	Fast Settling, Wideband Buff-Amp™ ($A_v = \pm1$ to ±5)
CLC232	Low Distortion, Wideband Op Amp
CLC400	Fast Settling, Wideband, Low-Gain, Monolithic Op Amp
CLC401	Fast Settling, Wideband, High-Gain, Monolithic Op
CLC402	Low Gain Op Amp with Fast 14-Bit Settling
CLC404	Wideband, High Slew Rate, Monolithic Op Amp
CLC406	Wideband, Low Power, Monolithic Op Amp
CLC409	Very Wideband, Low Distortion, Monolithic Op Amp
CLC410	Fast Settling, Video Op Amp with Disable
CLC414	Quad, Low-Power, Monolithic Op Amp
CLC415	Quad, Wideband Monolithic Op Amp
CLC420	High-Speed, Voltage Feedback Op Amp
CLC501	High-speed, Output Clamping Op Amp
CLC502	Clamping, Low Gain Op Amp with Fast 14-Bit Settling
CLC505	High-speed, Programmable Supply Current, Monolithic Op Amp
CLC520	Amplifier with Voltage Controlled Gain, AGC+Amp
CLC532	High-speed, 2:1, Analog Multiplexer
CLC561	Wideband, Low Distortion, DriveR-amp

We've changed our cover...

but the content is the same.

Together, Comlinear and National Semiconductor continue to bring you high-performance analog products – designed to meet your highest performance expectations. This 1995 Databook Supplement is the same as the one you may have already received ... and you'll want to be sure to get our NEW Databook available April 1996.





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How to use Comlinear's 1995 Databook Supplement

Refer to the Quick Reference Index on the inside front cover of this Supplement to locate a specific product datasheet. This Supplement contains datasheets supporting new products and serves as a supplement to Comlinear's 1993 - 1994 Databook. A complete, new Databook representing Comlinear's entire product line will be available in March 1996. To reserve your copy of Comlinear's 1996 Databook, complete the business reply card found in the back of this Supplement and drop in the mail or in North America contact National Semiconductor's Customer Response Group at 1-800-272-9959. Additional National Semiconductor sales office locations can be found on the back cover of this supplement.

Product Evaluation Tools

Samples, evaluation boards and product literature is available from your nearest National Semiconductor sales office. Check Section 14 of this Supplement for the sale office nearest you or refer to the back cover of this Supplement.

Technical Support

Comlinear and National Semiconductor are dedicated to providing innovative solutions to your high-speed signal processing challenges. To support this effort, Comlinear and National Semiconductor maintain a staff of research and development level applications engineers to provide you both technical and design assistance. Their experience, laboratory and computer simulation resources uniquely qualify them to assist you.

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In March 1995, Comlinear Corporation received ISO 9001 certification through the Defense Electronics Supply Center (DESC) and NSF, an auditor accredited by the Dutch Council for Certification. ISO 9001 is the highest certification level in the ISO 9000 series of quality-assurance standards. Commercial and military customers benefit from Comlinear's ISO 9001 Quality Management System certification for the design/development, manufacture and test of hybrid and monolithic microcircuits.

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1995 Databook Supplement

Comlinear Corporation, located in Fort Collins, Colorado merged with National Semiconductor Corporation in January of 1995. As a separate business unit within National's Analog Mixed Signal Systems Division, Comlinear continues to supply high performance analog signaling processing components.

Comlinear combines quality product performance with applications support to exceed our customers' expectations. On-going new product development at Comlinear centers around signal conditioning, signal processing and data converter products. Signal conditioning products include high-speed hybrid and monolithic operational amplifiers, buffers and clamping amplifiers. Products in the data converter line are track/hold amplifiers and analog-to-digital converters. Our newest product line for signal processing includes serial digital cable drivers.

Through worldwide sales, Comlinear products are designed into commercial, industrial and military applications. Some of the application areas include: communications, imaging, video and instrumentation.

Comlinear

A National Semiconductor Company

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The products in this databook are covered under one or more of the following patents; 4,358,739; 4,502,020; 4,628,279; 4,639,685; 4,713,628; 4,757,275; 4,766,367; 4,780,689; 5,049,653 (other patents pending).

November 1995

Product Selection Guide
Contents

PRODUCT SELECTION GUIDE

Operational Amplifiers (typical specifications, +25°C)

Part Number	Key Features	–3dB Bandwidth (MHz)			Optimal Gain Range ($A_v = V_o/V_i$)	Full Power BW (MHz @ V_{pp}, R_L)	Settling Time (nsec, %)	Output (V,mA)	Slew Rate (V/μsec)	Input Offset Drift (mV, μV/°C)	Test Conditions	Versions					
		$\|A_v\| = 4$	$\|A_v\| = 20$	$\|A_v\| = 40$								J	I	K	M	8	L
CLC103 Hybrid	High Output Current	170	150	130	± 1 to 40	80 @ 20, 100	10, 0.4	± 11, 200	6000	10, 50	$R_L = 100\Omega$ $V_{cc} = \pm 15V$		√	√	√		
CLC203 Hybrid	High Output Current	180	160	130	± 1 to 50	60 @ 20, 100	15, 0.2	± 11, 200	6000	0.5, 5	$R_L = 100\Omega$ $V_{cc} = \pm 15V$		√	√	√		
CLC200 Hybrid	General Purpose	100	95	90	± 1 to 50	25 @ 20, 200	18, 0.1 25, 0.02	± 12, 100	4000	10, 35	$R_L = 200\Omega$ $V_{cc} = \pm 15V$		√	√		√	
CLC201 Hybrid	Low Offset and Drift	100	95	90	± 1 to 50	50 @ 20, 200	18, 0.1 30, 0.02	± 12, 100	4000	0.5, 5	$R_L = 200\Omega$ $V_{cc} = \pm 15V$		√	√		√	
CLC220 Hybrid	General Purpose	200	190	160	± 1 to 50	100 @ 10, 200	8, .01 15, 0.02	± 12, 50	7000	10, 35	$R_L = 200\Omega$ $V_{cc} = \pm 15V$		√	√		√	
CLC221 Hybrid	Low Offset and Drift	200	170	120	± 1 to 50	130 @ 10, 200	15, 0.1 18, 0.02	± 12, 50	6500	0.5, 5	$R_L = 200\Omega$ $V_{cc} = \pm 15V$		√	√		√	
CLC205 Hybrid	Overdrive Protected Low Power	190	170	120	+ 7 to + 50 – 1 to – 50	100 @ 10, 200	22, 0.1 24, 0.05	± 12, 50	2400	3.5, 11	$R_L = 200\Omega$ $V_{cc} = \pm 15V$		√	√		√	
CLC206 Hybrid	Overdrive Protected 100mA Output Current	200	180	90	+ 7 to + 50 – 1 to – 50	70 @ 20, 200	19, 0.1 22, 0.05	± 12, 100	3400	3.5, 11	$R_L = 200\Omega$ $V_{cc} = \pm 15V$		√	√		√	
CLC207 Hybrid	Low Distortion	250	170	90	+ 7 to + 50 – 1 to – 50	100 @ 10, 200	24, 0.05	± 12, 150	2400	3.5, 11	$R_L = 200\Omega$ $V_{cc} = \pm 15V$		√	√		√	
CLC231 Hybrid	Low Gain Low Power	$\|A_v\| = 1$ 165	$\|A_v\| = 2$ 165	$\|A_v\| = 5$ 120	± 1 to 5	95 @ 10, 100	12, 0.1 15, 0.05	± 11, 100	3000	1, 10	$R_L = 100\Omega$ $V_{cc} = \pm 15V$		√	√		√	
CLC232 Hybrid	Low Distortion	$\|A_v\| = 1$ 220	$\|A_v\| = 2$ 175	$\|A_v\| = 5$ 110	± 1 to 5	95 @ 10, 100	15, 0.05	± 12, 100	3000	1, 10	$R_L = 100\Omega$ $V_{cc} = \pm 15V$		√	√		√	
CLC400	Low Cost Low Power	$\|A_v\| = 1$ 220	$\|A_v\| = 2$ 200	$\|A_v\| = 8$ 60	± 1 to 8	50 @ 5 100	12, 0.05	± 3.5, 70	700 (NI) 1600 (IN)	2, 20	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√		√	√	√
CLC401	Low Cost Low Power	$\|A_v\| = 5$ 400	$\|A_v\| = 20$ 150	$\|A_v\| = 50$ 75	± 7 to 50	100 @ 5, 100	10. 0.1	± 3.5, 70	1200	3, 20	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√		√	√	√
CLC402	14-Bit Accurate Low Offset and Drift	$\|A_v\| = 1$ 260	$\|A_v\| = 2$ 190	$\|A_v\| = 8$ 85	± 1 to 8	80 @ 5, 100	25, 0.0025	± 3.5, 55	800	0.5, 3.0	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√		√	√	√
CLC404	High Full-Power BW Low Power, High Slew	$\|A_v\| = 2$ 165	$\|A_v\| = 6$ 175	$\|A_v\| = 20$ 60	+ 2 to + 21 – 1 to – 20	165 @ 5, 100	10, 0.2	± 3.3, 70	2600	2.0, 30	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√		√	√	√
CLC405	Low Cost Low Power	$\|A_v\| = 1$ 130	$\|A_v\| = 2$ 110	$\|A_v\| = 4$ 83	± 1 to 50	40 @ 5, 100	14, .05	± 3.0, 60	400	1.0, 30	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√		√	√	√
CLC406	Low Cost Low Power	$\|A_v\| = 2$ 180	$\|A_v\| = 6$ 160	$\|A_v\| = 10$ 100	± 1 to 10	130 @ 5, 100	12, 0.05	± 2.7, 70	1500	2, 30	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√		√	√	√
CLC407	Low Power, Fast Disable, Programmable Gain	$\|A_v\| = 1$ 175	$\|A_v\| = -1$ 130	$\|A_v\| = 2$ 110	± 1 to 50	40 @ 5, 100	14, .05	± 3.0, 60	400	1.0, 30	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√		√	√	√
CLC409	Very Wideband	$\|A_v\| = 2$ 350	$\|A_v\| = 6$ 150	$\|A_v\| = 10$ 100	± 1 to 10	110 @ 5, 100	8, 0.1	± 3.5, 70	1200	0.5, 25	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√		√	√	√
CLC410	High-Speed Video Op Amp with Disable	$\|A_v\| = 1$ 220	$\|A_v\| = 2$ 200	$\|A_v\| = 8$ 60	± 1 to 8	50 @ 5, 100	12, 0.05	± 3.5, 70	700 (NI) 1600 (IN)	2, 20	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√		√	√	√
CLC411	High-Speed Video Op Amp with Disable	$\|A_v\| = 1$ 275	$\|A_v\| = 2$ 200	$\|A_v\| = 10$ 37	± 1 to 10	75 @ 6, 100	15, 0.1	± 4.5, 70	2300	2, 30	$R_L = 100\Omega$ $V_{cc} = \pm 15V$	√	√		√	√	√

Operational Amplifiers (typical specifications, +25°C) – *Continued*

Part Number	Key Features	– 3dB Bandwidth (MHz)			Optimal Gain Range ($A_v = V_o/V_i$)	Full Power BW (MHz @ V_{pp}, R_L)	Settling Time (nsec, %)	Output (V,mA)	Slew Rate (V/μsec)	Input Offset Drift (mV, μV/°C)	Test Conditions	Versions					
												J	I	K	M	8	L
CLC412	Dual Amp Low Power	$\|A_v\|=1$ 300	$\|A_v\|=2$ 250	$\|A_v\|=10$ 60	± 1 to 10	105 @ 4, 100	12, 0.05	± 3.1, 70	1300	2, 30	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√		√	√	√
CLC414	Quad Amp Low Power	$\|A_v\|=2$ 70	$\|A_v\|=6$ 90	$\|A_v\|=10$ 60	± 1 to 10	55 @ 5, 100	16, 0.1	± 2.8, 70	1000	2, 30	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√		√	√	√
CLC415	Quad Amp High Power	$\|A_v\|=2$ 180	$\|A_v\|=6$ 160	$\|A_v\|=10$ 140	± 1 to 10	120 @ 5, 100	12, 0.1	± 2.6, 70	1500	2, 20	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√		√	√	√
CLC420	Voltage Feedback Low Gain	$\|A_v\|=1$ 300	$\|A_v\|=2$ 100	$\|A_v\|=5$ 25	± 1 to 10	40 @ 5, 100	18, 0.01	± 3.2, 70	1100	0.5, 4/1, 3	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√		√	√	√
CLC422	Voltage Feedback Low Noise Dual	$\|A_v\|=30$ 250	$\|A_v\|=40$ 200	$\|A_v\|=50$ 120	± 30 to ± 200	200 @ 5, 100	17, 0.2	± 3.8, 70	2300	0.8, 2	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√		√	√	√
CLC425	Ultra Low Noise Wideband Op Amp	$\|A_v\|=10$ 60	$\|A_v\|=20$ 85	$\|A_v\|=40$ 40	±10 to ±1000	40 @ 5, 100	22, 0.2	± 3.4, 90	350	0.1, 2	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√		√	√	√
CLC426	Voltage Feedback Ultra Low Noise	$\|A_v\|=2$ 130	$\|A_v\|=5$ 44	$\|A_v\|=10$ 20	± 1 to 1000	50 @ 5, 100	16, 0.05	± 3.8, 80	400	0.3, 5	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√		√	√	√
CLC428	Voltage Feedback Low Noise Dual	$\|A_v\|=1$ 160	$\|A_v\|=2$ 80	$\|A_v\|=5$ 32	± 1 to 1000	50 @ 5, 100	16, 0.1	± 3.5, ± 80	500	± 3.5, ± 5	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√		√	√	√
CLC430	General Purpose with Disable	$\|A_v\|=1$ 100	$\|A_v\|=2$ 75	$\|A_v\|=10$ 19	± 1 to 100	30 @ 10, 100	35, 0.05	± 8, 85 ± 14, ± 85	2000	1, 25	$R_L = 100\Omega$ $V_{cc} = \pm 15V$	√	√		√	√	√
CLC431 CLC432	Dual Amps CLC431 has Disable	$\|A_v\|=1$ 92	$\|A_v\|=2$ 62	$\|A_v\|=10$ 60	± 1 to 100	62 @ 4, 100	70, 0.05	± 6, 70	2000	± 3, 20	$R_L = 100\Omega$ $V_{cc} = \pm 15V$	√	√		√	√	√
CLC440	High Speed Low Power Voltage Feedback	$\|A_v\|=1$ 750	$\|A_v\|=2$ 260	$\|A_v\|=10$ 23	± 1 to 10	190 @ 4, 100	10, 0.5	± 3.0, 90	1500	1, 5	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√			√	√	√
CLC449	Current Feedback 1,200MHz	$\|A_v\|=2$ 1.2GHz	$\|A_v\|=5$ 450	$\|A_v\|=10$ 130	± 1 to 100	350 @ 4, 100	6, 0.2	± 2.9, 90	2500	3, ± 25	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√			√	√	√
CLC501	Clamped Output 1ns Overload Recovery	$\|A_v\|=8$ 165	$\|A_v\|=20$ 120	$\|A_v\|=32$ 80	+ 7 to + 50 − 1 to − 50	80 @ 5,100	12, 0.05	± 3.5, 70	1200	1.5, 10	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√			√	
CLC502	Clamped Output, Low Offset, 14-bit Settling	$\|A_v\|=1$ 190	$\|A_v\|=2$ 150	$\|A_v\|=8$ 75	+ 1 to 8	65 @ 5, 100	25, 0.0025	± 3.5, 55	800	0.5, 3.0	$R_L = 100\Omega$ $V_{cc} = \pm 5V$	√	√			√	
CLC505	Very Low Programmable Supply Current/Power (10mW–100mW)	$\|A_v\|=6$ 50 I_{cc} 1mA	$\|A_v\|=6$ 100 I_{cc} 3.4mA	$\|A_v\|=6$ 150 I_{cc} 9mA	+ 2 to + 21 − 1 to − 20	80 @ 5, 500	14, 0.05	± 3.5, 25	1200	3.0, 40	$R_L = 3.4mA$ $V_{cc} = \pm 5V$	√	√		√	√	√

Variable Gain Amplifiers (typical specifications, +25°C)

Part Number	Key Features	–3dB Bandwidth (MHz)		Gain Adjust Range (dB)	Signal Non-Linearity (%)	Full Power BW (MHz@V_{pp},R_L)	Settling Time (nsec, %)	Output (V,mA)	Slew Rate (V/μsec	Output Offset Drift (mV/μV/°C)	Versions					
		Signal Channel	Control Chan.								J	I	K	M	8	L
CLC520	Voltage Controlled Gain	500	100	– 40	0.04	140 @ 4, 100	12, 0.1	±3.5, 70	2000	40, 100	√	√		√	√	√
CLC522	Variable Gain Amplifier (VGA)	$\|A_v\|=2$ 330	165	– 40	0.04	150 @ 5, 100	12, 0.1	±4, 70	2000	25, 100	√	√		√	√	√

Buffer Amplifiers (typical specifications, +25°C)

Part Number	Key Features	– 3dB Bandwidth (MHz)	Gain (V/V)	Full Power BW (MHz @ V_{pp}, R_L)	Harmonic Distortion (dBc @ 20MHz, $2V_{pp}$)	Settling Time (nsec, %)	Output (V, mA)	Slew Rate (V/μsec)	Output Offset Drift(mV,μV/°C)	Test Conditions	Versions					
											J	I	K	M	8	L
CLC109	Unity-Gain Buffer Low Power	270	0.96	120 @ 2,100	–46,–55	12, 0.5	+3.8, -2.5	350	1, ±10	R_L = 100Ω V_{cc} = ±5V	√	√		√	√	√
CLC110	Closed-Loop Design Low Distortion	730	0.97	90 @ 5,100	–65, –65	5, 0.2	4, 70	800	2, 20	R_L = 100Ω V_{cc} = ±5V	√	√		√	√	√
CLC111	Unity-Gain Buffer High Speed	800	0.98	450 @ 4,100	–62, –62	16, 0.1	±3.5, ±60	3500	2, ±30	R_L = 100Ω V_{cc} = ±5V	√	√		√	√	√
CLC114	Quad Buffer Low Power	200	0.97	95, @ 2, 100	–50, –58	10, 0.1	4, 25	450	.5, 9	R_L = 100Ω V_{cc} = ±5V	√	√		√	√	√
CLC115	Quad Buffer High Speed	700	0.99	270 @ 4, 100	–62, –62	12, 0.1	60	2700	2, 25	R_L = 100Ω V_{cc} = ±5V	√	√		√	√	√
CLC407	Prog. Gain: ±1, +2 Low Power	175	0.99	40 @ 5,100	(dBc @ 10MHz, $2V_{pp}$) –52, –57	14, 0.5	+3.0, 60	400	1, 30	R_L = 100Ω V_{cc} = ±5V	√	√		√	√	√

High Power Amplifiers (typical specifications, +25°C, R_L = 50Ω)

Part Number	Key Features	-3dB Bandwidth (MHz)	Large Signal Bandwidth (MHz@V_{pp})	2nd/3rd Harmonic Distortion (dBc)				Rise Time (nsec)	Input Offset Drift (mV,μV/°C)	Optimal Gain Range (V/V)	R_{out} Range (Ω)	Output (V, mA)	Versions			
				10dBm ($2V_{pp}$)		24dBm ($10V_{pp}$)							I	K	M	8
				20MHz	100Mhz	20MHz	100MHz									
CLC561 Hybrid	High-power, adjustable output impedance	215	150 @10V_{pp} (24dBm)	–59/ –62	–35/ –49	–50/ –41	–40/ –30	1.5	2.0, 35	+ 5 to + 80	25Ω to 200Ω	± 10V, 200mA	√	√		√

Analog Multiplexers (typical specifications, +25°C)

Part Number	Channels	Switching Speed (ns)	Input Voltage Range	Crosstalk Rejection (dB)	Settling Time to 0.01%	Settling Time to 0.0025%	2nd Harmonic Distortion (dBc)	3rd Harmonic Distortion (dBc)	Digital Interface	Features	Versions					
											J	I	K	M	8	L
CLC532	2:1	6	±3.4V	- 80	17ns	35ns	- 80	- 86	TTL/ECL	Buffered input/output	√	√			√	
CLC533	4:1	6	±3.4V	- 80	17ns		- 80	- 86	TTL/ECL	Buffered input/output	√	√			√	

Modular Series Encased Amplifiers

Part Number	-3dB Bandwidth (MHz)	Gain* (dB)	Gain Flatness (dB to MHz)	R_{in} & R_{out} (Ω)	Output at -1dB Gain Compression (+dBm@MHz)	Rise & Fall Time (nsec)	Overload Recovery Time (nsec)	Group Delay (nsec)	Deviation from Linear Phase (°)	Equivalent Input Noise (μV_{rms})	Package
CLC100	500	20	± 0.05 to 300	50	12 @ 500	0.600	< 2	1.4	1	20	1.9" X 4.14" Mach. Alum. Case
CLC102	250	15	± 0.4 to 200	50	26 @ 100	1.6	—	2.3	1	46	3.0" X 3.0" Mach. Alum. Case

*CLC100 is non-inverting gain, CLC102 is inverting gain.

Modular Series Encased Amplifiers – *Continued*

Part Number	Gain (Matched Load) (dB)	Bandwidth P_{out} (MHz, dBm)	Input Impedance (Ω)	Output Impedance (Ω)	V_{out}, I_{out} (Matched Load) (V, mA)	Power Supply Range (V)	Output Current (mA)	Input Voltage (V)
CLC140	20	500, 10	50	50	± 1.25, ± 15	± 5 to ± 16	± 20	± 0.5
CLC142	15 (inv.)	250, 18	50	50	± 10, ± 250	± 12 to ± 16	± 250	±2
CLC143	15 (inv.)	220, 18	50	50	± 10, ± 250	± 12 to ± 16	± 250	± 2

Part Number	Gain (Open Load) (V_o/V_i)	Bandwidth P_{out} (MHz, dBm)	Input Impedance (Ω)	Output Impedance (Ω)	V_{out}, (Open Load) I_{out} (V, mA)	Power Supply Range (V)	Output Current (mA)	Input Voltage (V)
CLC162	2 to 5	250, 10	50 to 1k	50 to 1k	± 10, ± 100	± 5 to ± 16	± 150	± 6
CLC163	5 to 40	170, 10	50 to 1k	50 to 1k	± 10, ± 100	± 5 to ± 16	± 150	*
CLC166	10 to 40	170, 10	50 to 200	50 to 1k	± 10, ± 50	± 5 to ± 16	± 75	*
CLC167	10 to 40	150, 10	50 to 200	50 to 1k	± 10, ± 200	± 10 to ± 16	± 200	*

*The output must not be overdriven for these parts. The maximum $\pm V_{in}$ will be $\pm (|V_{cc}| - 4V)/A_v$

Analog-to-Digital Converters (typical specifications, +25°C)

Part Number	Resolution (Bits)	Sampling Rate (MSPS)	Input Voltage Range	Differential Non-Linearity (LSB's)	Spurious Free Signal Range SFSR (dB)	SNR (excl. harmonics) (dB)	Dynamic Test Conditions	Digital Interface	Architecture	Features	Versions					
											C	J	I	K	M	8
CLC925B Hybrid	12	dc to 10	$2V_{pp}$ over a –2V to + 2V range	0.35	66.8	66.6	F_s =10MSPS F_{in} =4.996MHz FS –1dB	TTL	Complete Subsystem	Internal T/H and reference; has gain and offset adjust			√	√		√
CLC935B Hybrid	12	dc to 15	±1V	0.6	74.2	65.2	F_s =15MSPS F_{in} =7.22MHz FS –1dB	ECL	Complete Subsystem		√			√		√
CLC936C Hybrid	12	dc to 20	±1V	0.6	72.4	64.3	F_s =20MSPS F_{in} =9.663MHz FS –1dB	ECL	Complete Subsystem		√			√		√
CLC937B Hybrid	12	dc to 25.6	±1V	0.8	71.0	64.0	F_s =25.6MSPS F_{in} =9.89MHz FS –1dB	ECL	Complete Subsystem		√			√		
CLC938C Hybrid	12	dc to 30.72	±1V	1.2	70.6	63.7	F_s =30MSPS F_{in} =9.37MHz FS –1dB	ECL	Complete Subsystem		√			√		

Analog to Digital Converters (typical specifications, +25°C) – *Continued*

Part Number	Resolution (Bits)	Sampling Rate (MSPS)	Input Voltage Range	Differential Non-Linearity (LSB's)	Spurious Free Signal Range SFSR (dB)	SNR (excl. harmonics) (dB)	Dynamic Test Conditions	Digital Interface	Power Dissipation (W)	Architecture	Features	Versions					
												C	J	I	K	M	8
CLC949	12	dc to 20	±2V Differential	0.6	72.0	65.0	F_s = 20MSPS F_{in} = 9.663MHz FS –1dB F_s = 5MSPS	CMOS	0.22 0.07*	Complete Subsystem*	Internal T/H and Reference	√					

*User adjustable bias

Track & Hold Amplifiers (typical specifications, +25° C, $R_L = R_S = 50\Omega$, $V_{CC} = \pm 15V$)

Part Number	H-to-T Acquisition Time, Tolerance (nsec)	T-to-H Settling Time to 1mV (nsec)	Effective Aperture Delay (nsec)	Aperture Jitter ($psec_{rms}$)	–3dB Bandwidth (MHz)	Slew Rate (V/µs)	Pedestal Offset (mV)	Feedthrough Rejection (dB at 20MHz)	Output (± V, mA)	Digital Control	Versions				
											J	I	K	M	L
CLC942 Hybrid	20, 0.1 25, 0.01	5	–1.5	1.4	70	300	8	78	2.2 50	ECL		√		√	

Serial Digital Interface (typical specifications, +25°C)

Part Number	Description	Key Features	Data Rate Range (Mbps)	Rise/Fall Time (ps)	Supply Current		Residual Jitter (ps)	Output Voltage Swing (V_{pp})	Propagation Delay (ns)	Versions		
					No Load (mA)	Outputs Loaded (mA)				C	J	8
CLC006	Cable Driver	Low power, 2 outputs, adjustable output voltage	0 to >400	650	33	36	25	1.6 (adjustable)	1.0		√	
CLC007	Cable Driver	Low power, 4 outputs	0 to >400	650	33	38	25	1.6	1.0		√	

Comlinear reserves the right to change specifications without notice.

To fit your individual applications Comlinear screens their products for performance at various levels and temperature ranges.

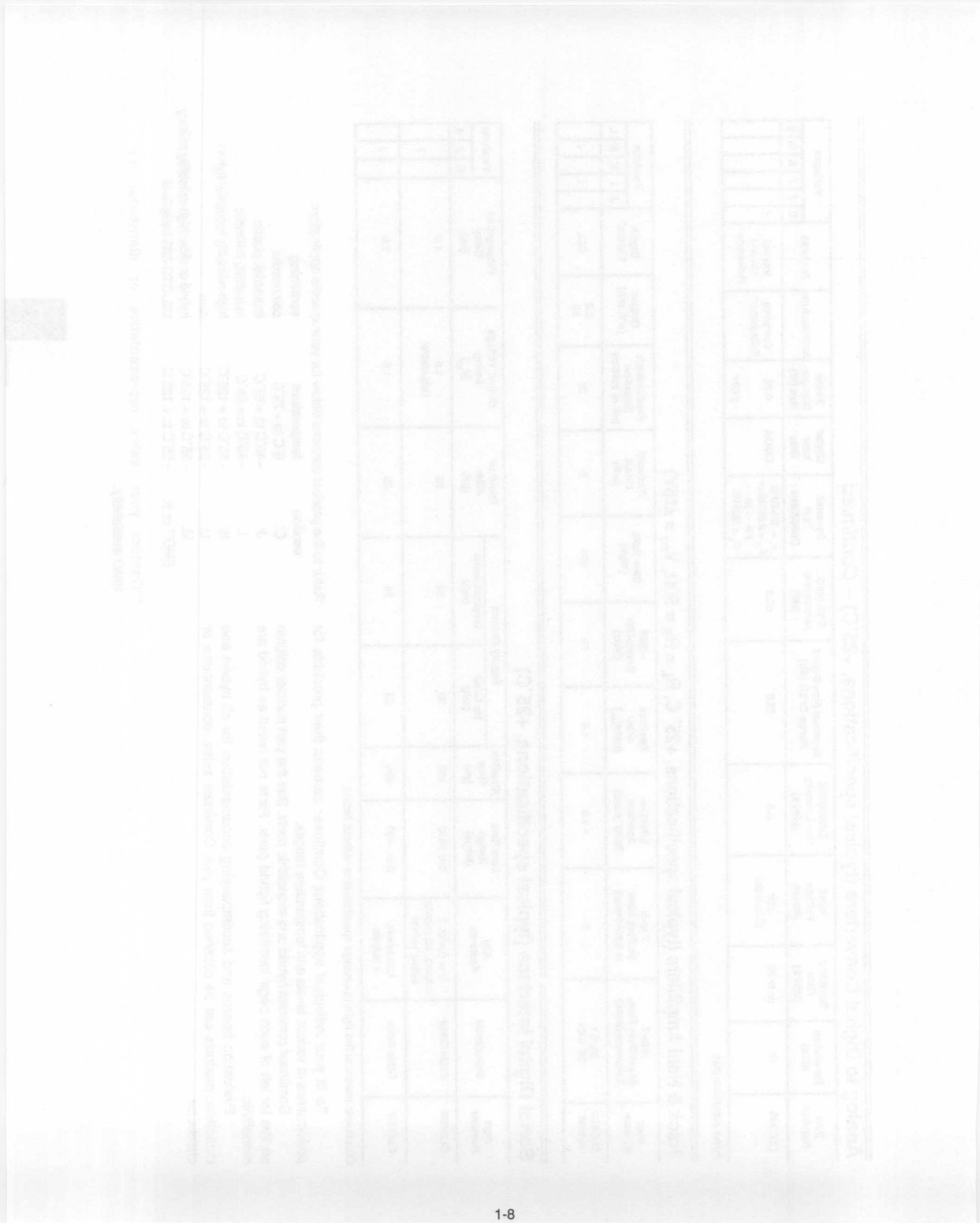
Comlinear provides hybrid and monolithic parts. See the part number column on the far left of each page identifying hybrid parts. Parts not noted as hybrid are monolithic.

Evaluation boards and accompanying documentation for all hybrid and monolithic products can be obtained from your Comlinear sales representative or distributor.

Refer to the product versions below for your specific application:

version	temperature	screening
C:	0°C to + 70°C	commercial
J:	– 40°C to + 85°C	industrial, plastic
I:	– 40°C to + 85°C	industrial, hermetic
K:	– 55°C to + 125°C	high-reliability industrial hybrid
L:	– 55°C to + 125°C	dice
M:	– 55°C to + 125°C	hybrid or dice: high-reliability military
SMD** or 8:	– 55°C to + 125°C	MIL-STD-883 compliant

**Contact your sales representative or distributor for SMD availability.



Quality and Reliability
Contents

Quality and Reliability

OUR QUALITY POLICY

- Comlinear Corporation is committed to providing products and customer service which meet or exceed our customers' expectations and requirements.
- Quality attitudes and the Quality System are the foundation on which Comlinear will conduct business, supported by all employees in the performance of their everyday functions.
- Continuous improvement of the Quality System is a Comlinear commitment in order to raise the level of Quality in all areas.
- Execution of the Quality System will advance and strengthen Comlinear to fulfill its mission and values.
- Overall Quality responsibility starts with executive management and is every employee's job, supported by management through training and guidance.

We elevate quality beyond its typical stature as a military mandated program, to foster an environment where it becomes a pervasive operating attitude. Comlinear's ability to deal with the required elements of a quality program is shown by the continual maintenance of our MIL-STD-1772 facility certification, and our MIL-STD-883 compliant, DESC SMD approved, monolithic and hybrid products.

What makes Comlinear a preferred supplier is our efforts to address the competitive challenge in today's market by focusing on quality throughout the company.

Our commitment to product assurance means we start with the required systems and enhance them with the most up-to-date quality assurance techniques available. Tools such as SPC, quality improvement teams, and experimental design are all used in an environment of Total Quality.

Applying these techniques is the responsibility of all managers and employees. And the desire for continuous quality improvement is found in areas ranging from accounting, research and development, and computer services to manufacturing processes and shipment.

The Quality Assurance group supports these efforts by providing technical resources in quality engineering for failure analysis, reliability monitoring, and process improvement. Quality levels in manufacturing are continually measured and the information is supplied to and reviewed with responsible managers.

Comlinear has obtained certification to the International Organization for Standardization (ISO), specification 9001. This effort will solidify Comlinear's commitment to fulfilling customer needs and achieving product and service excellence.

PRODUCTS AND TECHNOLOGIES

Comlinear's hybrid circuit manufacturing is located in our MIL-STD-1772 certified production line in Fort Collins, Colorado. Our capabilities include high density thin film substrate fabrication incorporating high precision, high stability tantalum nitride resistors, gold metalization, and alumina substrates.

Monolithic microcircuits are fabricated in the USA using a high speed complementary bipolar integrated circuit process. This combination has demonstrated an actual failure rate for ICs of less than 1.0 FIT in lifetesting.

Monolithic products are available in industrial commercial, and Class B and S MIL-STD-883 compliant.

Hybrid products are available in industrial, commercial, and Class H of MIL-H-38534. Though our hybrid products can be processed to selected K (space) level criteria, the final product would not be compliant or certified to MIL-STD-883 or MIL-H-38534, K level.

ENVIRONMENTAL IMPACT/SAFETY AWARENESS

Comlinear does not use ozone depleting substances (ODS) in its manufacturing processes and is persuading its suppliers to comply with the Montreal Protocol and all U.S. Federal regulations.

The flammability rating of plastic encapsulated monolithic products is 94V-0 of the UL-94 Flame Class (this rating is subject to change without notification).

The following section outlines the various flows for both the hybrid and the monolithic product lines and provides additional reliability data.

Space Level Products

Comlinear has the expertise, product lines and demonstrated reliability to support your space-based systems. In addition, we have the experience and program management necessary to meet the unique demands of processing space level.

The monolithic product lines have been designed for the robust, reliable assembly and high radiation tolerance necessary for success in the space system environment.

Our standard monolithic space product flow is self certified and DESC audited to 1.2.1.b of MIL-STD-883, Class "S." We also support the European equivalent space level flow, ESA9000, Level B, using MIL-STD-883 test methods.

Recognizing the special nature of space programs and the impact of component performance on system capability, we are fully prepared to provide either our standard "S" Level screening or full custom processing flows to suit your application requirements.

Below are the space products we have qualified to date and the appropriate package designators. Contact Comlinear for specific information.

CLC400ASF
CLC401ASD/ASF
CLC404ASD
CLC414ASD
CLC415ASH
CLC420ASD
CLC501ASD/ASH
CLC502ASH
CLC505ASD/ASH
CLC520ASD/ASH
CLC533ASB

Definition of suffixes:
ASB=Space, Cerdip package
ASD=Space, Side Brazed Dip package
ASF=Space, Ceramic/Metal Flatpackage
ASH=Space, Cerpak (Ceramic Flatpackage)

Radiation Data

Radiation testing has been completed on several Comlinear products at different levels. Our complementary bipolar IC process, for instance, has shown radiation tolerance up to one megarad total dose.

Radiation Test Data Summary

Part Number	Package Type	Qty	Date Code	Neutron Irrad. (neutron/cm^2)	Total Dose (Krads)	Dose Rate	Result Summary
CLC205*	TO-8	5	8931	None	50, 100, 300, 1000	126 rads Si/sec	Devices withstood radiation to 1Mrad (Si) with little degradation.
CLC220*	TO-8	4	8508	3.36 x 10^{12}	100, 300, 500, 1000	Unknown	No change in AC characteristics. Slight change in DC bias characteristics.
CLC231*	TO-8	4	-	1.2 X 10^{12} 3.2 X 10^{12} 9.9 X 10^{12} 25 X 10^{12} 36 X 10^{12}	None	None	Slight change in DC operating characteristics and distortion. No change in gain and bandwidth.
CLC400 (54 X 54 Mil typ. die size)	Ceramic Side Brazed Dip	6	8817	None	10, 30, 100, 300, 1000	140 rads(Si)/sec	Negligible degradation to 1000 krads specification. Should meet specification to 3000 krads.
CLC400 (39 X 39 Mil typ. die size)	Flat Pkg.	8	9452	1 X 10^{12}	30, 100, 300, 1000	50 rads/sec	Very slight change in DC operating point.
CLC401 (54 X 54 Mil typ. die size)	Ceramic Side Brazed Dip	2	-	1.85 X 10^{14}	None	None	Very little change in the small signal frequency response over a wide gain range.
CLC401 (39 X 39 Mil typ. die size)	Ceramic Side Brazed Dip	4	9136	None	10, 30, 50, 100	570 rads (Si)/min	No degradation of gain at all; slight degradation of bandwidth at initial radiation exposure only.
CLC401 (39 X 39 Mil typ. die size	Flat Pkg	8	9452	1 X 10^{12}	30, 100, 300, 1000	50 rads/sec	Very slight change in DC operating point.
CLC501	Plastic Dip	2	-	None	5, 10, 15, 20, 25	500 rads/hr	No degradation of gain at all; slight degradation of bandwidth at initial radiation exposure only.
CLC501	Ceramic Side Brazed Dip	7	9231	6 X 10^{11}	30, 60, 100, 150, 200	50 rads/sec	Slight change in DC bias characteristics. No AC testing performed.
CLC520	Cerpak	8	9504	1 X 10^{12}	30, 100, 300, 1000	50 rads/sec	Very slight change in DC operating point.
CLC925*	Ceramic Side Brazed Dip	2	-	None	0.5, 1, 1.5, 2, 5, 10, 20, 38, 40,50, 56	Unknown	Performance is virtually constant from 0 to 56 krad total dose. Any trend versus total dose is obscured by test repeatability.

March 31, 1995

* Product is Hybrid.

Reliability Predictions

This listing provides mean time between failure (MTBF) rate prediction analysis, calculated in accordance with MIL-HDBK-217E. The stated values are for MIL-STD-883, B level, H level, or Comlinear M level processed versions. For monolithic products, the number range of transistors has been shown; these products are achieving a continuous tested FIT (Failures in Time) rate of <1.0 fails per billion device hours

Monolithic			Hybrid		
[1]Part #	FITs @ 25C	MTTF @ 25C (million hours)	Part #	FITs @ 25C	MTTF @ 25C (million hours)
CLC109A8B	6.67	149.9	CLC103AM	60.2	16.6
CLC110A8B	11.554	86.6	CLC200A8C	90.2	11.1
CLC111A8B	13.73	72.8	CLC201A8C	43.2	23.1
CLC114A8B	22.7	44.1	CLC203AM	59	16.9
CLC115A8D	77	13.0	CLC205A8C	21.4	46.7
CLC400A8B	40.6	24.6	CLC206A8C	23.3	42.9
CLC401A8B	31.4	31.8	CLC207A8C	26.2	38.2
CLC402A8D	22.6	44.2	CLC220A8C	93.7	10.7
CLC404A8D	10.9	91.7	CLC221A9C	50	20.0
CLC406A8B	8.8	113.6	CLC231A8C	20.4	49.0
CLC409A8D	12.7	78.7	CLC232A8C	22	45.5
CLC410A8B	18.8	53.2	CLC300A	39.8	25.1
CLC411A8B	64.2	15.6	CLC560A8C	58.9	17.0
CLC412A8B	9.68	103.3	CLC561A8C	58.6	17.1
CLC414A8D	42.3	23.6	CLC922B8C	328	3.0
CLC415A8D	79.7	12.5	CLC925B8	393	2.5
CLC420A8D	6.64	150.6	CLC926B8C	393	2.5
CLC422A8B	32.5	30.8	CLC935B8C	307	3.3
CLC425A8B	20.8	48.1	CLC936B8C	300	3.3
CLC426A8B	8.7	114.9	CLC936C8C	325	3.1
CLC428A8B	39.3	25.4	CLC937B8C	288	3.5
CLC430A8B	50.6	19.8	CLC938C8C	290	3.4
CLC430A8L	13	76.9			
CLC431A8B	63.4	15.8			
CLC432A8B	113	8.8			
CLC500A8D	17	58.8			
CLC501A8D	23.4	42.7			
CLC502A8D	23.3	42.9			
CLC505A8D	8.2	122.0			
CLC520A8D	26.1	38.3			
CLC522A8B	55	18.2			
CLC532A8B	15.3	65.4			
CLC532A8D	14.3	69.9			
CLC533A8B	32.5	30.8			

[1]Based on MIL-STD-883, B level, H level or our M level versions; per MIL-HDBK-217F; Ground benign (GB) at 25°C ambient still air.

HYBRID

	883 CLASS H	Comlinear S Level	I, C LEVEL	M LEVEL	K LEVEL [3]
Element Evaluation per MIL-H-38534		X			
Assembly	X	X	X	X	X
100% NDT Bond Pull M 2023		X			
Internal Visual M 2017	X	X	X (indus. spec.)	X (with exceptions)	X (Indus. spec.)
Thermal Shock Cond. A M1011	X	X		X	
Constant Acceleration M 2001 Cond. A	X	X		X	
PIND M 2020 Cond. B		X			
Pre-burn-in Electrical Test (Per SCD)	X (optional)	X		X (optional)	
Burn-in M 1015	X	X		X	X +125°C for 24 hrs
Final Electrical Test (Per SCD)	X +25°C +125°C -55°C	X +25°C +125°C -55°C	X +25°C	X +25°C +125°C -55°C	X +25°C +125°C -55°C
Fine & Gross Leak M 1014	X	X		X	X
X-Ray M 2012		X			
External Visual M 2009	X	X	X (Indus. spec)	X (Indus. spec)	X (Indus. spec)
Quality Conformance Inspection Group A, B, C, D	X [2]	X [2]		X (when specified by contract)	

[1] All processing flows are based on MIL-STD-883, MIL-H-38534 and are subject to change to correspond to current revisions. MXXXX references are to test methods in MIL-STD-883.

[2] Quality Conformance Inspection is per MIL-H-38534, option 1 (in-line).

[3] Comlinear identification of an industrial grade flow. Not a MIL-H-38534 "Class K" equivalent.

Quality Conformance Inspection
MONOLITHIC

	883 COMPLIANT		INDUSTRIAL	COMMERCIAL	
	CLASS S	CLASS B	I LEVEL	J LEVEL	C LEVEL
Wafer Lot Acceptance M 5007	X				
100% NDT Bond Pull M 2023	X				
Internal Visual M 2010	X Cond. A	X Cond. B	X Cond. B	X Comm. Spec	X Comm. Spec
Temperature Cycling M 1010 Cond. C	X	X	X		
Constant Acceleration M 2001 Cond. E	X	X			
PIND M 2020 Cond. A	X				
Serialization	X				
Pre-burn-in Electrical Test (When specified in detail SCD)	X	X			
Burn-in M 1015	X	X			
Interim Electrical Test (Per SCD)	X				
PDA Calculation	X 3%	X 5%			
Final Electrical Test (Per SCD)	X +25°C +125°C -55°C	X +25°C +125°C -55°C	X +25°C DC	X +25°C DC	X +25°C DC
Fine & Gross Leak M 1014	X	X	X		
X-Ray M 2012	X				
External Visual M 2009	X	X	X Indus. Spec	X Comm. Spec	X Comm. Spec
Quality Conformance Inspection M 5005	X	X			
Industrial/Commercial Process Control Monitor			X	X	X

All processing flows are based on MIL-STD-883 or PRF-38535 and are subject to change to correspond to current revisions. MXXXX references are to test methods in MIL-STD-883.

Quality Conformance Inspection
MONOLITHIC

Class B and S
Group A Requirements
METHOD 5005/MIL-STD-883

SUBGROUPS TESTED AS A GROUP	CATEGORY	TEMPERATURE	SAMPLE SIZE (ACCEPT #)
1 4 7	Static Tests Dynamic Tests Functional Tests	+25°C	116(0)
2 5 8a	Static Tests Dynamic Tests Functional Tests	+125°C	
3 6 8b	Static Tests Dynamic Tests Functional Tests	-55°C	
9	Switching Test	+25°C	
10	Switching Test	+125°C	
11	Switching Test	-55°C	

Class B
Group B Requirements

SUBGROUP	TEST	MIL-STD-883 TEST METHOD/CONDITION	SAMPLE SIZE (ACCEPT #)
B2	RESISTANCE TO SOLVENTS	2015	3(0)
B3	SOLDERABILITY	2003	22 (0) LEADS FROM 3 DEVICES MINIMUM
B5	BOND STRENGTH	2011 CONDITION D	15(0) WIRES FROM 4 DEVICES MINIMUM

Group C, Class B

SUBGROUP	TEST	MIL-STD-883 TEST METHOD/CONDITION	SAMPLE SIZE (ACCEPT #)
C1	a. Board Check	1005	PER SPEC
	b. Life Test		45(0)
	c. End Point Electrical Test +25°C DC minimum[1]		

NOTES:

Life Test sample devices may be shipped after completion and passing of all final electrical tests (+25°C AC, +125°C AC/DC, -55°C AC/DC) per the applicable device SCD.

Quality Conformance Inspection
MONOLITHIC

SUBGROUP	TEST	MIL-STD-883 TEST METHOD/CONDITION	SAMPLE SIZE (ACCEPTANCE #)
B1	a. Physical Dimensions	2016	2(0)
	b. Internal Water Vapor (Glass-Frit-Seal)	1018	3(0) or 5(1) 5000 ppm @ 100°C
B2	a. Resistance to Solvents	2015	3(0)
	b. Internal Visual & Mechanical	2013 2014	2(0)
	c. Bond Strength	2011 Condition D	22(0) wires from 4 devices minimum
	d. Die Shear	2019	3(0)
B3	Solderability	2003	22(0) wires from 3 devices minimum
B4	a. Lead Integrity	2004, cond. B2	45(0) leads from 3 devices minimum
		2004, Cond. D (Leadless Chip Carriers Only)	15 (0) pads, from 3 devices min. (Leadless Chip Carriers only)
	b1. Fine Leak [1] b2. Gross Leak	1014 Cond. A2 1014 Cond. C1	As applicable
	c. Lid Torque [2]	2024 as applicable	
B5[3]	a. Pre-Life Test Electrical Test	Grp. A, Subgroup 1,2,3 per SCD +25°C, -55°C, +125°C DC	45(0)
	b1. Board Check	1005	100%
	b2. Device Functional Test		
	b3. Steady State Life	1005, Cond. B	45(0)
	b4. Device Functional Test	1005	100%
	c. Post- Life Test Electrical Test	Grp. A, Subgroup 1,2,3 per SCD +25°C, -55°C, +125°C DC	45(0)
B6	a. End Point Electrical Test	+25°C AC/DC per SCD	15(0)
	b. Temperature Cycling	1010 Cond. C 100 cycle minimum	
	c. Constant Acceleration	2001 Cond. E, Y1	
	d1. Fine Leak	1014, Cond. A2	
	d2. Gross Leak	1014, Cond. C1	
	e. End Point Electrical Test	+25°C AC/DC per SCD	

NOTES:

[1] Fine and Gross Leak test for Subgroup B4b need be performed only for packages having leads exiting though a glass seal.

[2] Lid Torque applies only to glass-frit-sealed packages.

[3] Sample devices may be shipped after completion and passing all final electrical tests (+25°C, +125°C, -55°C) per the applicable device SCD.

Quality Conformance Inspection
MONOLITHIC

Class B and S Group D Requirements

SUB-GROUP	TEST	SAMPLE SIZE (ACCEPT #)	MIL-STD-883 TEST METHOD/CONDITION
D1	Physical Dimensions	15(0)	2016
D2	a. Lead Integrity	45(0) leads/terminals from 3 devices minimum	2004, Condition B2
		15(0) pads from 3 devices minimum	2004, Condition D, Leadless Chip Carriers
	D2 Fine and Gross Leak tests are required only with packages with leads exiting through a glass seal (i.e., Cerdips, Cerpacks).		
	b.1 Fine Leak b.2 Gross Leak	45(0)	1014, Applicable Condition
D3	D3 devices may be used for D4 tests.		
	a. Thermal Shock	15(0)	1011, Condition B minimum 15 cycles minimum
	b. Temperature Cycle		1010, Condition C 100 cycles minimum
	c. Moisture Resistance		1004
	End-point Electrical test must be completed within forty-eight (48) hours after removal from the Moisture Resistance chamber.		
	d. End-point Electrical		+25°C DC, subgroup 1
	e. Visual Exam		1004, 1010
	f.1 Fine Leak f.2 Gross Leak		1014, Applicable condition
D4	D3 devices may be used for D4 tests.		
	a. Mechanical Shock	15(0)	2002, Condition B minimum
	b. Variable Frequency Vibration		2007, Condition A minimum
	c. Constant Acceleration		2001, Condition E minimum, Y1 axis
	d.1 Fine Leak d.2 Gross Leak		1014, Applicable condition
	e. Visual Exam		1010 or 1011
	f. End-point Electrical		+25°C DC, subgroup 1
D5	a. Salt Atmosphere	15(0)	1009, Condition A minimum
	b. Visual Exam		1009
	c.1 Fine Leak c.2 Gross Leak		1014, Applicable condition
D6	Internal Water Vapor	3(0) or 5(1)	1018
D7	Adhesion of Lead Finish is not applicable to Leadless Chip Carriers.		
	Adhesion of Lead Finish	15(0)	2025
D8	Lid Torque applies only to glass-sealed devices (i.e., Cerdips, Cerpacks).		
	Lid Torque	5(0)	2024

Operational Amplifiers
Contents

Comlinear
A National Semiconductor Company

Low-Cost, Low-Power, 110MHz Op Amp with Disable

CLC405

APPLICATIONS:

- Desktop Video Systems
- Multiplexers
- Video Distribution
- Flash A/D Driver
- High-Speed Switch/Driver
- High-Source Impedance Applications
- Peak Detector Circuits
- Professional Video Processing
- High Resolution Monitors

FEATURES:

- Low-cost
- Very low input bias current: 100nA
- High input impedance: 6MΩ
- 110MHz -3dB bandwidth (A_V = +2)
- Low power: I_{cc} = 3.5mA
- Ultra-fast enable/disable times
- High output current: 60mA

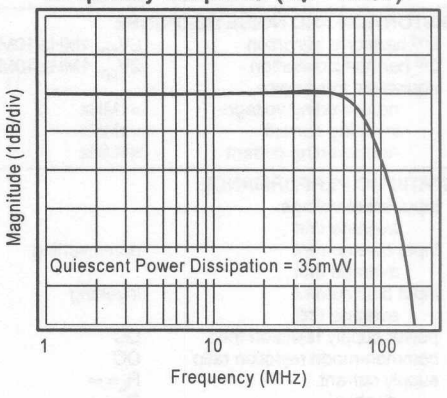
DESCRIPTION

The CLC405 is a low-cost, wideband (110MHz) op amp featuring a TTL-compatible disable which quickly switches off in 18ns and back on in 40ns. While disabled, the CLC405 has a very high input/output impedance and its total power consumption drops to a mere 8mW. When enabled, the CLC405 consumes only 35mW and can source or sink an output current of 60mA. These features make the CLC405 a versatile, high-speed solution for demanding applications that are sensitive to both power and cost.

Utilizing Comlinear's proven architectures, this current feedback amplifier surpasses the performance of alternative solutions and sets new standards for low power at a low price. This power-conserving op amp achieves low distortion with -72dBc and -70dBc for second and third harmonics respectively. Many high source impedance applications will benefit from the CLC405's 6MΩ input impedance. And finally, designers will have a bipolar part with an exceptionally low 100nA non-inverting bias current.

With 0.1dB flatness to 50MHz and low differential gain and phase errors, the CLC405 is an ideal part for professional video processing and distribution. However, the 110MHz -3dB bandwidth (Av = +2) coupled with a 350V/µs slew rate also make the CLC405 a perfect choice in cost-sensitive applications such as video monitors, fax machines, copiers, and CATV systems.

Frequency Response (A_V = +2V/V)



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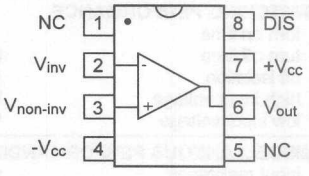
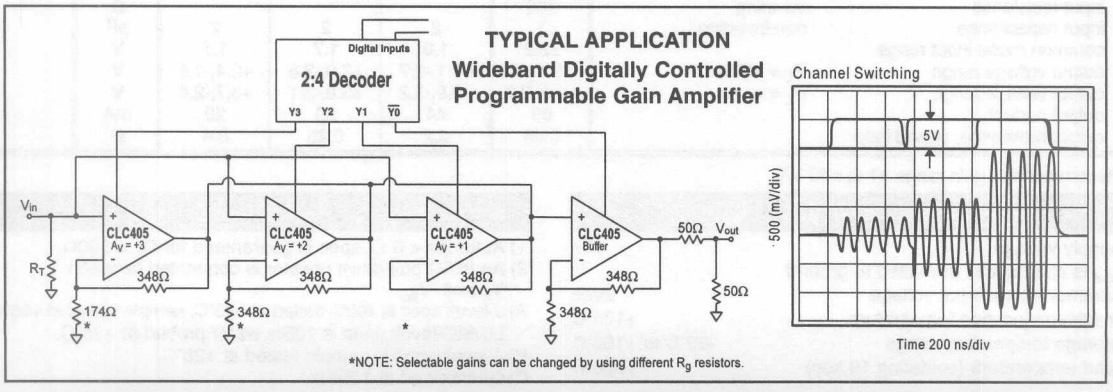
DIP & SOIC



TYPICAL APPLICATION
Wideband Digitally Controlled Programmable Gain Amplifier



*NOTE: Selectable gains can be changed by using different R_g resistors.

CLC405 Electrical Characteristics (A_V = +2, R_f = 348Ω: V_{cc} = ± 5V, R_L = 100Ω unless specified)

PARAMETERS	CONDITIONS	TYP	GUARANTEED MIN/MAX			UNITS	NOTES
Ambient Temperature	CLC405AJ	+25°C	+25°C	0 to 70°C	-40 to 85°C		
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth	V_{out} < 1.0V_{pp}	110	75	50	45	MHz	B
	V_{out} < 5.0V_{pp}	42	31	27	26	MHz	1
-3dB bandwidth A_V = +1	V_{out} < 0.5V_{pp} (R_f = 2K)	135				MHz	
±0.1dB bandwidth	V_{out} < 1.0V_{pp}	50	15			MHz	
gain flatness	V_{out} < 1.0V_{pp}						
peaking	DC to 200MHz	0	0.6	0.8	1.0	dB	B
rolloff	<30MHz	0.05	0.3	0.4	0.5	dB	B
linear phase deviation	<20MHz	0.3	0.6	0.7	0.7	deg	
differential gain	NTSC, R_L=150Ω	0.01	0.03	0.04	0.05	%	
	NTSC, R_L=150Ω (Note 2)	0.01				%	2
differential phase	NTSC, R_L=150Ω	0.25	0.4	0.5	0.55	deg	
	NTSC, R_L=150Ω (Note 2)	0.08				deg	2
TIME DOMAIN RESPONSE							
rise and fall time	2V step	5	7.5	8.2	8.4	ns	
settling time to 0.05%	2V step	18	27	36	39	ns	
overshoot	2V step	3	12	12	12	%	
slew rate A_V = +2	2V step	350	260	225	215	V/µs	
A_V = -1	1V step	650				V/µs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 1MHz/10MHz	-72/-52	-46	-45	-44	dBc	B, C
3rd harmonic distortion	2V_{pp}, 1MHz/10MHz	-70/-57	-50	-47	-46	dBc	B, C
equivalent input noise							
non-inverting voltage	>1MHz	5	6.3	6.6	6.7	nV/√Hz	
inverting current	>1MHz	12	15	16	17	pA/√Hz	
non-inverting current	>1MHz	3	3.8	4	4.2	pA/√Hz	
STATIC DC PERFORMANCE							
input offset voltage		1	5	7	8	mV	A
average drift		30	50		50	µV/°C	
input bias current	non-inverting	100	500	700	1100	nA	A
average drift		3		8	11	nA/°C	
input bias current	inverting	1	5	6	8	µA	A
average drift		17		40	45	nA/°C	
power supply rejection ratio	DC	52	47	46	45	dB	B
common-mode rejection ratio	DC	50	45	44	43	dB	
supply current	R_L= ∞	3.5	4.0	4.1	4.4	mA	A
disabled	R_L= ∞	0.8	0.9	0.95	1	mA	A
SWITCHING PERFORMANCE							
turn on time		40	55	58	58	ns	
turn off time	to >50dB attn. @ 10MHz	18	26	30	32	ns	
off isolation	10MHz	59	55	55	55	dB	
high input voltage	V_{IH}		2	2	2	V	
low input voltage	V_{IL}		0.8	0.8	0.8	V	
MISCELLANEOUS PERFORMANCE							
input resistance	non-inverting	6	3	2.4	1	MΩ	
input resistance	inverting	182				Ω	
input capacitance	non-inverting	1	2	2	2	pF	
common mode input range		±2.2	1.8	1.7	1.5	V	
output voltage range	R_L = 100Ω	+ 3.5,-2.8	+3.1,-2.7	+2.9,-2.6	+2.4,-1.6	V	
output voltage range	R_L = ∞	+4.0,-3.3	+3.9,-3.2	+3.8,-3.1	+3.7,-2.8	V	
output current		60	44	38	20	mA	
output resistance, closed loop		0.06	0.2	0.25	0.4	Ω	

Recommended gain range ±1 to ±40 V/V

Absolute Maximum Ratings

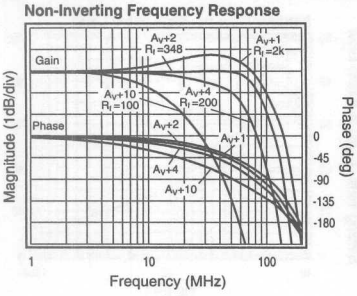
supply voltage	±7V
I_{out} is short circuit protected to ground	
common-mode input voltage	±Vcc
maximum junction temperature	+175°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

Notes

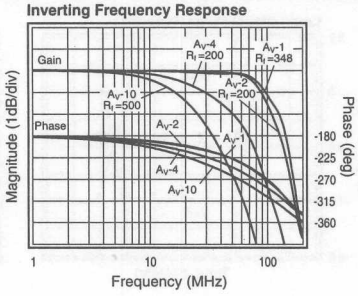
1) At temps < 0°C, spec is guaranteed for R_L = 500Ω.
2) An 825Ω pull-down resistor is connected between V_o and -V_{cc}. .
A) J-level: spec is 100% tested at +25°C, sample tested at +85°C. LC/MC-level: spec is 100% wafer probed at +25°C.
B) J-level: spec is sample tested at +25°C.
C) Guaranteed at 10MHz.

CLC405 Typical Performance Characteristics (A_V = +2, R_f = 348Ω: V_{CC} = ± 5V, R_L = 100Ω unless specified)

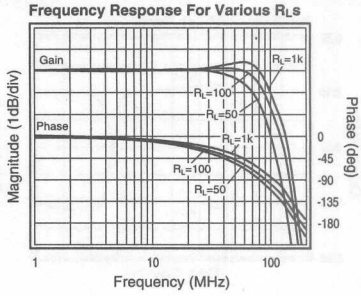
Non-Inverting Frequency Response



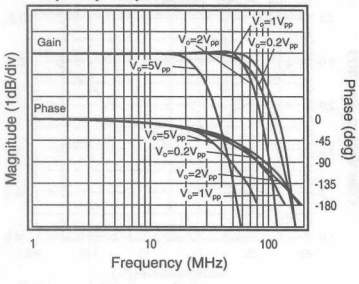
Inverting Frequency Response



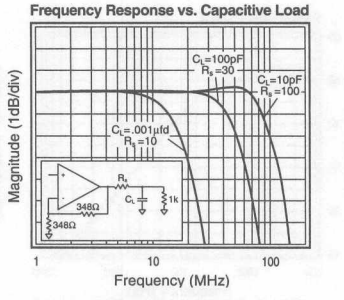
Frequency Response For Various R_Ls



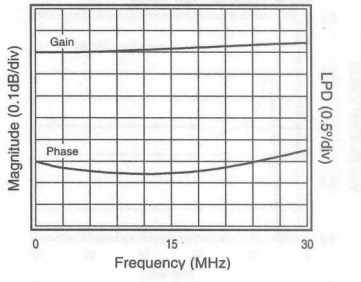
Frequency Response vs. V_{out}



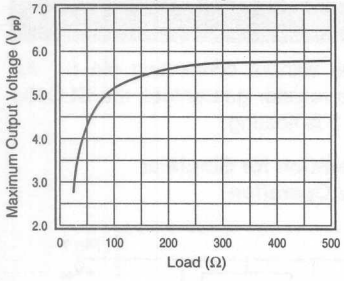
Frequency Response vs. Capacitive Load



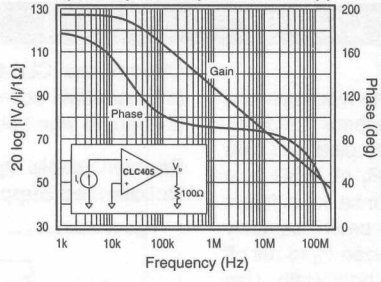
Gain Flatness & Linear Phase Deviation



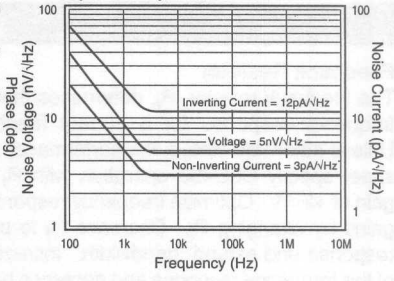
Maximum Output Voltage vs. R_L



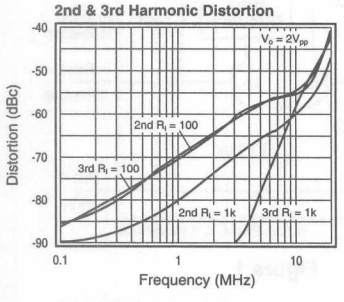
Open Loop Transimpedance Gain, Z(s)



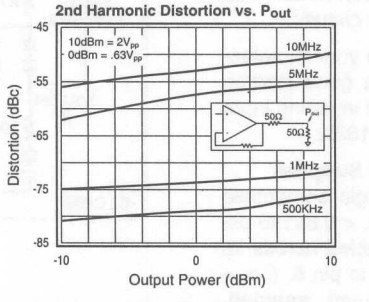
Equivalent Input Noise



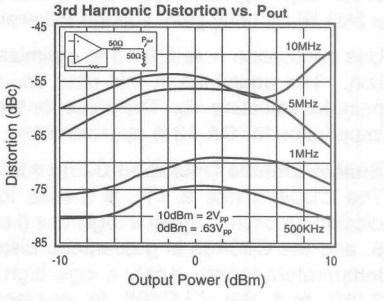
2nd & 3rd Harmonic Distortion



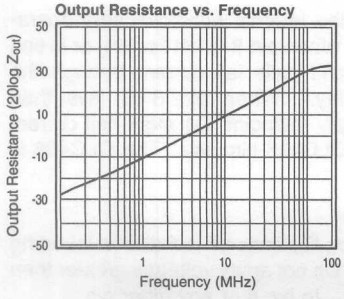
2nd Harmonic Distortion vs. P_{out}



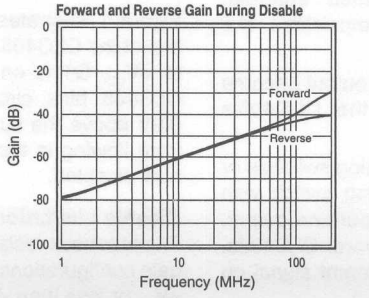
3rd Harmonic Distortion vs. P_{out}



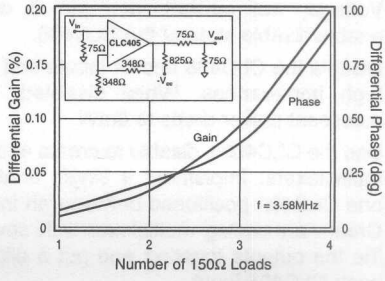
Output Resistance vs. Frequency



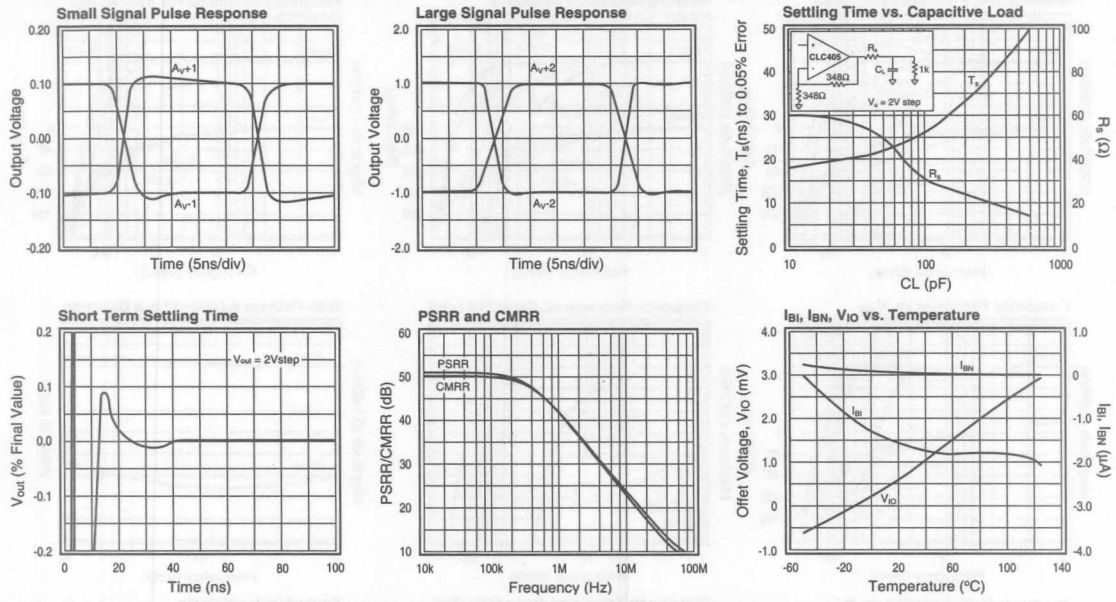
Forward and Reverse Gain During Disable



Differential Gain and Phase



CLC405 Typical Performance Characteristics (A_V = +2, R_f = 348Ω: V_{cc} = ± 5V, R_L = 100Ω unless specified)



CLC405 OPERATION

Feedback Resistor

The feedback resistor, R_f, determines the loop gain and frequency response for a current feedback amplifier. Unless otherwise stated, the performance plots and data sheet specify CLC405 operation with R_f of 348Ω at a gain of +2V/V. Optimize frequency response for different gains by changing R_f. Decrease R_f to peak frequency response and extend bandwidth. Increase R_f to roll off of the frequency response and decrease bandwidth. Use a 2kΩ R_f for unity gain, voltage follower circuits.

Use application note OA-13 to optimize your R_f selection. The equations in this note are a good starting point for selecting R_f. The value for the inverting input impedance for OA-13 is approximately 182Ω.

Enable/Disable Operation Using ±5V Supplies

The CLC405 has a TTL & CMOS logic compatible disable function. Apply a logic low (i.e. < 0.8V) to pin 8, and the CLC405 is guaranteed disabled across its temperature range. Apply a logic high to pin 8, (i.e. > 2.0V) and the CLC405 is guaranteed enabled. Voltage, not current, at pin 8 determines the enable/disable state of the CLC405.

Disable the CLC405 and its inputs and output become high impedances. While disabled, the CLC405's quiescent power drops to 8mW.

Use the CLC405's disable to create analog switches or multiplexers. Implement a single analog switch with one CLC405 positioned between an input and output. Create an analog multiplexer with several CLC405s. Tie the outputs together and put a different signal on each CLC405 input.

Operate the CLC405 without connecting pin 8. An internal 20kΩ pull-up resistor guarantees the CLC405 is enabled when pin 8 is floating.

Enable/Disable Operation for Single or Unbalanced Supply Operation

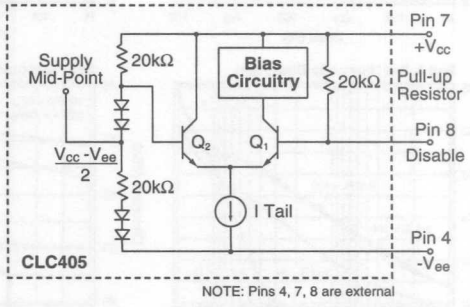


Figure 1

Figure 1 illustrates the internal enable/disable operation of the CLC405. When pin 8 is left floating or is tied to $+V_{cc}$, Q1 is on and pulls tail current through the CLC405 bias circuitry. When pin 8 is less than 0.8V above the supply midpoint, Q1 stops tail current from flowing in the CLC405 circuitry. The CLC405 is now disabled.

Disable Limitations

The feedback resistor, R_f, limits off isolation in inverting gain configurations. Do not apply voltages greater than $+V_{cc}$ or less than $-V_{ee}$ to pin 8 or any other pin.

Input - Bias Current, Impedances, and Source Termination Considerations

The CLC405 has:

- a 6MΩ non-inverting input impedance.
- a 100nA non-inverting input bias current.

If a large source impedance application is considered, remove all parasitic capacitance around the non-inverting input and source traces. Parasitic capacitances near the input and source act as a low-pass filter and reduce bandwidth.

Current feedback op amps have uncorrelated input bias currents. These uncorrelated bias currents prevent source impedance matching on each input from canceling offsets. Refer to application note OA-07 of the data book to find specific circuits to correct DC offsets.

Layout Considerations

Whenever questions about layout arise, USE THE EVALUATION BOARD AS A TEMPLATE.

Use the 730013 and 730027 evaluation boards for the DIP and SOIC respectively. These board layouts were optimized to produce the typical performance of the CLC405 shown in the data sheet. To reduce parasitic capacitances, the ground plane was removed near pins 2, 3, and 6. To reduce series inductance, trace lengths of components and nodes were minimized.

Parasitics on traces degrade performance. Minimize coupling from traces to both power and ground planes. Use low inductive resistors for leaded components.

Do not use dip sockets for the CLC405 DIP amplifiers. These sockets can peak the frequency domain response or create overshoot in the time domain response. Use flush-mount socket pins when socketing is necessary. The 730013 circuit board device holes are sized for Cambion P/N 450-2598 socket pins or their functional equivalent.

Insert the back matching resistor (R_{out}) shown in Figure 2 when driving coaxial cable or a capacitive load. Use the plot in the typical performance section labeled "Settling Time vs. Capacitive Load" to determine the optimum resistor value for $\mathbf{R_{out}}$ for different capacitive loads. This optimal resistance improves settling time for pulse-type applications and increases stability.

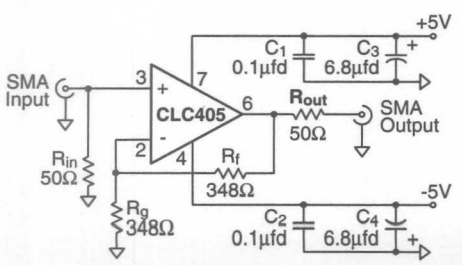
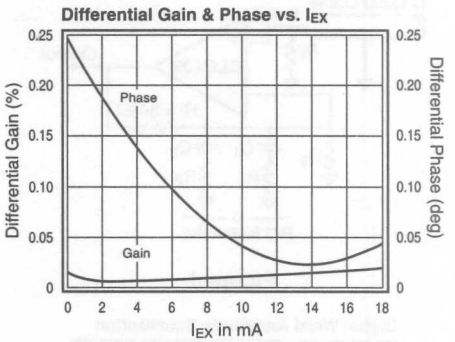


Figure 2

Use power-supply bypassing capacitors when operating this amplifier. Choose quality 0.1µF ceramics for C_1 and C_2. Choose quality 6.8µF tantalum capacitors for C_3 and C_4. Place the 0.1µF capacitors within 0.1 inches from the power pins. Place the 6.8µF capacitors within 3/4 inches from the power pins.

Video Performance vs. I_{EX}

Improve the video performance of the CLC405 by drawing extra current from the amplifier output stage. Using a single external resistor as shown in Figure 3, you can adjust the differential phase. Video performance vs. I_{EX} is illustrated below in Graph 1. This graph represents positive video performance with negative synchronization pulses.



Graph1

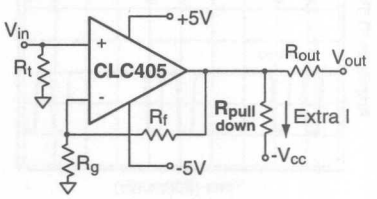


Figure 3

The value for R_{pd} in Figure 3 is determined by :

$$R_{pd} = \frac{5}{I_{EX}}$$

at ±5V supplies.

Wideband Digital PGA

As shown on the front page, the CLC405 is easily configured as a digitally controlled programmable gain amplifier. Make a PGA by configuring several amplifiers at required gains. Keep R_f near 348Ω and change R_g for each different gain. Use a TTL decoder that has enough outputs to control the selection of different gains and the buffer stage. Connect the buffer stage like the buffer of the front page. The buffer isolates each gain stage from the load and can produce a gain of zero for

a gain selection of zero. Use of an inverter (7404) on the buffer disable pin to keep the buffer operational at all gains except zero. Or float the buffer disable pin for a continuous enable state.

Amplitude Equalization

Sending signals over coaxial cable greater than 50 meters in length will attenuate high frequency signal components. Equalizers restore the attenuated components of this signal. The circuit in Figure 4, is an op amp equalizer. The RC networks peak the response of the CLC405 at higher frequencies. This peaking restores cable-attenuated frequencies. Graph 2 shows how the equalizer actually restored a digital word through 150 meters of coaxial cable.

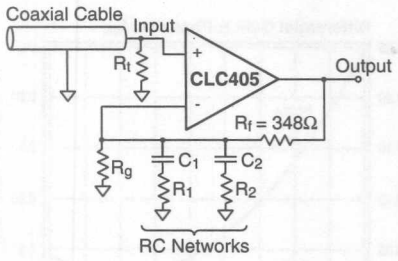
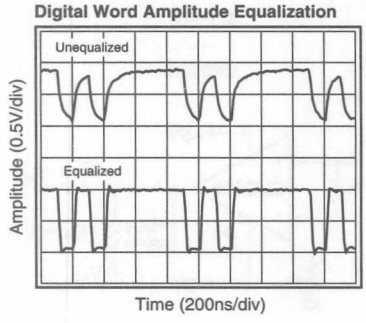


Figure 4



Graph 2

The values used to produce Graph 2 are:

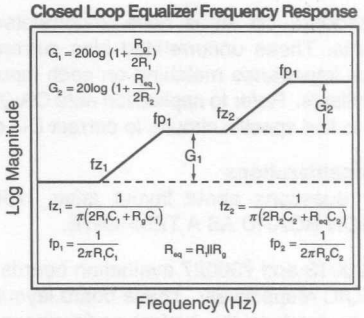
R_g = 348Ω C_1 = 470pF C_2 = 70pF

R_1 = 450Ω R_2 = 90Ω

Amplitude Equalizer

Place the first zero (fz_1) at some low frequency (540 khz for Graph 2). R_1 & C_1 produce a pole (fp_1 @ 750khz) that cancels fz_1. Place a second zero at a higher frequency (fz_2 @ 12Mhz). R_2 & C_2 provide a canceling pole (of fp_2 = 25Mhz).

Graph 3 shows the closed loop response of the op amp equalizer with equations for the poles, zeros, and gains.



Graph 3

Note: For very-high frequency equalization, use a higher bandwidth part (i.e. CLC44X)

Package Thermal Resistance

Package	θjc	θjA
Plastic (AJP)	75°/W	125°/W
Surface Mount (AJE)	130°/W	150°/W
CerDip	65°/W	155°/W

Ordering Information

Model	Temperature Range	Description
CLC405AJP	-40°C to +85°C	8-pin PDIP
CLC405AJE	-40°C to +85°C	8-pin SOIC
CLC405AIB*	-40°C to +85°C	8-pin CerDIP
CLC405ALC	-55°C to +125°C	dice
CLC405SMD*	-55°C to +125°C	8-pin CerDIP, MIL-STD-883
CLC405AMC	-55°C to +125°C	dice, MIL-STD-883

*See CLC405 MIL-883 Data Sheet for Specifications

Comlinear
A National Semiconductor Company

Low-Cost, Low-Power, Programmable Gain Buffer w/Disable

CLC407

APPLICATIONS:
- Desktop Video Systems
- Multiplexers
- Video Distribution
- Flash A/D Driver
- High-Speed Switch/Driver
- High-Source Impedance Applications
- Peak Detector Circuits
- Professional Video Processing
- High Resolution Monitors

FEATURES:
- Low-cost
- High output current: 60mA
- High input impedance: 6MΩ
- Gains of ±1, +2 with no external components
- Low power: Icc = 3.5mA
- Ultra-fast enable/disable times
- Very low input bias currents: 100nA
- Excellent gain accuracy: 0.1%
- High speed: 110MHz -3dB BW

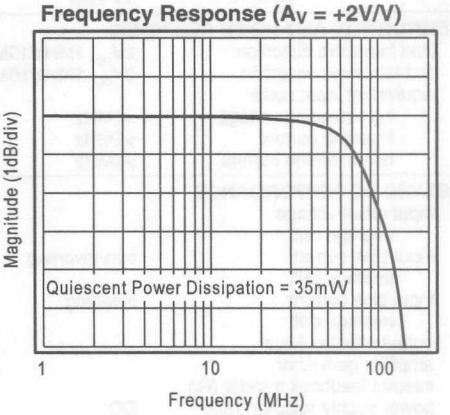
DESCRIPTION

The CLC407 is a low-cost, high-speed (110MHz) buffer which features user-programmable gains of +2, +1, and -1 V/V. This high-performance part has the added versatility of a TTL-compatible disable which quickly switches the buffer off in 18ns and back on in 40ns. The CLC407's high 60mA output current, coupled with its ultra-low 35mW power consumption makes it the ideal choice for demanding applications that are sensitive to both power and cost.

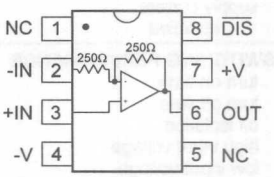
Utilizing Comlinear's proven architectures, this current feedback amplifier surpasses the performance of alternate solutions with a closed-loop design that produces new standards for buffers in gain accuracy, input impedance, and input bias currents. The CLC407's internal feedback network provides an excellent gain accuracy of 0.1%. High source impedance applications will benefit from the CLC407's 6MΩ input impedance along with its exceptionally low 100nA input bias current.

With 0.1dB flatness to 30MHz and low differential gain and phase errors, the CLC407 is very useful for professional video processing and distribution. A 110MHz -3dB bandwidth coupled with a 350V/µs slew rate also make the CLC407 a perfect choice in cost-sensitive applications such as video monitors, fax machines, copiers, and CATV systems. Back-terminated video applications will especially appreciate +2 gains which require no external gain components reducing inventory costs and board space.

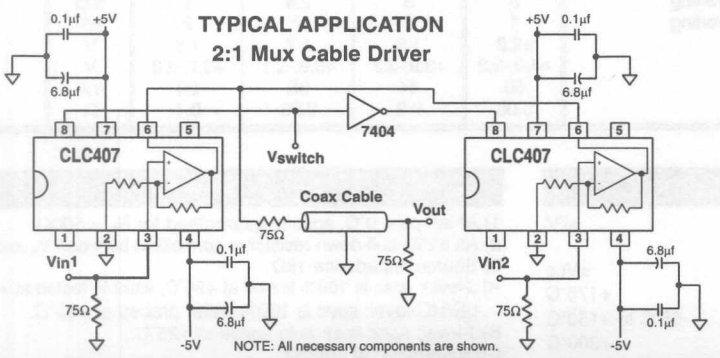
Frequency Response (A_V = +2V/V)



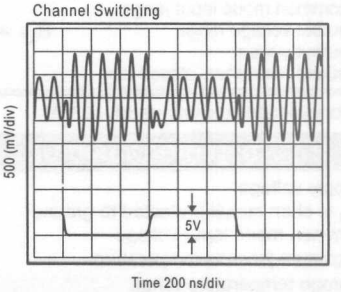
PINOUT
DIP & SOIC



TYPICAL APPLICATION
2:1 Mux Cable Driver



Channel Switching



CLC407 Electrical Characteristics (A_V = +2, V_{cc} = ± 5V, R_L = 100Ω unless specified)

PARAMETERS	CONDITIONS	TYP	GUARANTEED MIN/MAX			UNITS	NOTES
Ambient Temperature	CLC407AJ	+25°C	+25°C	0 to 70°C	-40 to 85°C		
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth	V_{out} < 1.0V_{pp}	110	75	50	45	MHz	B
	V_{out} < 5.0V_{pp}	42	31	27	26	MHz	1
±0.1dB bandwidth	V_{out} < 1.0V_{pp}	30	15			MHz	
gain flatness	V_{out} < 1.0V_{pp}						
peaking	DC to 200MHz	0	0.4	0.6	0.8	dB	B
rolloff	<30MHz	0.1	0.5	0.65	0.7	dB	B
linear phase deviation	<20MHz	0.3	0.6	0.7	0.7	deg	
differential gain	NTSC, RL=150Ω	0.03	0.05	0.06	0.07	%	
	NTSC, RL=150Ω (Note 2)	0.01				%	2
differential phase	NTSC, RL=150Ω	0.25	0.4	0.5	0.55	deg	
	NTSC, RL=150Ω (Note 2)	0.08				deg	2
TIME DOMAIN RESPONSE							
rise and fall time	2V step	5	7.5	8.2	8.4	ns	
settling time to 0.05%	2V step	18	27	36	39	ns	
overshoot	2V step	3	12	12	12	%	
slew rate AV = +2	2V step	350	260	225	215	V/µs	
AV = -1	1V step	650				V/µs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 1MHz/10MHz	-72/-52	-46	-45	-44	dBc	B, C
3rd harmonic distortion	2V_{pp}, 1MHz/10MHz	-70/-57	-50	-47	-46	dBc	B, C
equivalent input noise							
non-inverting voltage	>1MHz	5	6.3	6.6	6.7	nV/√Hz	
inverting current	>1MHz	12	15	16	17	pA/√Hz	
non-inverting current	>1MHz	3	3.8	4	4.2	pA/√Hz	
STATIC DC PERFORMANCE							
input offset voltage		1	5	7	8	mV	
average drift		30		50	50	µV/°C	
input bias current	non-inverting	100	600	800	1300	nA	A
average drift		3		8	11	nA/°C	
input bias current	inverting	1	5	6	8	µA	
average drift		17		40	45	nA/°C	
output offset voltage		2.5	13	17	19	mV	A,3
amplifier gain error		±0.1%	±1.0%	±1.0%	±1.0%	V/V	A
internal feedback resistor (R_f)		250	±20%			Ω	
power supply rejection ratio	DC	52	47	46	45	dB	B
common-mode rejection ratio	DC	50	45	44	43	dB	
supply current	R_L= ∞	3.5	3.9	4	4.3	mA	A
disabled	R_L= ∞	0.8	0.9	0.95	1	mA	A
SWITCHING PERFORMANCE							
turn on time		40	55	58	58	ns	
turn off time	to >50dB attn. @ 10MHz	18	26	30	32	ns	
off isolation	10MHz	85	80	80	80	dB	
high input voltage	V_{IH}		2	2	2	V	
low input voltage	V_{IL}		0.8	0.8	0.8	V	
MISCELLANEOUS PERFORMANCE							
input resistance	non-inverting	6	3	2.4	1	MΩ	
input capacitance	non-inverting	1	2	2	2	pF	
common mode input range		±2.2	1.8	1.7	1.5	V	
output voltage range	R_L= ∞	+4.0,-3.3	+3.9,-3.2	+3.8,-3.1	+3.7,-2.8	V	
output current		60	44	38	20	mA	
output resistance, closed loop		0.06	0.2	0.25	0.4	Ω	

Recommended gain range ±1, +2 V/V

Absolute Maximum Ratings

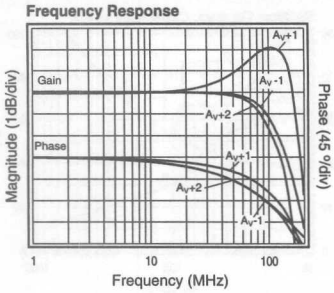
supply voltage	±7V
I_{out} is short circuit protected to ground	
common-mode input voltage	±Vcc
maximum junction temperature	+175°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

Notes

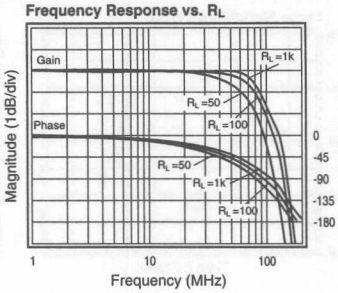
1) At temps < 0°C, spec is guaranteed for R_L = 500Ω.
2) An 825Ω pull-down resistor is connected between V_o and -V_{cc}.
3) Source impedance 1kΩ.
A) J-level: spec is 100% tested at +25°C, sample tested at +85°C.
LC/MC-level: spec is 100% wafer probed at +25°C.
B) J-level: spec is sample tested at +25°C.
C) Guaranteed at 10MHz.

CLC407 Typical Performance Characteristics (A_V = +2, R_f = 250Ω: V_{cc} = ± 5V, R_L = 100Ω unless specified)

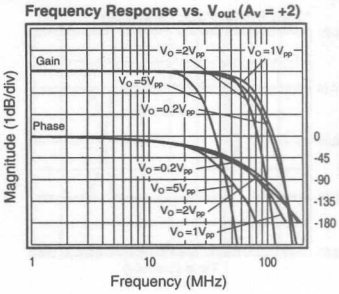
Frequency Response



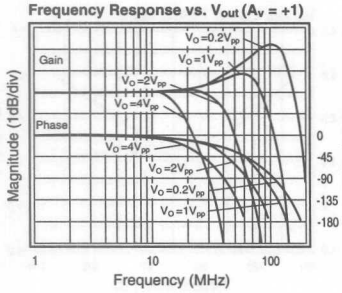
Frequency Response vs. R_L



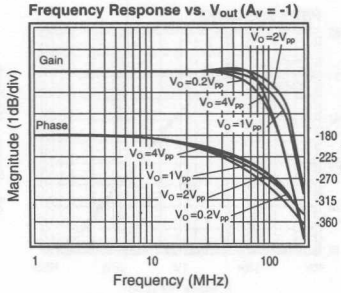
Frequency Response vs. V_{out} (A_V = +2)



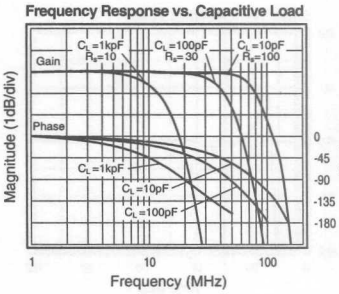
Frequency Response vs. V_{out} (A_V = +1)



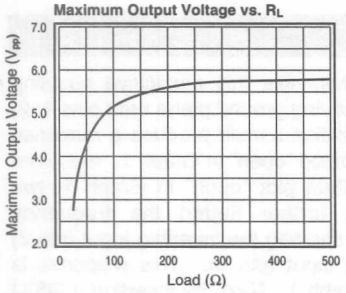
Frequency Response vs. V_{out} (A_V = -1)



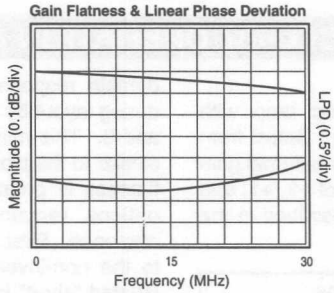
Frequency Response vs. Capacitive Load



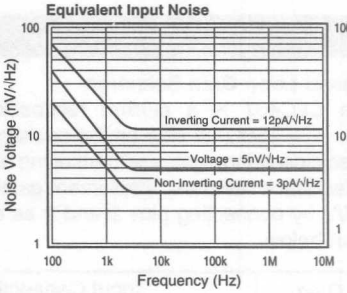
Maximum Output Voltage vs. R_L



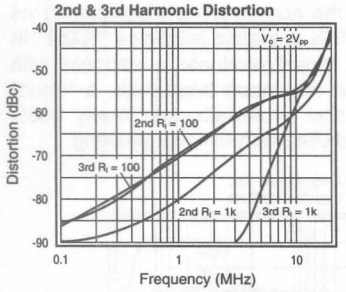
Gain Flatness & Linear Phase Deviation



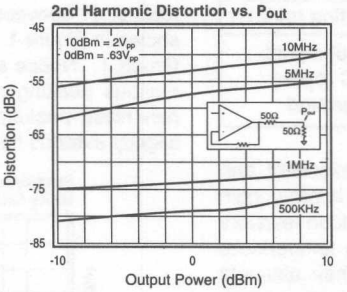
Equivalent Input Noise



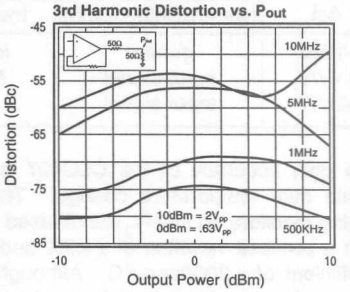
2nd & 3rd Harmonic Distortion



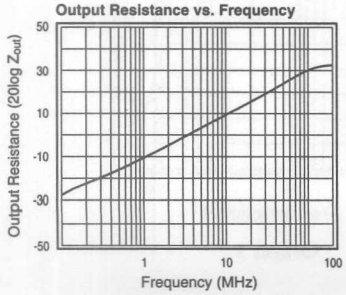
2nd Harmonic Distortion vs. P_{out}



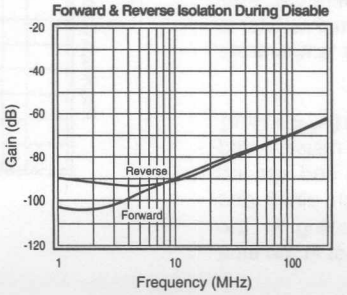
3rd Harmonic Distortion vs. P_{out}



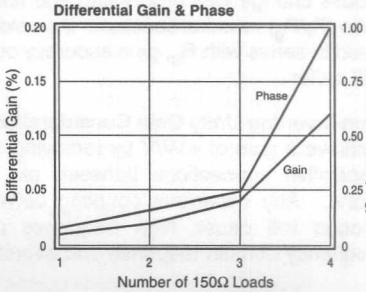
Output Resistance vs. Frequency



Forward & Reverse Isolation During Disable

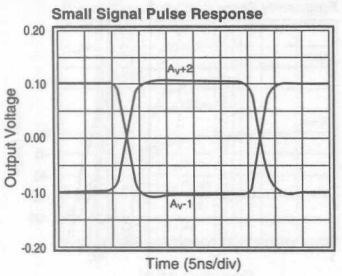


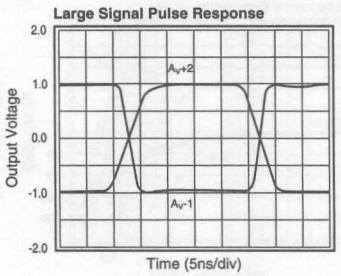
Differential Gain & Phase

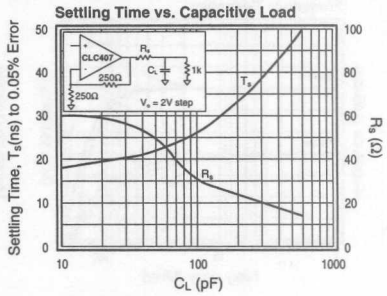


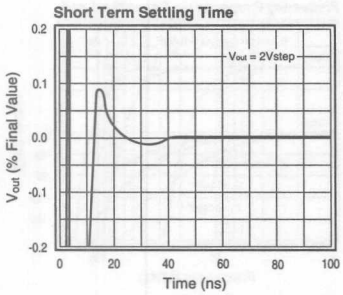
3

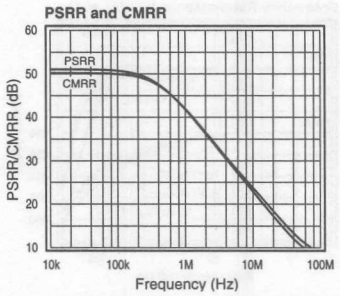
CLC407 Typical Performance Characteristics (A_V = +2, R_f = 250Ω: V_{cc} = ± 5V, R_L = 100Ω unless specified)

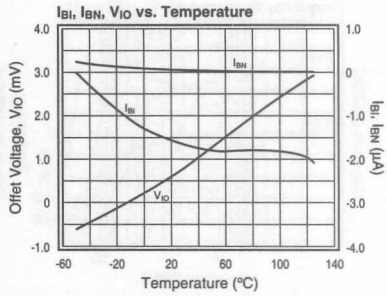












CLC407 OPERATION

Closed Loop Gain Selection

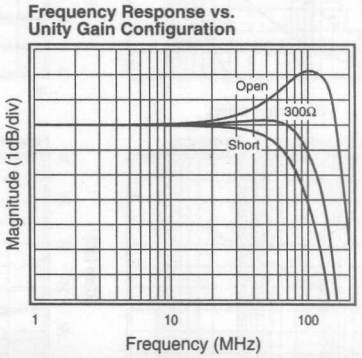
The CLC407 is a current feedback op amp with $R_f = R_g = 250\Omega$ on chip (in the package). Select from three closed loop gains without using any external gain or feedback resistors. Implement gains of +2, +1, and -1V/V by connecting pins 2 and 3 as described in the chart below.

Gain Acl	Input Connections	
	Non-Inverting (pin3)	Inverting (pin2)
-1V/V	ground	input signal
+1V/V	input signal	NC (open)
+2V/V	input signal	ground

The gain accuracy of the CLC407 is excellent and stable over temperature change. The internal gain setting resistors, R_f and R_g are diffused silicon resistors with a process variation of ± 20% and a temperature coefficient of ~ 2000ppm/°C. Although their absolute values change with processing and temperature, their ratio (R_f/R_g) remains constant. If an external resistor is used in series with R_g, gain accuracy over temperature will suffer .

Non-Inverting Unity Gain Considerations (A_v = +1V/V)

Achieve a gain of +1V/V by removing all resistive and capacitive connections between pin 2 and ground plane. Any capacitive coupling between pin 2 and ground will cause high frequency peaking in the frequency domain response and overshoot in the time domain response. Minimize this capacitive coupling during layout by removing ground plane near pins 1, 2, and 3. This minimization should produce a response similar to the plot labeled "open" in Graph 1. If desired flatness is greater than plot "open" in Graph 1, two options remain to further flatten the frequency response. First, try shorting the inverting input (pin 2) to the non-inverting input (pin 3). This response is labeled "short" in Graph 1. Next, try inserting a 300Ω resistor **R** between the non-inverting input (pin 2) as shown in Figure 1. This response is labeled "300Ω " in Graph 1. Notice an "open" produces a response with obvious peaking and maximum bandwidth, a "short" minimizes peaking and bandwidth, and finally 300Ω slightly extends bandwidth with minimal peaking.



Graph 1

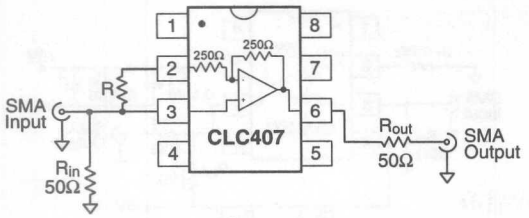


Figure 1

Enable/Disable Operation Using ±5V Supplies

The CLC407 has a TTL & CMOS logic compatible disable function. Apply a logic low (i.e. < 0.8V) to pin 8, and the CLC407 is guaranteed disabled across its temperature range. Apply a logic high to pin 8, (i.e. > 2.0V) and the CLC407 is guaranteed enabled. Voltage, not current, at pin 8 determines the enable/disable state of the CLC407.

Disable the CLC407 and its inputs and output become high impedances. While disabled, the CLC407's quiescent power drops to 8mW.

Use the CLC407's disable to create analog switches or multiplexers. Implement a single analog switch with one CLC407 positioned between an input and output. Create an analog multiplexer with several CLC407s. Tie the outputs together and put a different signal on each CLC407 input.

Operate the CLC407 without connecting pin 8. An internal 20kΩ pull-up resistor guarantees the CLC407 is enabled when pin 8 is floating.

Enable/Disable Operation for Single or Unbalanced Supply Operation

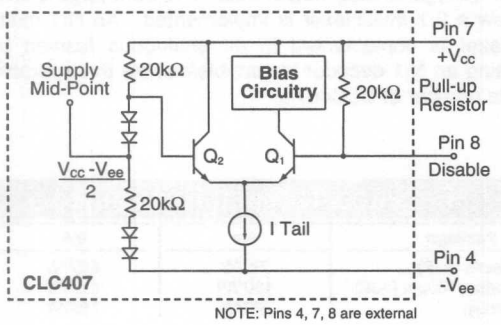


Figure 2

Figure 2 illustrates the internal enable/disable operation of the CLC407. When pin 8 is left floating or is tied to $+V_{cc}$, Q_1 is on and pulls tail current through the CLC407 circuitry. When pin 8 is less than 0.8V above the supply mid-point, Q_1 stops tail current from flowing in the bias circuitry. The CLC407 is now disabled.

Disable Limitations

The internal feedback resistor, R_f limits off isolation in inverting gain configurations. Do not apply voltages greater than $+V_{cc}$ or less than $-V_{ee}$ to pin 8.

Input - Bias Current, Impedances, and Source Termination Considerations

The CLC407 has:

- a 6MΩ non-inverting input impedance.
- 100nA non-inverting input bias current.

If a large source impedance application is considered, remove all parasitic capacitance around the non-inverting input and source traces. Parasitic capacitances near the input and source act as a low-pass filter and reduce bandwidth.

Current feedback op amps have uncorrelated input bias currents. These uncorrelated bias currents prevent source impedance matching on each input from cancelling offsets. Refer to application note OA-07 of the data book to find specific circuits to correct DC offsets.

Layout Considerations

Whenever questions about layout arise, USE THE EVALUATION BOARD AS A TEMPLATE.

Use the 730013 and 730026 evaluation boards for the DIP and SOIC respectively. These board layouts were optimized to produce the typical performance of the CLC407 shown in the data sheet. To reduce parasitic capacitances, the ground plane was removed near pins 2, 3, and 6. To reduce series inductance, trace lengths of components and nodes were minimized.

Parasitics on traces degrade performance. Minimize coupling from traces to both power and ground planes. Use low inductance resistors for leaded components .

Do not use dip sockets for the CLC407 DIP amplifiers. These sockets can peak the frequency domain response or create overshoot in the time domain response. Use flush-mount socket pins if socketing cannot be avoided. The 730013 circuit board device holes are sized for Cambion P/N 450-2598 socket pins or their functional equivalent.

Insert the back matching resistor $\mathbf{R_{out}}$ shown in Figure 3 when driving coaxial cable or a capacitive load. Use the plot in the typical performance section labeled "Settling Time vs. Capacitive Load" to determine the optimum resistor value for R_{out} for different capacitive loads. This optimal resistance improves settling time for pulse-type applications and increases stability.

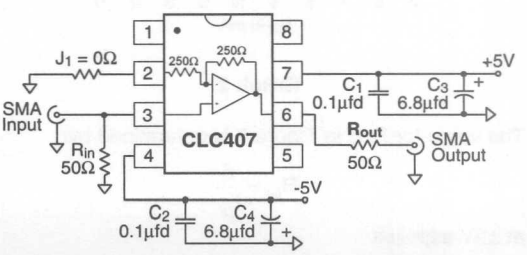


Figure 3

Use power-supply bypassing capacitors when operating this amplifier. Choose quality 0.1µF ceramics for C_1 and C_2. Choose quality 6.8µF tantalum capacitors for C_3 and C_4. Place the 0.1µF capacitors within 0.1 inches from the power pins. Place the 6.8µF capacitors within 3/4 inches from the power pins.

Special Evaluation Board Considerations for the CLC407

To optimize off-isolation of the CLC407, cut the R_f trace on both the 730013 and the 730026 evaluation boards. This cut minimizes capacitive feedthrough between the input and the output. Figure 4 shows where to cut both evaluation boards for improved off-isolation.

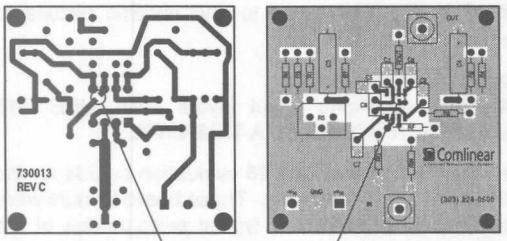
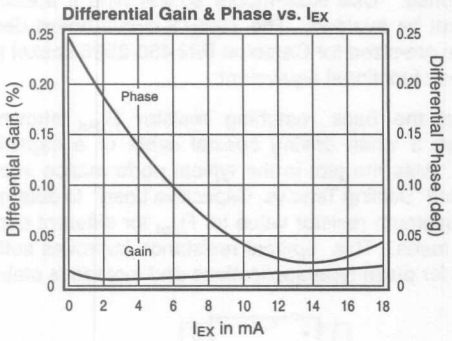


Figure 4

Video Performance vs. I_{EX}

Improve the video performance of the CLC407 by drawing extra current from the amplifier's output stage. Using a single external resistor as shown in Figure 5, you can adjust the differential phase. Video performance vs. I_{EX} is illustrated below in Graph 2. This graph represents positive video performance with negative synchronization pulses.



Graph 2

The value for Rpd in Figure 5 is determined by:

$$R_{pd} = \frac{5}{I_{EX}}$$

at ±5V supplies.

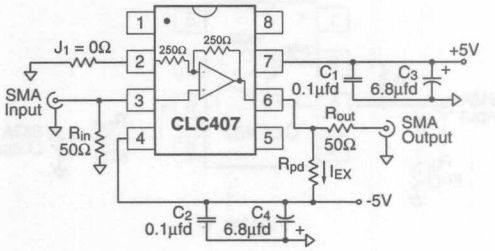


Figure 5

Video Cable Driver

The CLC407 was designed to produce exceptional video performance at all three closed-loop gains. At the non-inverting gain of 2V/V configuration, back terminate the cable using R_{out}. A typical cable driving configuration is shown below in Figure 6.

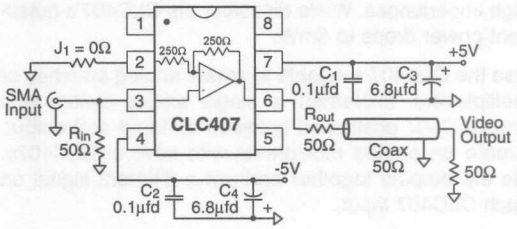


Figure 6

N:1 Mux Cable Driver

The CLC407 is capable of multiplexing several signals on a single analog output bus. The front page shows how a 2:1 multiplexer is implemented. An N:1 multiplexer is implemented in an analogous fashion by using an N:1 decoder to enable/disable the appropriate number of CLC407's.

Package Thermal Resistance

Package	θjc	θjA
Plastic (AJP)	75°/W	125°/W
Surface Mount (AJE)	130°/W	150°/W
CerDip	65°/W	155°/W

Ordering Information

Model	Temperature Range	Description
CLC407AJP	-40°C to +85°C	8-pin PDIP
CLC407AJE	-40°C to +85°C	8-pin SOIC
CLC407AIB*	-40°C to +85°C	8-pin CerDIP
CLC407ALC	-55°C to +125°C	dice
CLC407SMD*	-55°C to +125°C	8-pin CerDIP, MIL-STD-883
CLC407AMC	-55°C to +125°C	dice, MIL-STD-883

*See CLC407 MIL-883 Data Sheet for Specifications

Comlinear
A National Semiconductor Company

High-Speed Video Op Amp with Disable

CLC411

APPLICATIONS:

- HDTV amplifier
- video line driver
- high-speed analog bus driver
- video signal multiplexer
- DAC output buffer

FEATURES (typical):

- 200MHz small signal bandwidth ($1V_{pp}$)
- ±0.05dB gain flatness to 30MHz
- 0.02%, 0.03° differential gain, phase
- 2300V/µs slew rate
- 10ns disable to high-impedance output
- 70mA continuous output current
- ±4.5V output swing into 100Ω load
- ±4.0V input voltage range

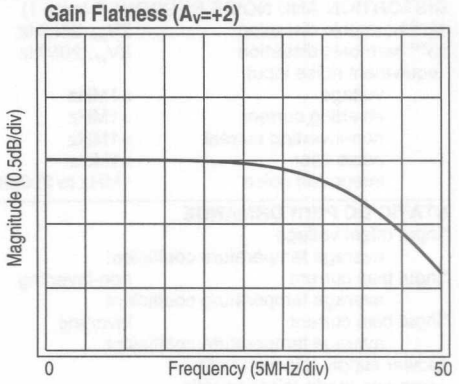
DESCRIPTION

The CLC411 combines a state-of-the-art complementary bipolar process with Comlinear's patented current-feedback architecture to provide a very high-speed op amp operating from ±15V supplies. Drawing only 11mA quiescent current, the CLC411 provides a 200MHz small signal bandwidth and a 2300V/µs slew rate while delivering a continuous 70mA current output with ±4.5V output swing. The CLC411's high-speed performance includes a 15ns settling time to 0.1% (2V step) and a 2.3ns rise and fall time (6V step).

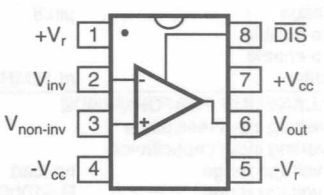
The CLC411 is designed to meet the requirements of professional broadcast video systems including composite video and high definition television. The CLC411 exceeds the HDTV standard for gain flatness to 30MHz with it's ±0.05dB flat frequency response and exceeds composite video standards with its very low differential gain and phase errors of 0.02%, 0.03°. The CLC411 is the op amp of choice for all video systems requiring upward compatibility from NTSC and PAL to HDTV.

The CLC411 features a very fast disable/enable (10ns/ 55ns) allowing the multiplexing of high-speed signals onto an analog bus through the common output connections of multiple CLC411's. Using the same signal source to drive disable/enable pins is easy since "break-before-make" is guaranteed.

Gain Flatness (A_V=+2)



Pinout
DIP & SOIC

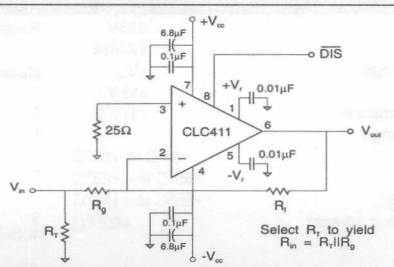


The CLC411 is available in several versions.

CLC411AJP	-40°C to +85°C	8-pin plastic DIP
CLC411AJE	-40°C to +85°C	8-pin plastic SOIC
CLC411AIB	-40°C to +85°C	8-pin hermetic CERDIP
CLC411A8B	-55°C to +125°C	8-pin hermetic CERDIP, MIL-STD-883
CLC411ALC	-55°C to +125°C	dice
CLC411AMC	-55°C to +125°C	dice, MIL-STD-883, Level B

Contact factory for other packages and DESC SMD number.

Recommended Inverting Gain Configuration



CLC411 Electrical Characteristics (A_V = +2; V_{CC} = ±15V; R_L = 100Ω; R_f = 301Ω, unless noted)

PARAMETERS	CONDITIONS	TYP	MIN AND MAX RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC411 AJ/AI	+25°C	-40°C	+25°C	+85°C		
Ambient Temperature	CLC411 A8/AM/AL	+25°C	-55°C	+25°C	+125°C		
FREQUENCY DOMAIN RESPONSE							
†-3dB bandwidth	V_{out} < $1V_{pp}$	200	150	150	110	MHz	SSBW
	V_{out} < $6V_{pp}$	75	50	50	40	MHz	LSBW
gain flatness	V_{out} < $1V_{pp}$						
†peaking	DC to 30MHz	0.05				dB	GFPL
†rolloff DC to 30MHz	0.05				dB	GFRL	
†peaking	DC to 200MHz	0.1	0.6	0.5	0.6	dB	GFPH
†rolloff DC to 60MHz	0.2	0.5	0.4	0.5	dB	GFRH	
linear phase deviation	DC to 60MHz	0.3	1.0	1.0	1.0	°	LPD
differential gain	4.43MHz, R_L=150Ω	0.02				%	DG
differential phase	4.43MHz, R_L=150Ω	0.03				°	DP
TIME DOMAIN RESPONSE							
rise and fall time	6V step	2.3				ns	TR
settling time to 0.1%	2V step	15	23	18	23	ns	TS
overshoot	2V step	5	15	10	15	%	OS
slew rate	6V step	2300				V/µs	SR
DISTORTION AND NOISE RESPONSE (note 1)							
†2ND harmonic distortion	$2V_{pp}$, 20MHz	-48				dBc	HD2
†3RD harmonic distortion	$2V_{pp}$, 20MHz	-52				dBc	HD3
equivalent noise input							
voltage	>1MHz	2.5				nV/√Hz	VN
inverting current	>1MHz	12.9				pA/√Hz	ICI
non-inverting current	>1MHz	6.3				pA/√Hz	ICN
noise floor	>1MHz	-157				dBm_{1Hz}	SNF
integrated noise	1MHz to 200MHz	45				µV	INV
STATIC DC PERFORMANCE							
*input offset voltage		±2	±13	±9.0	±14	mV	VIO
average temperature coefficient		+30	±50	—	±50	µV/°C	DVIO
*input bias current	non-inverting	12	65	30	±20	µA	IBN
average temperature coefficient		±200	±400	—	±250	nA/°C	DIBN
*input bias current	inverting	±12	±40	±30	±30	µA	IBI
average temperature coefficient		±50	±200	—	±150	nA/°C	DIBI
†power supply rejection ratio		56	48	50	48	dB	PSRR
♠common mode rejection ratio		52	44	46	44	dB	CMRR
*supply current	no load	11	14	12	12	mA	ICC
supply current	disabled	2.5	4.5	3.5	4.5	mA	ICCD
DISABLE/ENABLE PERFORMANCE (note 2)							
disable time	to >50dB attenuation @10MHz	10	30	30	60	ns	TOFF
enable time		55				ns	TON
DIS voltage	pin 8						
to disable		4.5	<3.0	<3.0	<3.0	V	VDIS
to enable		5.5	>7.0	>6.5	>6.5	V	VEN
off isolation	at 10MHz	59	55	55	55	dB	OSD
MISCELLANEOUS PERFORMANCE							
non-inverting input resistance		1000	250	750	1000	kΩ	RIN
non-inverting input capacitance		2.0	3.0	3.0	3.0	pF	CIN
output voltage range	no load	±6.0		±4.5		V	VO
output voltage range	R_L=100Ω	±4.5		±4.0		V	VOL
common mode input range		±4.0		±3.5		V	CMIR
output current		70	30	50	40	mA	IO

Absolute Maximum Ratings

V_{cc}	±18V
I_{out}	125mA
common-mode input voltage	±V_{cc}
differential input voltage	±15V
maximum junction temperature	+175°C
operating temperature range	
AJ/AI	-40°C to +85°C
A8/AM/AL:	-55°C to +125°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

Miscellaneous Ratings

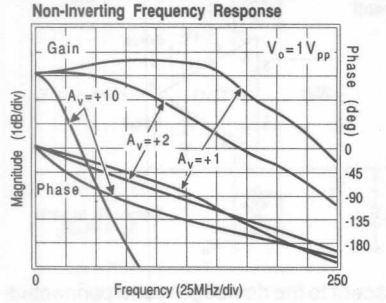
Recommended gain range ±1 to ±10V/V

Notes:

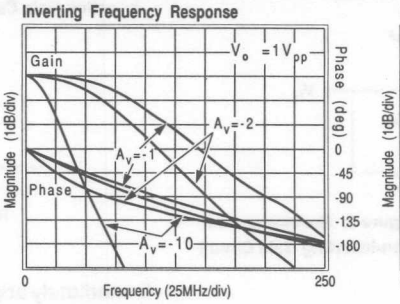
* AJ,AI : 100% tested at +25°C, sample at +85°C.
† AJ : Sample tested at +25°C.
† AI : 100% tested at +25°C.
* A8 : 100% tested at +25°C, -55°C, +125°C.
† A8 : 100% tested at +25°C, sample at -55°C, +125°C
* AL, AM : 100% wafer probed +25°C to +25°C min/max specs.
♠ SMD : Sample tested at +25°C, -55°C and +125°C.
note 1) : Specifications guaranteed using 0.01µF bypass capacitors on pins 1 & 5.
note 2) : Break before make is guaranteed.

CLC411 Typical Performance (T_A=+25 C, A_V=+2, V_{CC}=±15V, R_L=100Ω, R_f=301Ω, unless noted)

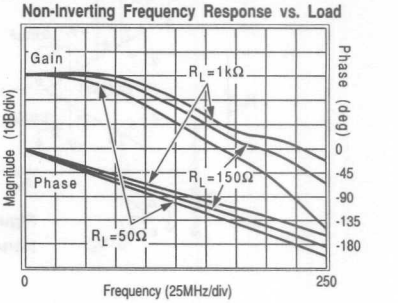
Non-Inverting Frequency Response



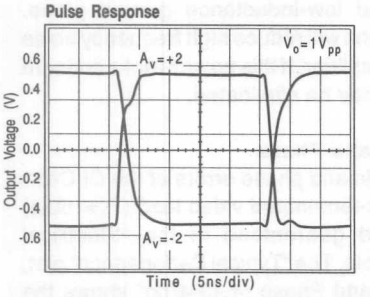
Inverting Frequency Response



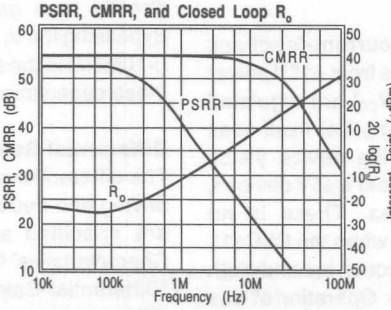
Non-Inverting Frequency Response vs. Load



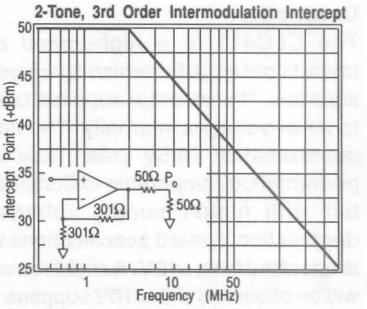
Pulse Response



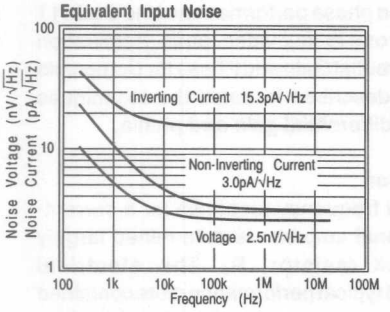
PSRR, CMRR, and Closed Loop R_o



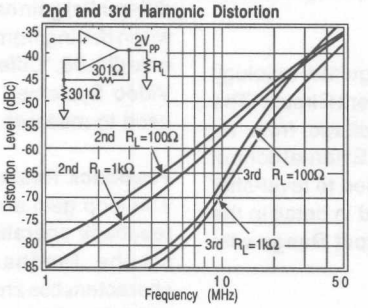
2-Tone, 3rd Order Intermodulation Intercept



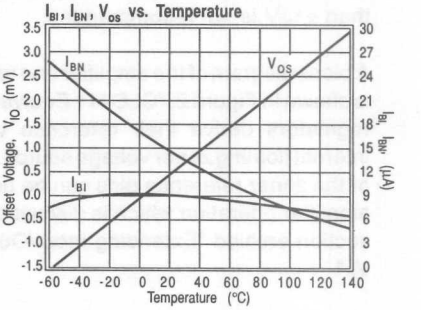
Equivalent Input Noise



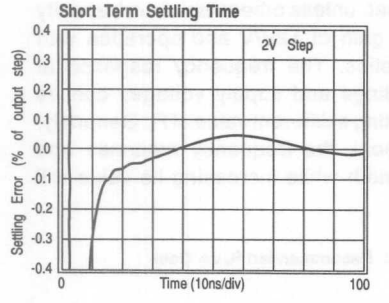
2nd and 3rd Harmonic Distortion



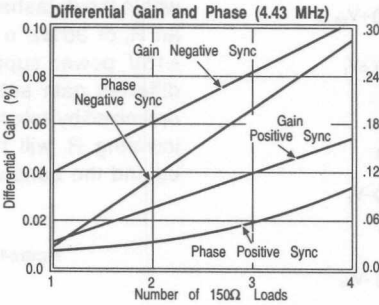
I_{BI}, I_{BN}, V_{OS} vs. Temperature



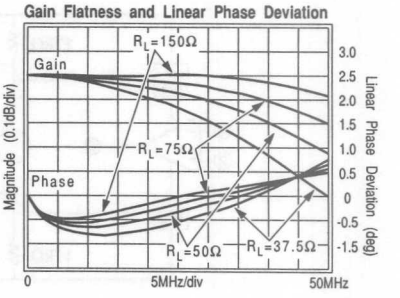
Short Term Settling Time



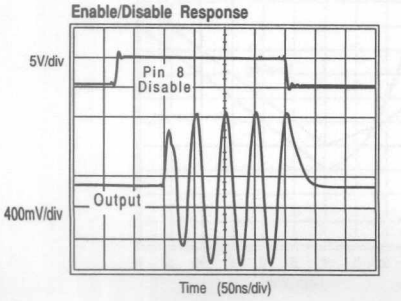
Differential Gain and Phase (4.43 MHz)



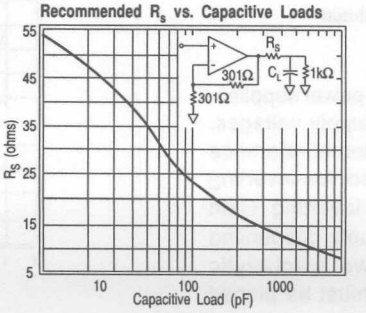
Gain Flatness and Linear Phase Deviation



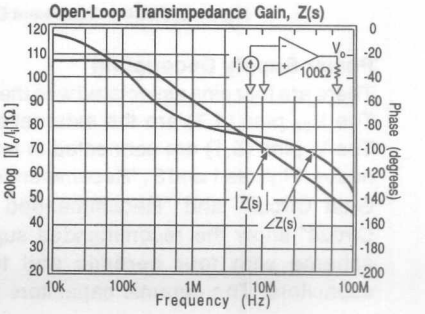
Enable/Disable Response



Recommended R_s vs. Capacitive Loads



Open-Loop Transimpedance Gain, Z(s)



3

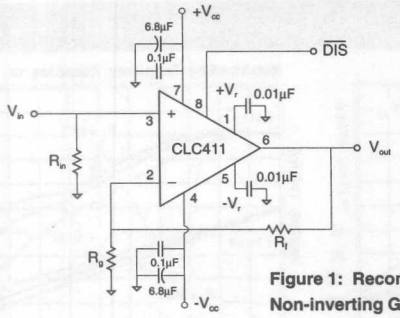


Figure 1: Recommended Non-inverting Gain Circuit

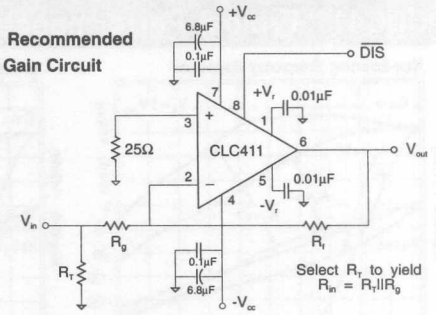


Figure 3: Recommended Inverting Gain Circuit

Description

The CLC411 is a high-speed current-feedback operational amplifier which operates from ±15V power supplies. The external supplies ($\pm V_{CC}$) are regulated to lower voltages internally. The amplifier itself sees approximately ±6.5V rails. Thus the device yields performance comparable to Comlinear's ±5V devices, but with higher supply voltages. There is no degradation in rated specifications when the CLC411 is operated from ±12V. A slight reduction in bandwidth will be observed with ±10V supplies. Operation at less than ±10V is not recommended.

A block diagram of the amplifier and regulator topology is shown in Figure 2, "CLC411 Equivalent Circuit." The regulators derive their reference voltage from an internal floating zener voltage source. External control of the zener reference pins can be used to level-shift amplifier operation which is discussed in detail in the section entitled "Extending Input/Output Range with V_r."

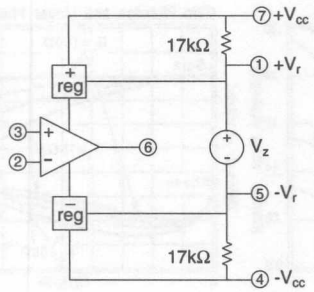


Figure 2: CLC411 Equivalent Circuit

Power Supply Decoupling

There are four pins associated with the power supplies. The V_{CC} pins (4,7) are the external supply voltages. The V_r pins (5,1) are connected to internal reference nodes. Figures 1 and 3, "Recommended Non-inverting Gain Circuit" and "Recommended Inverting Gain Circuit" show the recommended supply decoupling scheme with four ceramic and two electrolytic capacitors. The ceramic capacitors must be placed immediately adjacent to the device pins and connected directly to a good low-inductance ground plane. Bypassing the V_r pins will reduce high frequency noise (>10MHz) in the amplifier. If this noise is not a concern these capacitors may be eliminated.

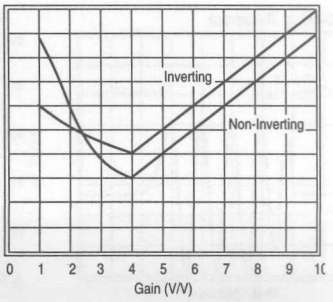
Differential Gain and Phase

The differential gain and phase errors of the CLC411 driving one doubly-terminated video load (R_L=150Ω) are specified and guaranteed in the "Electrical Characteristics" table. The "Typical Performance" plot, "Differential Gain and Phase (4.43MHz)" shows the differential gain and phase performance of the CLC411 when driving from one to four video loads. Application note OA-08, "Differential Gain and Phase for Composite Video Systems," describes in detail the techniques used to measure differential gain and phase.

Feedback Resistor

The loop gain and frequency response for a current-feedback operational amplifier is determined largely by the feedback resistor, R_f. The electrical characteristics and typical performance plots contained within the datasheet, unless otherwise stated, specify an R_f of 301Ω, a gain of +2V/V and operation with ±15V power supplies. The frequency response at different gain settings and supply voltages can be optimized by selecting a different value of R_f. Generally, lowering R_f will peak the frequency response and extend the bandwidth while increasing its value will

Figure4: Recommended R_f vs. Gain



roll off the response. For unity-gain voltage follower circuits, a non-zero R_f must be used with current-feedback operational amplifiers such as the CLC411. Application note OA-13, "Current-Feedback Loop-Gain Analysis and Performance Enhancements," explains the ramifications of R_f and how to use it to tailor the desired frequency response with respect to gain. The equations found in the application note should be considered as a starting point for the selection of R_f. The equations do not factor in the effects of parasitic capacitance found on the inverting input, the output nor across the feedback resistor. Equations in OA-13 require values for R_f (301Ω), Av (+2) and R_i (inverting input resistance, 50Ω). Combining these values yields a Z_t* (optimum feedback transimpedance) of 400Ω. Figure 4 entitled "Recommended R_f vs. Gain" will enable the selection of the feedback resistor that provides a maximally flat frequency response for the CLC411 over its gain range. The linear portion of the two curves (i.e. A_V>4) results from the limitation on R_g (i.e. R_g ≥50Ω).

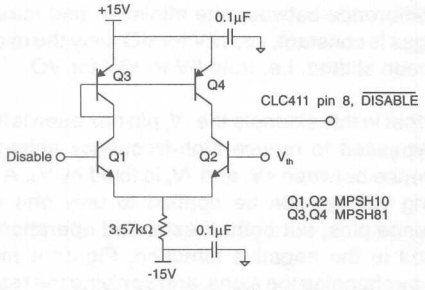


Figure 5A: Disable Interface

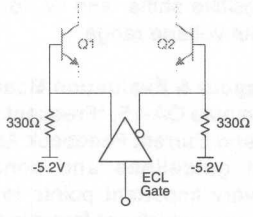


Figure 5B: Differential ECL Interface

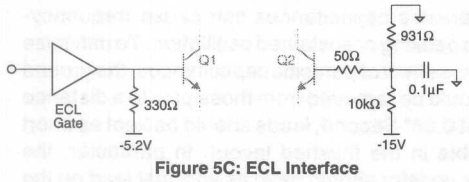


Figure 5C: ECL Interface

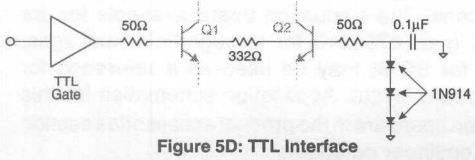


Figure 5D: TTL Interface

Enable/Disable Operation

The disable feature allows the outputs of several CLC411 devices to be connected onto a common analog bus forming a high-speed analog multiplexer. When disabled, the output and inverting inputs of the CLC411 become high impedances. The disable pin has an internal pull-up resistor which is pulled-up to an internal voltage, not to the external supply. The CLC411 is enabled when pin 8 is left open or pulled-up to ≥+7V and disabled when grounded or pulled below +3V. CMOS logic devices are necessary to drive the disable pin. For example, CMOS logic with V_{DD} ≥ +7V will guarantee proper operation over temperature. TTL voltage levels are inadequate for controlling the disable feature.

For faster enable/disable operation than 15V CMOS logic devices will allow, the circuit of Figure 5 is recommended. A fast four-transistor comparator, Figure 5A, interfaces between the CLC411 DISABLE pin and several standard logic families. This circuit has a differential input between the bases of Q1 and Q2. As such it may be driven directly from differential

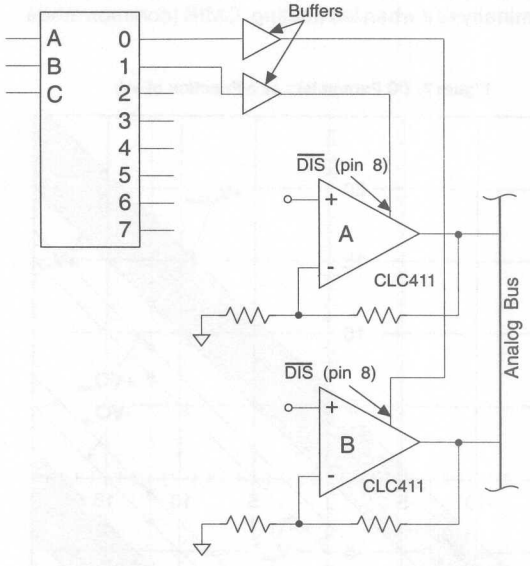


Figure 6: General Multiplexing Circuit

ECL logic, as in shown in Figure 5B. Single-ended logic families may also be used by establishing an appropriate threshold voltage on the V_{th} input, the base of Q2. Figures 5C and 5D illustrate a single-ended ECL and TTL interface respectively. The Disable input, the base of Q1, is driven above and below the threshold, V_{th}.

Fastest switching speeds result when the differential voltage between the bases of Q1 and Q2 is kept to less than one volt. Single-ended ECL, Figure 5C, maintains this desired maximum differential input voltage. TTL and CMOS have higher V_{high} to V_{low} excursions. The circuit of figure 5D will ensure the voltage applied between the bases of Q1 and Q2 does not cause excessive switching delays in the CLC411. Under the above proscribed four-transistor interface, all variations were evaluated with approximately 1ns rise and fall times which produced switching speeds equivalent to the rated disable/enable switching times found in the "CLC411 Electrical Characteristics" table.

A general multiplexer configuration using several CLC411s is illustrated in figure 6, where a typical 8-to-1 digital mux is used to control the switching operation of the paralleled CLC411s. Since "break-before-make" is a guaranteed specification of the CLC411 this configuration works nicely. Notice the buffers used in driving the disable pins of the CLC411s. These buffers may be 15V CMOS logic devices mentioned previously or any variation of the four-transistor comparator illustrated above.

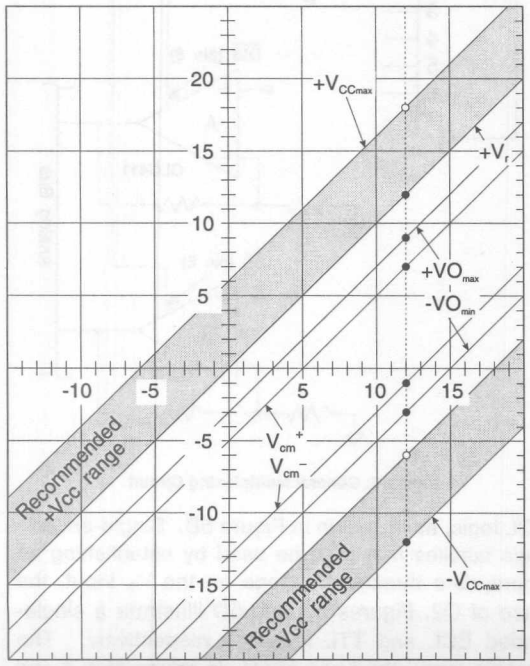
Extending Input/Output Range with V_r

As can be seen in Figure 3, the magnitude of the internal regulated supply voltages is fixed by V_z. In normal operation, with ±15V external supplies, $+V_r$ is nominally+9V when left floating. CMIR (common mode input range) and VO (output voltage range, no load) are specified under these conditions. These parameters implicitly have 0V as their midpoint, i.e. the VO range is ±6V, centered at 0V.

An external voltage source can be applied to $+V_r$ to shift the range of the input/output voltages. For example, if it were desired to move the positive VO range from+6V to a+9V maximum in unipolar operation, Figure 7, "DC Parameters as a Function of $+V_r$", is used to determine the required supply and$+V_r$ voltages. Referring to Figure 7, locate the point on the $+VO_{MAX}$ line where the ordinate is +9V. Draw a vertical line from this point intersecting the other lines in the graph. The circuit voltages are the ordinates of these intersections. For this example these points are shown in the graph as solid dots. The required voltage sources are $+V_r$=+12V, $+V_{CC}$=+12V, $-V_{CC}$=-12V. When these supply and reference voltages are applied, the range for VO is -3V to+9V, and CMIR ranges from -1V to+7V. The difference between the minimum and maximum voltages is constant, i.e. 12V for VO, only the midpoint has been shifted, i.e. from 0V to +3V for VO.

Note that in this example the $-V_r$ pin has been left open (or bypassed to reduce high-frequency noise). The difference between $+V_r$ and $-V_r$ is fixed by V_z. A level-shifting voltage can be applied to only one of the reference pins, not both. If extended operation were needed in the negative direction, Figure 4 may be used by changing the signs, and applying the resultant negative voltage to the $-V_r$ pin. It is recommended that $+V_r$ be used for positive shifts, and $-V_r$ for negative shifts of input/output voltage range.

Figure 7: DC Parameters as a Function of $+V_r$



Printed Circuit Layout & Evaluation Board

Refer to application note OA-15, "Frequent Faux Pas in Applying Wideband Current Feedback Amplifiers," for board layout guidelines and construction techniques. Two very important points to consider before creating a layout which are found in the above application note are worth reiteration. First the input and output pins are sensitive to parasitic capacitances. These parasitic capacitances can cause frequency-response peaking or sustained oscillation. To minimize the adverse effect of parasitic capacitances, the ground plane should be removed from those pins to a distance of at least 0.25" Second, leads should be kept as short as possible in the finished layout. In particular, the feedback resistor should have its shortest lead on the inverting input side of the CLC411. The output is less sensitive to parasitic capacitance and therefore can drive the longer of the two feedback resistor connections. The evaluation board available for the CLC411 (part #730013 for through-hole packages, 730027 for SO-8) may be used as a reference for proper board layout. Application schematics for this evaluation board are in the product accessories section of the Comlinear databook.

Comlinear
A National Semiconductor Company

Dual Wideband Video Op Amp

CLC412

3

APPLICATIONS:

- HDTV, NTSC & PAL video systems
- video switching and distribution
- IQ amplifiers
- wideband active filters
- cable drivers
- dc coupled single-to-differential conversions

FEATURES:

- wide bandwidth 330MHz (A_v=+1V/V)
  250MHz (A_v=+2V/V)
- 0.1dB gain flatness to 30MHz
- low power: 5mA/channel
- very low diff. gain, phase: 0.02%, 0.02°
- -76dB channel-to-channel crosstalk (10MHz)
- fast slew rate: 1300V/µs
- unity-gain stable

DESCRIPTION

The CLC412 combines a high-speed complementary bipolar process with Comlinear's current-feedback topology to produce a very high-speed dual op amp. The CLC412 provides a 250MHz small-signal bandwidth at a gain of +2V/V and a 1300V/µs slew rate while consuming only 50mW per amplifier from ±5V supplies.

The CLC412 offers exceptional video performance with its 0.02% and 0.02° differential gain and phase errors for NTSC and PAL video signals while driving one back terminated 75Ω load. The CLC412 also offers a flat gain response of 0.1dB to 30MHz and very low channel-to-channel crosstalk of -76dB at 10MHz. Additionally, each amplifier can deliver a 70mA continuous output current. This level of performance makes the CLC412 an ideal dual op amp for high-density broadcast-quality video systems.

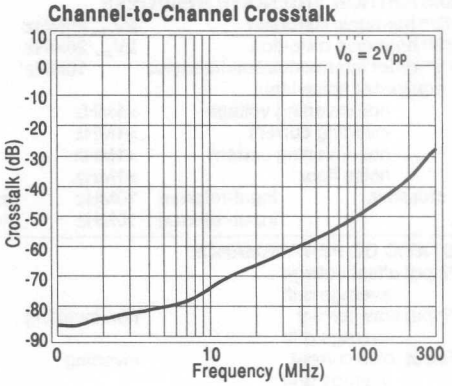
The CLC412's two very well-matched amplifiers support a number of applications such as differential line drivers and receivers. In addition, the CLC412 is well suited for Sallen Key active filters in applications such as anti-aliasing filters for high-speed A/D converters. Its small 8-pin SOIC package, low power requirement, low noise and distortion allow the CLC412 to serve portable RF applications such as IQ-channels.

The CLC412 is available in the following versions.

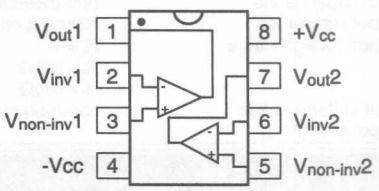
CLC412AJP	-40°C to +85°C	8-pin Plastic DIP
CLC412AJE	-40°C to +85°C	8-pin Plastic SOIC
CLC412AIB	-40°C to +85°C	8-pin CERDIP
CLC412A8B	-55°C to +125°C	8-pin CERDIP, MIL-STD-883, Level B
CLC412A8L-2A	-55°C to +125°C	20-pin LCC, MIL-STD-883, Level B
CLC412ALC	-55°C to +125°C	dice
CLC412AMC	-55°C to +125°C	dice, MIL-STD-883, Level B

Contact factory for other packages and DESC SMD number.

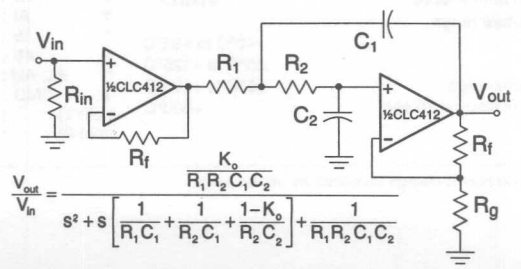
Channel-to-Channel Crosstalk



Pinout
DIP & SOIC



TYPICAL APPLICATION
Sallen-Key Low-Pass Filter



CLC412 Electrical Characteristics (A_V = +2; R_f = 634Ω; V_{CC} = ±5V; R_L = 100Ω)

PARAMETERS	CONDITIONS	TYP	MIN AND MAX RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC412 AJ/AI	+25°C	-40°C	+25°C	+85°C		
Ambient Temperature	CLC412 A8/AM/AL	+25°C	-55°C	+25°C	+125°C		
FREQUENCY DOMAIN RESPONSE							
†-3dB bandwidth	V_{out} < 0.5V_{pp}	250	150	175	135	MHz	SSBW
	V_{out} < 4.0V_{pp}	105	80	80	65	MHz	LSBW
gain flatness	V_{out} < 0.5V_{pp}						
†peaking	DC to 30MHz	0.1	0.1	0.1	0.2	dB	GFP
†rolloff	DC to 30MHz	0.1	0.4	0.3	0.3	dB	GFR
linear phase deviation	DC to 75MHz	0.5	1.3	1.0	1.0	deg	LPD
differential gain	4.43MHz, R_L=150Ω	0.02	0.04	0.04	0.08	%	DG
differential phase	4.43MHz, R_L=150Ω	0.02	0.04	0.04	0.08	deg	DP
TIME DOMAIN RESPONSE							
rise and fall time	0.5V step	1.4	2.3	2.0	2.6	ns	TRS
	4V step	3.2	4.4	4.4	4.8	ns	TRL
settling time to 0.05%	2V step	12	18	18	20	ns	TSS
overshoot	0.5V step	8	15	15	15	%	OS
slew rate	2V step	1300	1000	1000	800	V/µs	SR
DISTORTION AND NOISE RESPONSE							
†2nd harmonic distortion	2V_{pp}, 20MHz	- 46	- 42	- 42	- 38	dBc	HD2
†3rd harmonic distortion	2V_{pp}, 20MHz	- 50	- 46	- 46	- 42	dBc	HD3
3rd order intermodulation intercept	10MHz	43				dBm_{1Hz}	IMD
equivalent noise input							
non-inverting voltage	>1MHz	3.0	3.4	3.4	3.8	nV/√Hz	VN
inverting current	>1MHz	12.0	13.9	13.9	15.5	pA/√Hz	NICN
non-inverting current	>1MHz	2.0	2.6	2.6	3.0	pA/√Hz	ICN
noise floor	>1MHz	- 157	- 156	- 156	- 155	dBm_{1Hz}	SNF
crosstalk input-referred	10MHz (note 1)	- 76	- 70	- 70	- 70	dB	XTLKA
input-referred	10MHz (note 2)	- 70	- 64	- 64	- 64	dB	XTLKB
STATIC DC PERFORMANCE							
*input offset voltage		± 2	± 10	± 6	± 12	mV	VIO
average drift		± 30	± 60	—	± 60	µV/°C	DVIO
*input bias current	non-inverting	± 5	± 28	± 12	± 12	µA	IBN
average drift		± 30	± 187	—	± 90	nA/°C	DIBN
*input bias current	inverting	± 3	± 34	± 15	± 20	µA	IBI
average drift		± 20	± 125	—	± 80	nA/°C	DIBI
†power supply rejection ratio	DC	50	46	46	44	dB	PSRR
♠common mode rejection ratio	DC	50	45	45	43	dB	CMRR
*supply current	R_L= ∞	10.2	13.6	12.8	12.8	mA	ICC
MISCELLANEOUS PERFORMANCE							
input resistance	non-inverting	1000	300	500	500	kΩ	RIN
input capacitance	non-inverting	1.0	2.0	2.0	2.0	pF	CIN
output resistance	closed loop	0.04	0.6	0.3	0.2	Ω	ROUT
output voltage range	R_L= ∞	+ 3.8,-3.3	+ 3.6,-2.9	+ 3.7,-3.0	+ 3.7,-3.0	V	VO
	R_L=100Ω	+ 3.1,-2.9	+ 2.0,-2.5	± 2.7	± 2.7	V	VOL
	R_L=100Ω (0° to 70°C)			+ 2.5,-2.6		V	VOLC
input voltage range	common mode	± 2.2	± 1.4	± 2.0	± 2.0	V	CMIR
output current		70	25	45	45	mA	IO

Absolute Maximum Ratings

V_{cc}	±7V
I_{out} short circuit protected to ground, however maximum reliabiliy is obtained if I_{out} does not exceed...	150mA
common-mode input voltage	±V_{cc}
maximum junction temperature	+175°C
operating temperature range	
AJ/AI	-40°C to +85°C
A8/AM/AL:	-55°C to +125°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

Miscellaneous Ratings

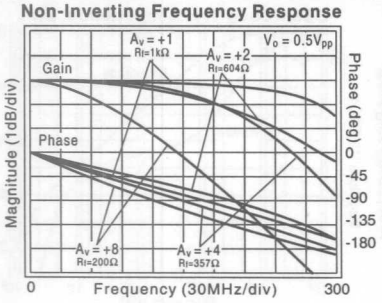
Recommended gain range ±1 to ±10V/V

Notes:

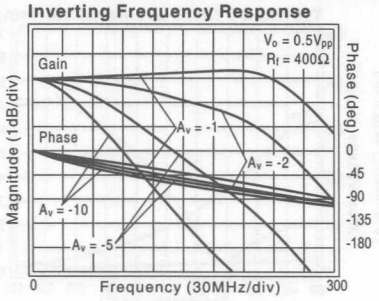
* AJ,AI : 100% tested at +25°C, sample tested at +85°C.
† AJ : Sample tested at +25°C.
† AI : 100% tested at +25°C.
* A8 : 100% tested at +25°C, -55°C, +125°C.
† A8 : 100% tested at +25°C, sample at -55°C, +125°C
* AL, AM : 100% wafer probed +25°C to +25°C min/max specs.
♠ SMD : Sample tested at +25°C, -55°C, +125°C.
note 1) : Specification is guaranteed for AJ, AL, AM only.
note 2) : Specification guaranteed for A8, AI only.

CLC412 Typical Performance (T_A=25°C, V_{CC}=±5V, A_V=±2V/V, R_f=634Ω, R_L=100Ω, unless noted)

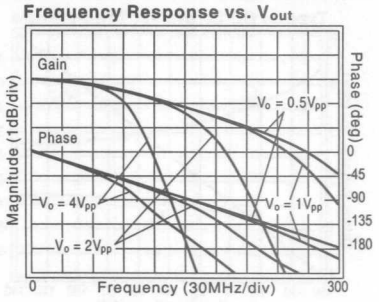
Non-Inverting Frequency Response



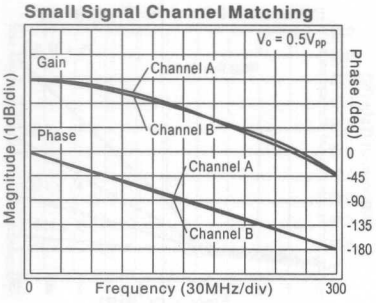
Inverting Frequency Response



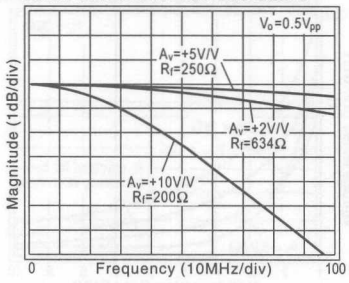
Frequency Response vs. V_{out}



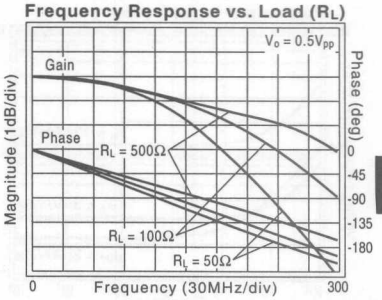
Small Signal Channel Matching



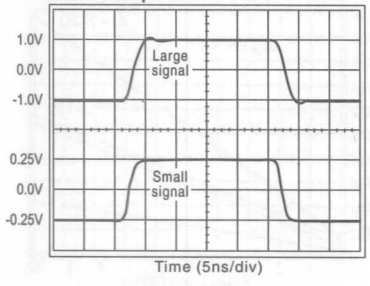
Gain Flatness for Various Gains



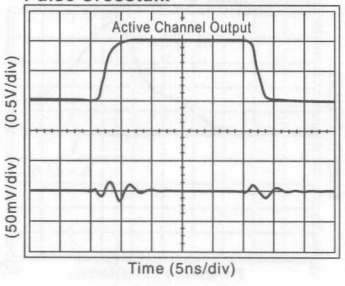
Frequency Response vs. Load (R_L)



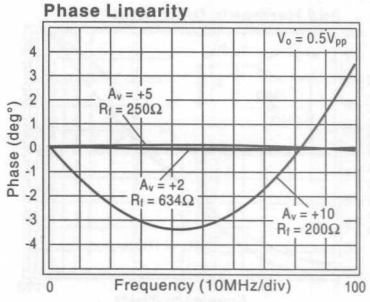
Pulse Response



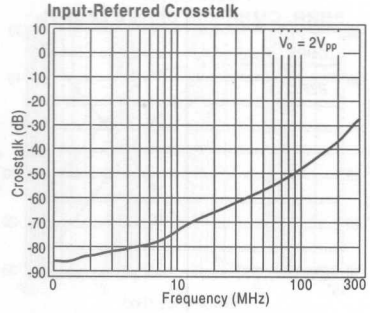
Pulse Crosstalk



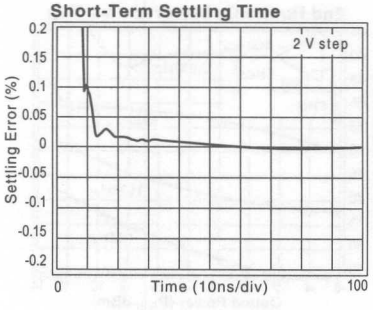
Phase Linearity



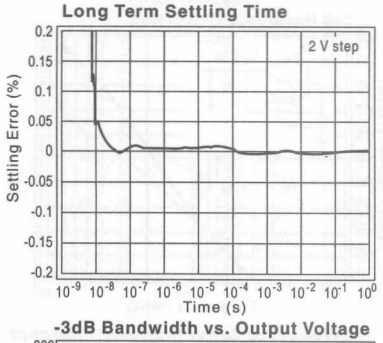
Input-Referred Crosstalk



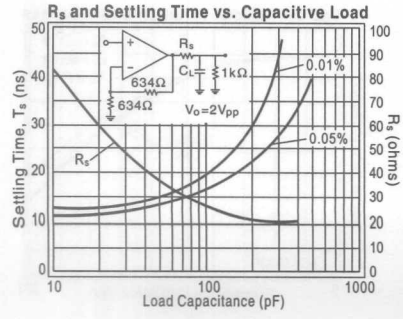
Short-Term Settling Time



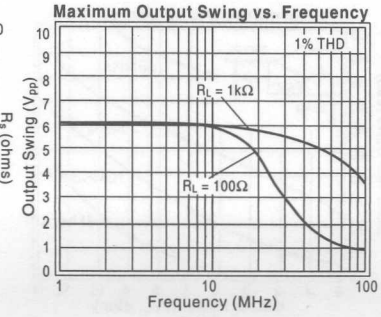
Long Term Settling Time



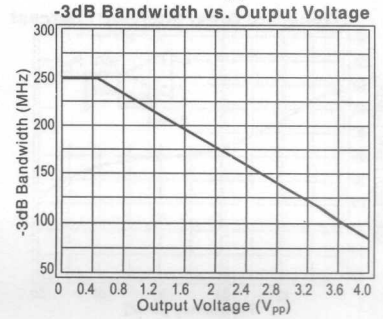
R_s and Settling Time vs. Capacitive Load



Maximum Output Swing vs. Frequency



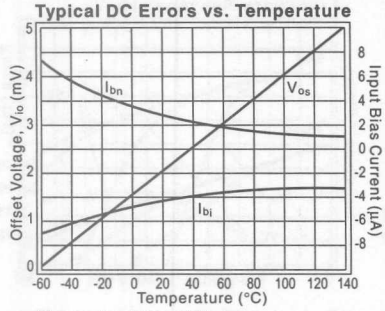
-3dB Bandwidth vs. Output Voltage



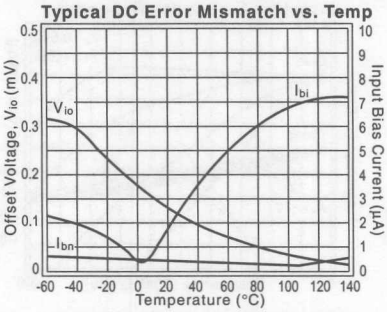
3

CLC412 Typical Performance (T_A=25°C, V_{CC}=5V, A_V=±2V/V, R_L=634Ω, R_L=100Ω, unless noted)

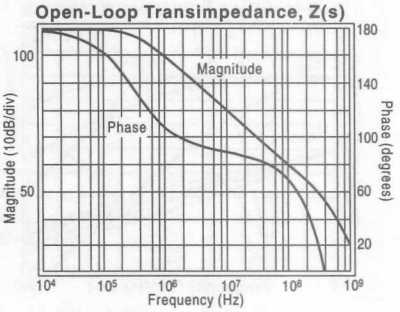
Typical DC Errors vs. Temperature



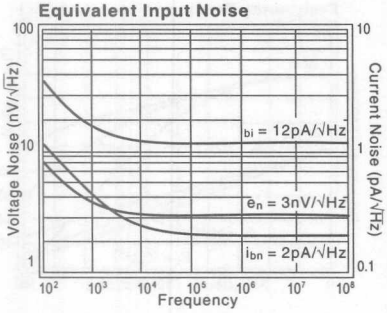
Typical DC Error Mismatch vs. Temp



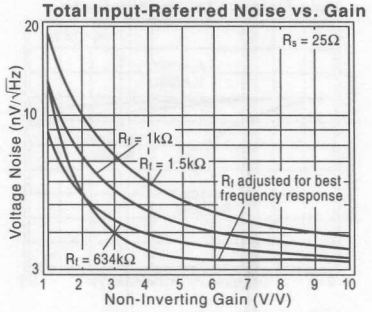
Open-Loop Transimpedance, Z(s)



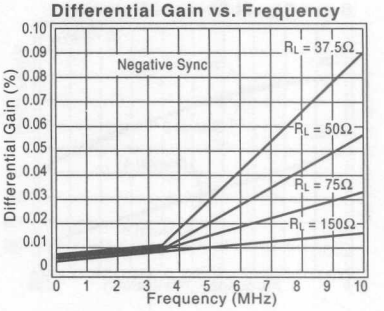
Equivalent Input Noise



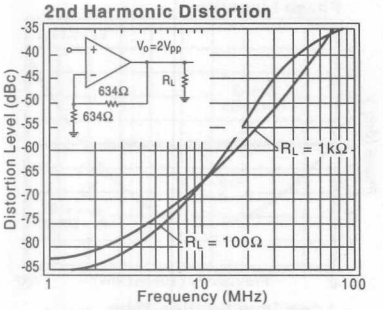
Total Input-Referred Noise vs. Gain



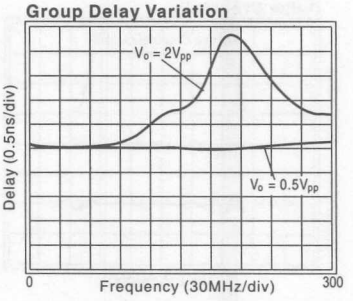
Differential Gain vs. Frequency



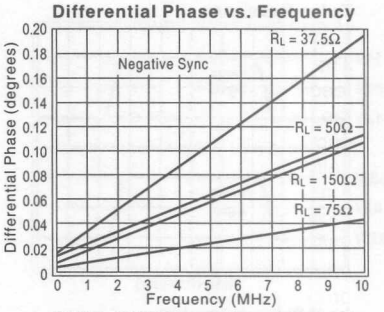
2nd Harmonic Distortion



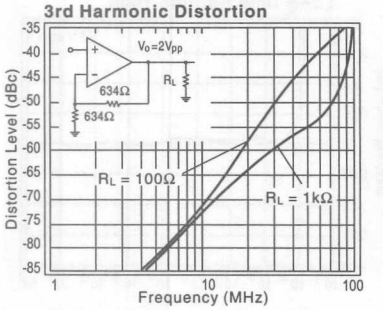
Group Delay Variation



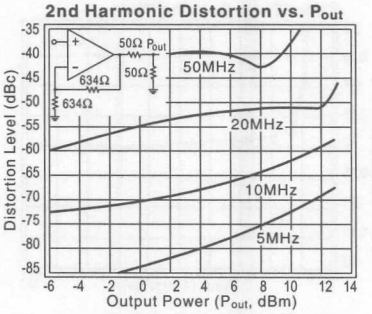
Differential Phase vs. Frequency



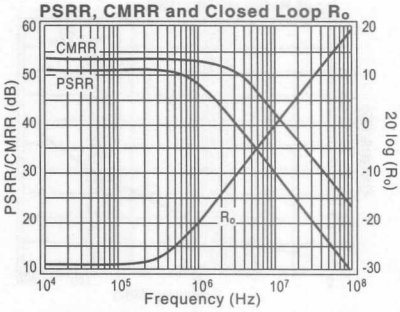
3rd Harmonic Distortion



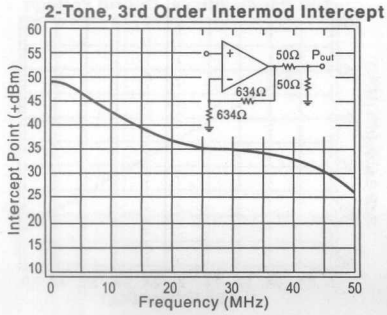
2nd Harmonic Distortion vs. Pout



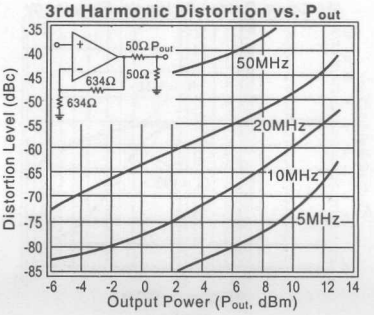
PSRR, CMRR and Closed Loop Ro



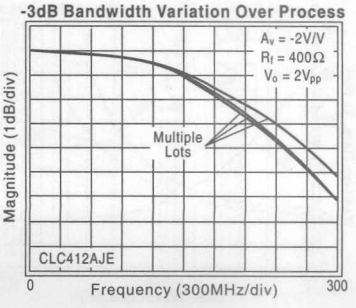
2-Tone, 3rd Order Intermod Intercept



3rd Harmonic Distortion vs. Pout



-3dB Bandwidth Variation Over Process



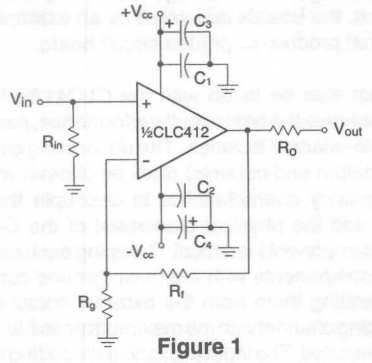


Figure 1

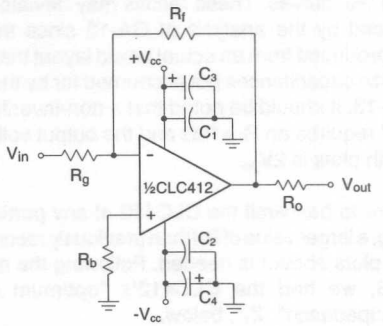


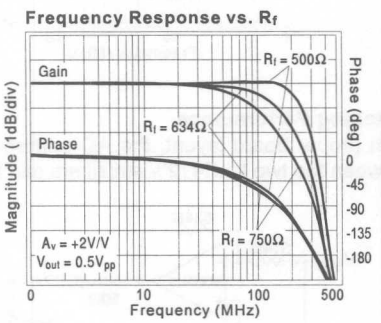
Figure 2

Application Introduction

Offered in an 8-pin package for reduced space and cost, the wideband CLC412 dual current-feedback op amp provides closely matched DC & AC electrical performance characteristics making the part an ideal choice for wideband signal processing. Applications such as broadcast-quality video systems, IQ amplifiers, filter blocks, high-speed peak detectors, integrators and transimpedance amplifiers will all find superior performance in the CLC412 dual op amp.

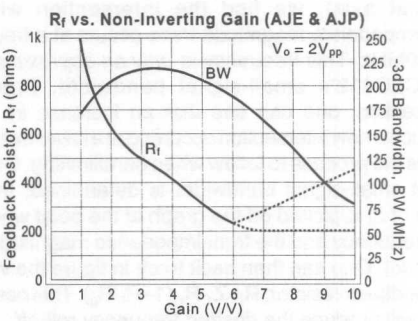
Feedback Resistor Selection

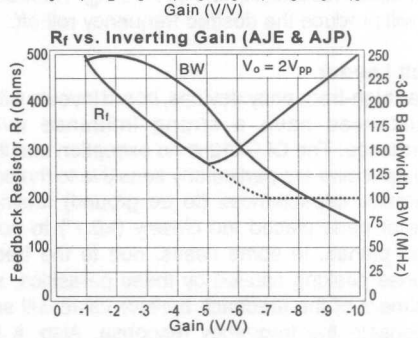
The loop gain and frequency response for a current-feedback operational amplifier is determined largely by the feedback resistor, R_f. The Electrical Characteristics and Typical Performance plots specify an R_f of 634Ω, a gain of +2V/V and operation with ±5V power supplies (unless otherwise stated). Generally, lowering R_f from its recommended value will peak the frequency response and extend the bandwidth while increasing its value will roll off the response. Reducing the value of R_f too far below its recommended value will cause overshoot, ringing and eventually oscillation.



The plot above labeled "Frequency Response vs. R_f" shows the CLC412's frequency and phase response as R_f is varied while the gain remains constant at +2V/V (R_L=100Ω). This plot shows that one particular value of R_f will optimize the frequency and phase response at the specified gain setting, i.e. 634Ω at a gain of +2V/V. Current-feedback op amps, unlike voltage-feedback op amps, have a direct relationship between their frequency and phase response to the value of the feedback resistor, R_f. For more information see Application Note OA-13 which describes the relationship between R_f and closed-loop frequency response.

When configuring the CLC412 for other inverting or non-inverting gains, it is necessary to adjust the value of the feedback resistor in order to optimize the device's frequency and phase response. The two plots below provide the means of selecting the recommended feedback-resistor value for both inverting and non-inverting gain selections. Both plots show the value of R_f approaching a non-zero minimum (dashed line) at high gains, which is characteristic of current-feedback op amps, while the linear portion of the two (solid) curves (i.e. -5>A_v>+6) results from the limitation placed on R_g (i.e. $R_g \geq 50\Omega$). This limitation is due to the desire to keep R_g greater in value than that of the inverting input resistance. Therefore, the resulting small-signal





bandwidth curves, labeled "BW", correspond to the two (solid) "R_f" curves. These results may deviate from that produced by the analysis of OA-13 since these plots were produced from an actual board layout that included parasitic capacitances not accounted for by the analysis of OA-13. It should be noted that a non-inverting gain of +1V/V requires an R_f =1kΩ and the output voltage used for both plots is $2V_{pp}$.

In order to bandlimit the CLC412 at any particular gain setting, a larger value of R_f (than previously recommended in the plots above) is needed. Following the analysis in OA-13, we find the CLC412's "optimum feedback transimpedance", Z_t*, below.

$$Z_t^* = R_f + R_{in}\left(1+\frac{R_f}{R_g}\right)$$
$$= 634 + 60\left(1+\frac{634}{634}\right)$$
$$= 754\Omega$$
$$20\log(754) = 57.5\text{dB}$$

The "optimum feedback transimpedance" is unique for each current-feedback op amp and determines the recommended value of R_f for a particular gain setting. Drawing a horizontal line on the "Open-loop Transimpedance, Z(s)" plot from 57.5dB (on the left vertical axis), we find the intersection with the transimpedance magnitude trace occurs at a frequency of 180MHz. This frequency is *only an approximation* of the CLC412's small-signal bandwidth. From this intersection, one can see that an increase in Z_t will produce a new intersection occurring at a lower frequency. This is the process to follow when bandlimiting. Once the target small-signal bandwidth is determined, the new value of Z_t is picked off the graph at the point where the this frequency and the transimpedance magnitude trace intersect. One can then back track to figure the value of the feedback resistor, R_f=Z_t-R_{in}(1+R_f/R_g). This new value of R_f will produce the desired frequency roll-off.

Circuit Layout

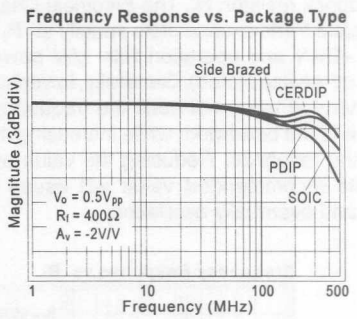
With all high-frequency devices, board layouts with stray capacitances have a strong influence over AC performance. The CLC412 is no exception and its input and output pins are particularly sensitive to the coupling of parasitic capacitances (to ac ground) arising from traces or pads placed too closely (<0.1") to power or ground planes. In some cases, due to the frequency response peaking caused by these parasitics, a small adjustment of the feedback resistor value will serve to compensate the frequency response. Also, it is very important to keep the parasitic capacitance across the feedback resistor to an absolute minimum.

The performance plots in the data sheet can be reproduced using the evaluation boards available from Comlinear. There are two types of boards; the DIP (#730038) and SOIC (#730036). The #730036 board uses all SMT parts for the evaluation of the CLC412 in its surface mount package. Either of these layouts can assist the designer in obtaining the desired performance. In addition, the boards can serve as an example layout for the final production printed circuit board.

Care must also be taken with the CLC412's layout in order to achieve the best circuit performance, particularly channel-to-channel isolation. The decoupling capacitors (both tantalum and ceramic) must be chosen with good high frequency characteristics to decouple the power supplies and the physical placement of the CLC412's external components is critical. Grouping each amplifier's external components with their own ground connection and separating them from the external components of the opposing channel with the maximum possible distance is recommended. The input (R_{in}) and gain-setting resistors (R_g) are the most critical. It is also recommended that the ceramic decoupling capacitor (0.1μF chip or radial-leaded with low ESR) should be placed as closely to the power pins as possible.

Package Parasitics

In addition to the parasitic capacitances arising from the board layout, each of the CLC412's packages has its own characteristic set of parasitic capacitances and inductances causing frequency response variation from package to package as shown in the plot below labeled "Frequency Response vs. Package Type". Due to its much smaller size, the CLC412AJE (8-pin SOIC) shows the least amount of peaking.



Matching Performance

With proper board layout, the AC performance match between the two CLC412's amplifiers can be tightly

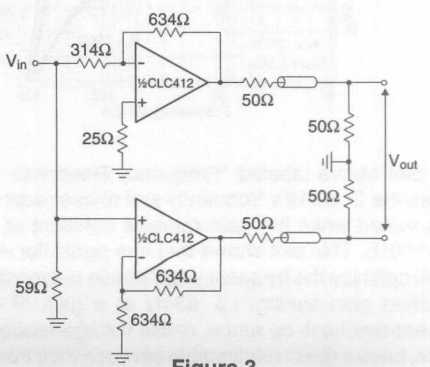
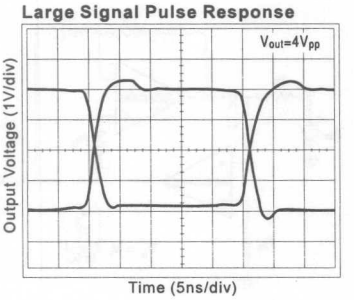


Figure 3

controlled as shown in Typical Performance plot labeled "Small-Signal Channel Matching". The measurements were performed with SMT components using the recommended value of feedback resistor of 634Ω at a gain of +2V/V. The pulse response plot labeled "Pulse Matching" found below shows the group delay matching between amplifiers of the CLC412. The circuit topology is described in Figure 3.



The CLC412's amplifiers, built on the same die, provide the advantage of having tightly matched DC characteristics. The typical DC matching specifications of the CLC412 are:

$\Delta Vio = \pm 0.60mV$, $\Delta Ibn = \pm 0.25\mu A$, $\Delta Ibi = \pm 1.5\mu A$.

Slew Rate and Settling Time

One of the advantages of current-feedback topology is an inherently high slew rate which produces a wider full-power bandwidth. The CLC412 has a typical slew rate of 1300V/μs. The required slew rate for a design can be calculated by the following equation: $SR=2\pi fV_{pk}$

Careful attention to parasitic capacitances is critical to achieving the best settling time performance. The CLC412 has a typical short term settling time to 0.05% of 12ns for a 2 volt step. Also, the amplifier is virtually free of any long term thermal tail effects at low gains as shown in the Typical Performance plot labeled "Long Term Settling Time".

When measuring settling time, a solid ground plane should be used in order to reduce ground inductance which can cause common-ground-impedance coupling. Power supply and ground trace parasitic capacitances and the load capacitance will also affect settling time.

Placing a series resistor (R_s) at the output pin is recommended for optimal settling time performance when driving a capacitive load. The Typical Performance plot labeled "R_s and Settling Time vs. Capacitive Load" provides a means for selecting a value of R_s for a given capacitive load. The plot also shows the resulting settling time to 0.05 and 0.01%.

DC & Noise Performance

A current-feedback amplifier's input stage does not have equal nor correlated bias currents, therefore they cannot be canceled and each contributes to the total DC offset voltage at the output by the following equation:

$$V_{offset} = \pm\left(I_{bn} * R_s\left(1+\frac{R_f}{R_g}\right) + V_{io}\left(1+\frac{R_f}{R_g}\right) + I_{bi} * R_f\right)$$

The input resistor R_{in} is the resistance looking from the non-inverting input back towards the source. For inverting DC-offset calculations, the source resistance seen by the input resistor R_g must be included in the output offset calculation as a part of the non-inverting gain equation. Application note OA-7 gives several circuits for DC offset correction. The noise currents for the inverting and non-inverting inputs are graphed in the Typical Performance plot labeled "Equivalent Input Noise". A more complete discussion of amplifier input-referred noise and external resistor noise contribution can be found in OA-12.

Differential Gain & Phase

The CLC412 can drive multiple video loads with very low differential gain and phase errors. The Typical Performance plots labeled "Differential Gain vs. Frequency" and "Differential Phase vs. Frequency" show performance for loads from 1 to 4. The Electrical Characteristics table also specifies guaranteed performance for one 150Ω load at 4.43MHz. For NTSC video, the guaranteed performance specifications also apply. Application note OA-08, "Differential Gain and Phase for Composite Video Systems," describes in detail the techniques used to measure differential gain and phase.

I/O Voltage & Output Current

The usable common-mode input voltage range (CMIR) of the CLC412 specified in the Electrical Characteristics table of the data sheet shows a range of ±2.2 volts. Exceeding this range will cause the input stage to saturate and clip the output signal.

The output voltage range is determined by the load resistor and the choice of power supplies. With ±5 volts the class A/B output driver will typically drive +3.1/-2.7 volts into a load resistance of 100Ω. Increasing the supply voltages will change the common-mode input and output voltage swings while at the same time increase the internal junction temperature. The output voltage for different load resistors can be determined from the data sheet plots labeled "Frequency Response vs. Load (R_L)" and "Maximum Output Swing vs. Frequency".

Applications Circuits

Single-to-Differential Line Driver.

The CLC412's well matched AC channel-response allows a single-ended input to be transformed to highly-matched push-pull driver. From a 1V single-ended input the circuit of Figure 4 produces 1V differential signal between the two outputs. For larger signals, the input voltage divider (R_1=2R_2) is necessary to limit the input voltage on channel 2. To achieve the same performance when driving a matched load, see Figure 3.

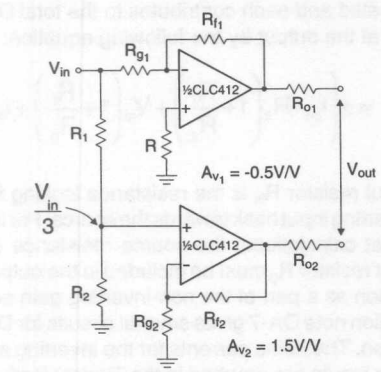


Figure 4

Differential Line Receiver. Figures 5 and 5a show two different implementations of an instrumentation amplifier which convert differential signals to single-ended. Figure 5a allows CMRR adjustment through R_2.

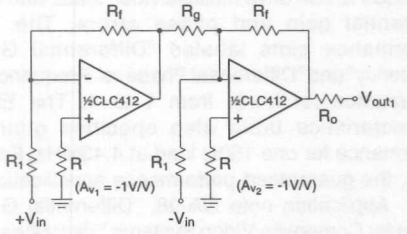


Figure 5

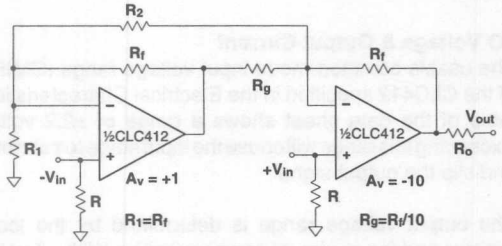


Figure 5a

High-Speed Instrumentation Amplifier.
For applications requiring higher CMRR the composite circuit of Figure 6 uses the two amplifiers of the CLC412 to create balanced inputs for the CLC420 voltage-feedback op amp. The DC CMRR can be fine tuned through the adjustment of R_b. Further improvement of CMRR over frequency can be achieved through the placement of an RC network between the outputs (A and B) of the two amplifiers of the CLC412.

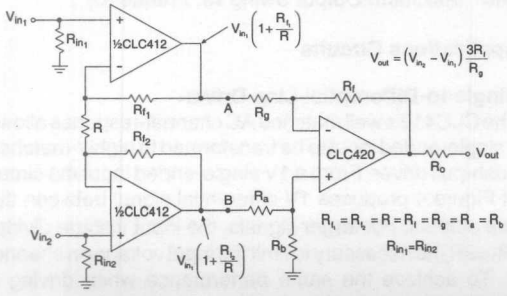


Figure 6

Non-Inverting Current-Feedback Integrator.
The circuit of Figure 7 achieves its high-speed integration by placing one of the CLC412's amplifiers in the feedback loop of the second amplifier configured as shown.

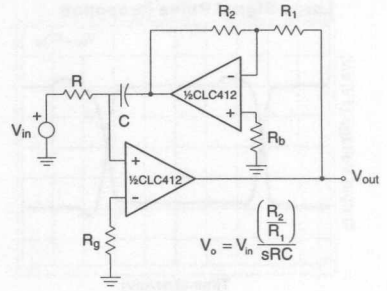


Figure 7

Low-Noise Wide-Bandwidth Transimpedance Amplifier. Figure 8 implements a low-noise transimpedance amplifier using both channels of the CLC412. This circuit takes advantage of the lower input-bias-current noise of the non-inverting input and achieves negative feedback through the second CLC412 channel. The output voltage is set by the value of R_f while frequency compensation is achieved through the adjustment of R_T.

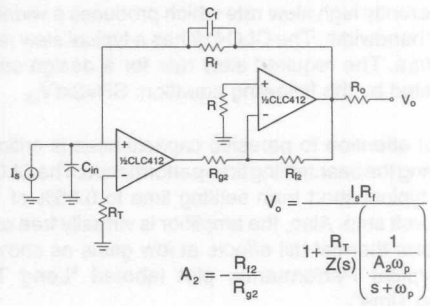


Figure 8

Buffered 2nd-Order Sallen-Key Low-Pass Filter.
Figure 9 shows one implementation of a 2nd order Sallen-Key low pass filter buffered by one of the CLC412's channels. The CLC412 enables greater precision since it provides the advantage of very low output impedance and very linear phase throughout the pass-band.

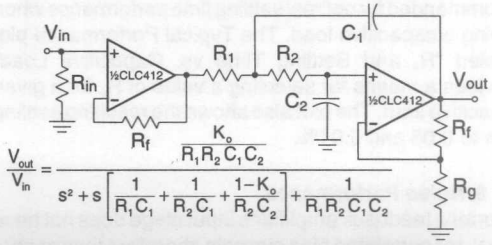


Figure 9

Comlinear
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Dual, Low-Cost, Low-Power, 110MHz Op Amp

Advance Data CLC416

APPLICATIONS:
- Desktop Video Systems
- Video Distribution
- Flash A/D Driver
- High-Speed Driver
- High-Source Impedance Applications
- Professional Video Processing
- High Resolution Monitors

FEATURES:
- Low-cost
- Very low input bias current: 100nA
- High input impedance: 6MΩ
- 110MHz -3dB bandwidth (A_V = +2)
- Low power
- High output current: 60mA

3

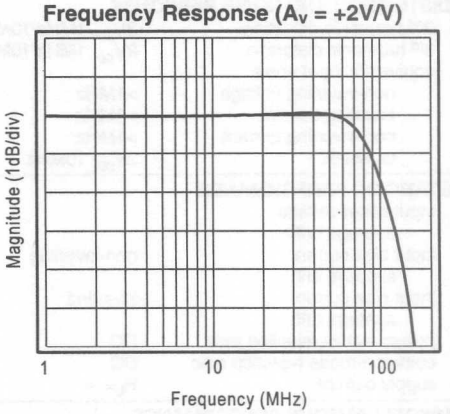
DESCRIPTION

The CLC416 is a dual, low-cost, wideband (110MHz) op amp. The CLC416 consumes only 39mW per channel and can source or sink an output current of 60mA. These features make the CLC416 a versatile, high-speed solution for demanding applications that are sensitive to both power and cost.

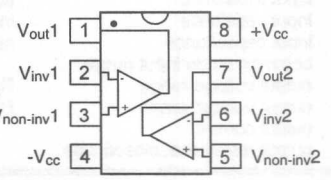
Utilizing Comlinear's proven architectures, this dual current feedback amplifier surpasses the performance of alternative solutions and sets new standards for low power at a low price. This power-conserving dual op amp achieves low distortion with -72dBc and -70dBc for second and third harmonics respectively. Many high source impedance applications will benefit from the CLC416's 6MΩ input impedance. And finally, designers will have a bipolar part with an exceptionally low 100nA non-inverting bias current.

With 0.1dB flatness to 30MHz and low differential gain and phase errors, the CLC416 is an ideal part for professional video processing and distribution. The 110MHz -3dB bandwidth (A_V = +2) coupled with a 350V/µs slew rate also makes the CLC416 a perfect choice in cost-sensitive applications such as video monitors, fax machines, copiers, and CATV systems.

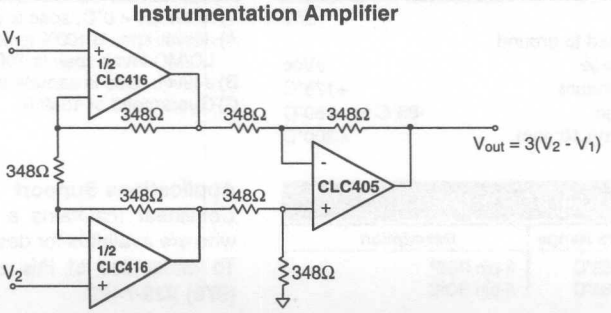
Frequency Response (A_V = +2V/V)



PINOUT
DIP & SOIC



TYPICAL APPLICATION
Instrumentation Amplifier



CLC416 Electrical Characteristics (A_V = +2, R_f = 348Ω: V_{cc} = ± 5V, R_L = 100Ω unless specified)

PARAMETERS	CONDITIONS	TYP	GUARANTEED MIN/MAX			UNITS	NOTES
Ambient Temperature	CLC416AJ	+25°C	+25°C	0 to 70°C	-40 to 85°C		
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth	V_{out} < 1.0V_{pp}	110				MHz	B
	V_{out} < 5.0V_{pp}	42				MHz	1
-3dB bandwidth A_V = +1	V_{out} < 0.5V_{pp} (R_f = 2K)	135				MHz	
±0.1dB bandwidth	V_{out} < 1.0V_{pp}	30				MHz	
gain flatness	V_{out} < 1.0V_{pp}						
peaking	DC to 200MHz	0				dB	B
rolloff	<20MHz	0.05				dB	B
linear phase deviation	<20MHz	0.3				deg	
differential gain	4.43MHz, R_L=150Ω	0.01				%	
differential phase	4.43MHz, R_L=150Ω	0.03				deg	
TIME DOMAIN RESPONSE							
rise and fall time	2V step	5				ns	
settling time to 0.05%	2V step	18				ns	
overshoot	2V step	5				%	
slew rate A_V = +2	2V step	350				V/µs	
A_V = -1	1V step	650				V/µs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 1MHz/10MHz	-72/-55				dBc	B, C
3rd harmonic distortion	2V_{pp}, 1MHz/10MHz	-70/-60				dBc	B, C
equivalent input noise							
non-inverting voltage	>1MHz	5				nV/√Hz	
inverting current	>1MHz	12				pA/√Hz	
non-inverting current	>1MHz	3				pA/√Hz	
crosstalk	2V_{pp}, 10MHz	65				dB	
STATIC DC PERFORMANCE							
input offset voltage		1				mV	A
average drift		30				µV/°C	
input bias current	non-inverting	100				nA	A
average drift		3				nA/°C	
input bias current	inverting	1				µA	A
average drift		17				nA/°C	
power supply rejection ratio	DC	52				dB	B
common-mode rejection ratio	DC	50				dB	
supply current	R_L = ∞	3.9				mA	A
MISCELLANEOUS PERFORMANCE							
input resistance	non-inverting	6				MΩ	
input resistance	inverting	182				Ω	
input capacitance	non-inverting	1				pF	
common mode input range		±2.2				V	
output voltage range	R_L = 100Ω	+ 3.5,-2.8				V	
output voltage range	R_L = ∞ @ package	+4.0,-3.3				V	
output current		60				mA	
output resistance, closed loop		0.06				Ω	

Recommended gain range ±1 to ±40 V/V

Absolute Maximum Ratings

supply voltage	±7V
I_{out} is short circuit protected to ground	
common-mode input voltage	±Vcc
maximum junction temperature	+175°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

Notes

1) At temps < 0°C, spec is guaranteed for R_L = 500Ω.
A) J-level: spec is 100% tested at +25°C, sample tested at +85°C. LC/MC-level: spec is 100% wafer probed at +25°C.
B) J-level: spec is sample tested at +25°C.
C) Guaranteed at 10MHz.

Ordering Information

Model	Temperature Range	Description
CLC416AJP	-40°C to +85°C	8-pin PDIP
CLC416AJE	-40°C to +85°C	8-pin SOIC

Applications Support

Comlinear maintains a staff of applications engineers who are available for design and applications assistance. To make use of this service call **(800) 776-0500 or (970) 225-7422**.

Comlinear
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Dual, Low-Cost, Low-Power, Programmable Gain Buffer

Advance Data CLC417

APPLICATIONS:
- Desktop Video Systems
- Video Distribution
- Flash A/D Driver
- High-Speed Driver
- High-Source Impedance Applications
- Professional Video Processing
- High Resolution Monitors

FEATURES:
- Low-cost
- High output current: 60mA
- High input impedance: 6MΩ
- Gains of ±1, +2 with no external components
- Low power
- Very low input bias currents: 100nA
- Excellent gain accuracy: 0.1%
- High speed: 110MHz -3dB BW

3

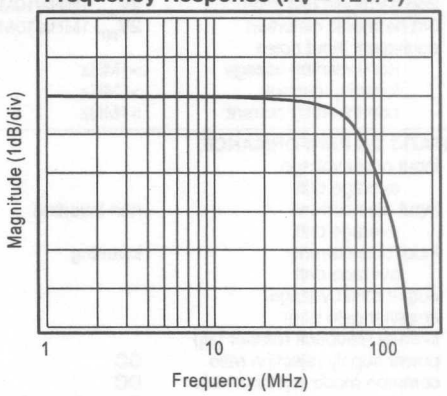
DESCRIPTION

The CLC417 is a dual, low-cost, high-speed (110MHz) buffer which features user-programmable gains of +2, +1, and -1 V/V. The CLC417's high 60mA output current, coupled with its ultra-low 39mW per channel power consumption makes it the ideal choice for demanding applications that are sensitive to both power and cost.

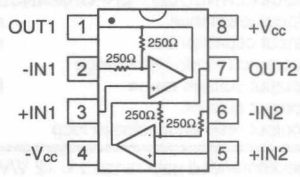
Utilizing Comlinear's proven architectures, this dual current feedback amplifier surpasses the performance of alternate solutions with a closed-loop design that produces new standards for buffers in gain accuracy, input impedance, and input bias currents. The CLC417's internal feedback network provides an excellent gain accuracy of 0.1%. High source impedance applications will benefit from the CLC417's 6MΩ input impedance along with its exceptionally low 100nA input bias current.

With exceptional flatness and low differential gain and phase errors, the CLC417 is very useful for professional video processing and distribution. A 110MHz -3dB bandwidth coupled with a 350V/µs slew rate also make the CLC417 a perfect choice in cost-sensitive applications such as video monitors, fax machines, copiers, and CATV systems. Back-terminated video applications will especially appreciate +2 gains which require no external gain components reducing inventory costs and board space.

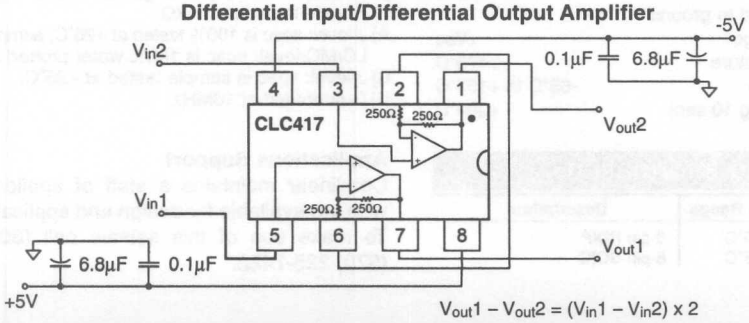
Frequency Response (A_V = +2V/V)



PINOUT
DIP & SOIC



TYPICAL APPLICATION
Differential Input/Differential Output Amplifier



$V_{out}1 - V_{out}2 = (V_{in}1 - V_{in}2) \times 2$

CLC417 Electrical Characteristics (A_V = +2, V_{cc} = ± 5V, R_L = 100Ω unless specified)

PARAMETERS	CONDITIONS	TYP	GUARANTEED MIN/MAX			UNITS	NOTES
Ambient Temperature	CLC417AJ	+25°C	+25°C	0 to 70°C	-40 to 85°C		
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth	V_{out} < 1.0V_{pp}	110				MHz	B
	V_{out} < 5.0V_{pp}	42				MHz	1
±0.1dB bandwidth	V_{out} < 1.0V_{pp}	–				MHz	
gain flatness	V_{out} < 1.0V_{pp}						
peaking	DC to 200MHz	–				dB	B
rolloff	<20MHz	–				dB	B
linear phase deviation	<20MHz	0.3				deg	
differential gain	4.43MHz, RL=150Ω	0.03				%	
differential phase	4.43MHz, RL=150Ω	0.03				deg	
TIME DOMAIN RESPONSE							
rise and fall time	2V step	5				ns	
settling time to 0.05%	2V step	18				ns	
overshoot	2V step	5				%	
slew rate A_V = +2	2V step	350				V/µs	
A_V = -1	1V step	650				V/µs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 1MHz/10MHz	-72/-55				dBc	B, C
3rd harmonic distortion	2V_{pp}, 1MHz/10MHz	-70/-60				dBc	B, C
equivalent input noise							
non-inverting voltage	>1MHz	5				nV/√Hz	
inverting current	>1MHz	12				pA/√Hz	
non-inverting current	>1MHz	3				pA/√Hz	
STATIC DC PERFORMANCE							
input offset voltage		1				mV	
average drift		30				µV/°C	
input bias current	non-inverting	100				nA	A
average drift		3				nA/°C	
input bias current	inverting	1				µA	
average drift		17				nA/°C	
output offset voltage		2.5				mV	A,2
amplifier gain error		±0.1%				V/V	A
internal feedback resistor (R_f)		250				Ω	
power supply rejection ratio	DC	52				dB	B
common-mode rejection ratio	DC	50				dB	
supply current	R_L= ∞ @ package	7.8				mA	A
MISCELLANEOUS PERFORMANCE							
input resistance	non-inverting	6				MΩ	
input capacitance	non-inverting	1				pF	
common mode input range		±2.2				V	
output voltage range	R_L= ∞	+4.0,-3.3				V	
output current		60				mA	
output resistance, closed loop		0.06				Ω	

Recommended gain range ±1, +2 V/V

Absolute Maximum Ratings

supply voltage	±7V
I_{out} is short circuit protected to ground	
common-mode input voltage	±Vcc
maximum junction temperature	+175°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

Ordering Information

Model	Temperature Range	Description
CLC417AJP	-40°C to +85°C	8-pin PDIP
CLC417AJE	-40°C to +85°C	8-pin SOIC

Notes

1) At temps < 0°C, spec is guaranteed for R_L = 500Ω.
2) Source impedance 1kΩ.
A) J-level: spec is 100% tested at +25°C, sample tested at +85°C. LC/MC-level: spec is 100% wafer probed at +25°C.
B) J-level: spec is sample tested at +25°C.
C) Guaranteed at 10MHz.

Applications Support

Comlinear maintains a staff of applications engineers who are available for design and applications assistance. To make use of this service call **(800) 776-0500 or (970) 225-7422.**

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90MHz, Single Supply Voltage Feedback Op Amp

Advance Data CLC423

APPLICATIONS:
- Video ADC Driver
- Desktop Multimedia
- Single Supply Cable Driver
- Instrumentation
- Video cards
- Disk drive actuators
- Wireless IF amplifiers
- Telecommunications

FEATURES:
- Low-cost
- Operates on single +3V, +5V or ±5V supplies
- 92MHz unity-gain bandwidth (+5V supply)
- $2.3V_{pp}$ output on single +3V supply
- Low power: 20mW on +3V supply
- High drive: 46mA output current

3

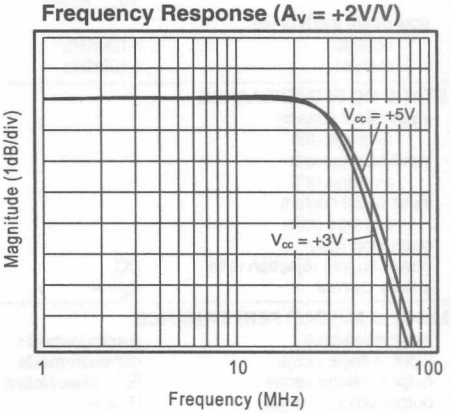
DESCRIPTION

The CLC423 is a wideband, low-cost voltage feedback op amp optimized for high performance on a single +3V to +10V supply. The unique design provides near-rail-to-rail operation, with the input voltage range including the negative rail. Generous headroom for low-voltage range operation was a primary design objective: $2.3V_{pp}$ on a single +3V supply is achieved.

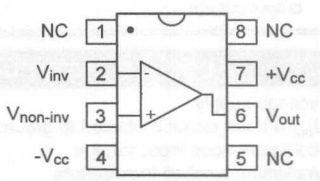
Designed in a high-speed complementary bipolar process, the CLC423 delivers a wide 92MHz unity-gain bandwidth on a single +5V supply. Combined with a fast 130V/µs slew rate, 0.02%/0.33° differential gain/phase errors, and 46mA output current, the CLC423 is ideal for desktop multimedia and video distribution applications. On a single +3V supply, the CLC423 maintains an 82MHz unity-gain bandwidth, 115V/µs slew rate, and 2nd/3rd harmonic distortion of -70/-77dBc ($1V_{pp}$, 1MHz), excellent for portable, battery-operated equipment. Operation on ±5V supplies is similarly impressive, with 72MHz unity-gain bandwidth and 150V/µs slew rate.

Given the CLC423's voltage feedback architecture and high level of performance, it is a perfect choice for wideband signal conditioning circuit functions such as active filters, integrators, differentiators, gain blocks and buffers.

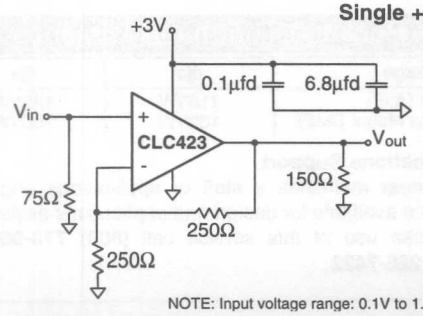
Frequency Response (A_V = +2V/V)



PINOUT
DIP & SOIC

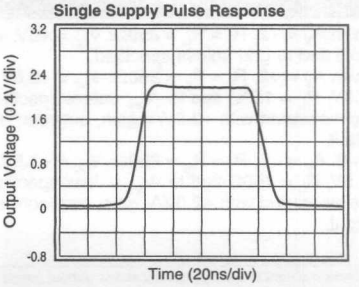


TEST CIRCUIT
Single +3V Supply Operation



NOTE: Input voltage range: 0.1V to 1.1V

Single Supply Pulse Response



CLC423 Electrical Characteristics

PARAMETERS	CONDITIONS	AMBIENT TEMP TYP +25°			UNITS
	CLC423AJ	±5V Supply (See Note 1)	+5V Supply (See Note 2)	+3V Supply (See Note 3)	
FREQUENCY DOMAIN RESPONSE					
-3dB bandwidth	$V_{out} < 0.2V_{pp}$	46	46	42	MHz
	$V_{out} < 1.0V_{pp}$	42	44	40	MHz
-3dB bandwidth $A_V = +1$	$V_{out} < 0.2V_{pp}$	72	92	82	MHz
rolloff	<5MHz	0	0.03	0.02	dB
peaking	DC to 5MHz	0.03	0.01	0.01	dB
differential gain	NTSC, R_L=150Ω	0.28	0.02	0.45	%
differential phase	NTSC, R_L=150Ω	0.53	0.33	0.86	deg
TIME DOMAIN RESPONSE					
rise and fall time	1V step	7.5	7.8	8.5	ns
settling time to 0.05%	1V step	80	–	–	ns
overshoot	1V step	13	5.6	6	%
slew rate $A_V = +2$	2V step	150	130	115	V/µs
DISTORTION AND NOISE RESPONSE					
2nd harmonic distortion	$1V_{pp}$, 1MHz	46	72	70	dBc
	$1V_{pp}$, 5MHz	32	58	56	dBc
3rd harmonic distortion	$1V_{pp}$, 1MHz	60	80	77	dBc
	$1V_{pp}$, 5MHz	42	75	77	dBc
equivalent input noise					
voltage	>100KHz	9.7	9.7	9.7	nV/√Hz
current	>100KHz	3.8	4	4	pA/√Hz
STATIC DC PERFORMANCE					
input offset voltage		1	1	1	mV
average drift		7	2.3	1	µV/°C
input bias current		15	16	16	µA
average drift		61	58	65	nA/°C
input offset current		0.2	0.2	0.2	µA
average drift		3.5	2.3	1.6	nA/°C
open loop gain		70	70	60	dB
power supply rejection ratio	DC	84	79	77	dB
supply current	$R_L = \infty$	7.8	7.4	6.7	mA
MISCELLANEOUS PERFORMANCE					
input resistance	common-mode	1	1	1	MΩ
input voltage range	common-mode	+4.1, -4.8	+1.75, -2.4	+0.7, -1.4	V
output voltage range	R_L = (See Notes)	+3.8, -3.8	+1.9, -2.1	+1.0, -1.3	V
output voltage range	$R_L = \infty$	+4.6, -4.3	+2.2, -1.9	+1.2, -1.1	V
output resistance, closed loop		140	175	220	mΩ
output current		46	46	44	mA

Absolute Maximum Ratings

voltage supply	±6V
I_{out} is short circuit protected to ground	
common-mode input voltage	±Vcc
maximum junction temperature	+175°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+260°C
differential input voltage	±2.0V

Notes

1) Tested with $A_V = +2$, $R_f = R_g = 250\Omega$: $V_{cc} = +5V$, $V_{ee} = -5V$, $R_L = 100\Omega$ tied to gnd unless specified.
2) Tested with $A_V = +2$, $R_f = R_g = 250\Omega$: $V_{cc} = +2.5V$, $V_{ee} = -2.5V$, $R_L = 150\Omega$ tied to $-V_{ee}$ unless specified. DG & Dϕ measured with +2.0V/V gain, between -0.9V & 0.5V output.
3) Tested with $A_V = +2$, $R_f = R_g = 250\Omega$: $V_{cc} = +1.5V$, $V_{ee} = -1.5V$, $R_L = 150\Omega$ tied to $-V_{ee}$ unless specified. DG & Dϕ measured with +2.0V/V gain, between -0.9V & 0.5V output.

Ordering Information

Model	Temperature Range	Description
CLC423AJP	-40°C to +85°C	8-pin PDIP
CLC423AJE	-40°C to +85°C	8-pin SOIC

Package Thermal Resistance

Package	θjc	θja
Plastic (AJP)	115°/W	125°/W
Surface Mount (AJE)	130°/W	150°/W

Applications Support

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Ultra Low Noise Wideband Op Amp

CLC425

APPLICATIONS:

- instrumentation sense amplifiers
- ultrasound pre-amps
- magnetic tape & disk pre-amps
- photo-diode transimpedance amplifiers
- wide band active filters
- low noise figure RF amplifiers
- professional audio systems
- low-noise loop filters for PLLs

FEATURES:

- 1.9GHz gain-bandwidth product
- 1.05nV/√Hz input voltage noise
- 0.8pA/√Hz @ Icc ≤ 5mA
- 100µV input offset voltage, 2µV/°C drift
- 350V/µs slew rate
- 15mA to 5mA adjustable supply current
- gain range ±10 to ±1,000V/V
- evaluation boards and simulation macromodel
- 0.9dB NF @ R_s = 700Ω

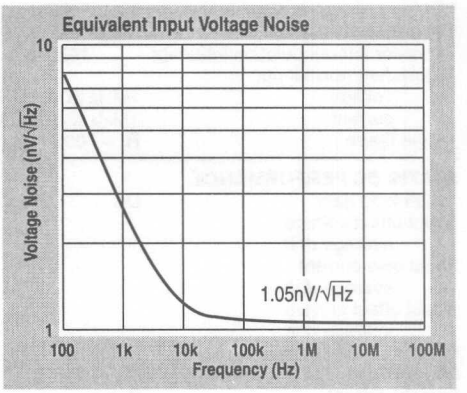
DESCRIPTION

The CLC425 combines a wide bandwidth (**1.9GHz GBW**) with very low input noise (**1.05nV/√Hz, 1.6pA/√Hz**) and low dc errors (**100µV V_{os}, 2µV/° C drift**) to provide a very precise, wide dynamic-range op amp offering closed-loop gains of ≥10.

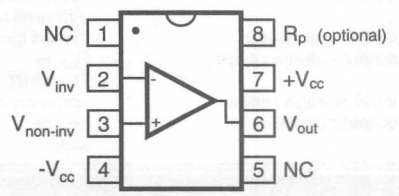
Singularly suited for very wideband high-gain operation, the CLC425 employs a traditional voltage-feedback topology providing all the benefits of balanced inputs, such as low offsets and drifts, as well as a 96dB open-loop gain, a 100dB CMRR and a 95dB PSRR.

The CLC425 also offers great flexibility with its externally adjustable supply current, allowing designers to easily choose the optimum set of power, bandwidth, noise and distortion performance. Operating from ±5V power supplies, the CLC425 defaults to a 15mA quiescent current, or by adding one external resistor, the supply current can be adjusted to less than 5mA.

The CLC425's combination of ultra-low noise, wide gain-bandwidth, high slew rate and low dc errors will enable applications in areas such as medical diagnostic ultrasound, magnetic tape & disk storage, communications and opto-electronics to achieve maximum high-frequency signal-to-noise ratios.



Pinout
DIP & SOIC

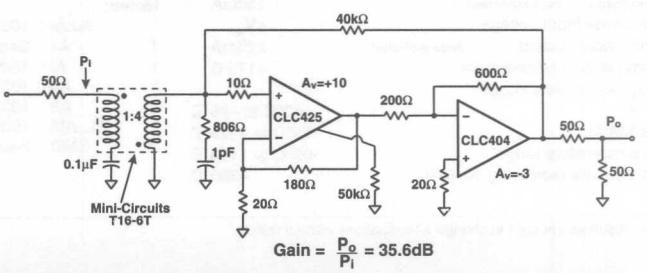


The CLC425 is available in the following versions.

CLC425AJP	-40°C to +85°C	8-pin PDIP
CLC425AJE	-40°C to +85°C	8-pin SOIC
CLC425AIB	-40°C to +85°C	8-pin CerDIP
CLC425A8B	-55°C to +125°C	8-pin CerDIP, MIL-STD-883 Level B
CLC425ALC	-55°C to +125°C	dice
CLC425AMC	-55°C to +125°C	dice, MIL-STD-883 Level B

Contact factory for other packages; DESC SMD number 5962-93259.

TYPICAL APPLICATION
Very Low Noise Figure Amplifier



Gain = $\frac{P_o}{P_i}$ = 35.6dB

CLC425 Electrical Characteristics (V_{CC} = ±5V; A_V = +20; R_f =499Ω; R_g = 26.1Ω; R_L = 100Ω; unless noted)

PARAMETERS	CONDITIONS	TYP	MIN AND MAX RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC425 AJ/AI	+25°C	-40°C	+25°C	+85°C		
Ambient Temperature	CLC425 A8/AM/AL	+25°C	-55°C	+25°C	+125°C		
FREQUENCY DOMAIN RESPONSE							
gain bandwidth product	V_{out} < 0.4V_{pp}	1.9	1.5	1.5	1.0	GHz	GBW
†-3dB bandwidth	V_{out} < 0.4V_{pp}	95	75	75	50	MHz	SSBW
	V_{out} < 5.0V_{pp}	40	30	30	20	MHz	LSBW
gain flatness	V_{out} < 0.4V_{pp}						
†peaking	DC to 30MHz	0.3	0.7	0.5	0.7	dB	GFP
†rolloff	DC to 30MHz	0.1	0.7	0.5	0.7	dB	GFR
linear phase deviation	DC to 30MHz	0.7	1.5	1.5	2.5	°	LPD
TIME DOMAIN RESPONSE							
rise and fall time	0.4V step	3.7	4.7	4.7	7.0	ns	TRS
settling time to 0.2%	2V step	22	30	30	40	ns	TSS
overshoot	0.4V step	5	12	10	12	%	OS
slew rate	2V step	350	250	250	200	V/µs	SR
DISTORTION AND NOISE RESPONSE							
†2nd harmonic distortion	1V_{pp}, 10MHz	- 53	48	48	46	dBc	HD2
†3rd harmonic distortion	1V_{pp}, 10MHz	- 75	65	65	60	dBc	HD3
3rd order intermodulation intercept	10MHz	35				dBm	IMD
equivalent noise input							
voltage	1MHz to 100MHz	1.05	1.25	1.25	1.8	nV/√Hz	VN
current	1MHz to 100MHz	1.6	4.0	2.5	2.5	pA/√Hz	ICN
noise figure	R_s = 700Ω	0.9				dB	NF
STATIC DC PERFORMANCE							
open-loop gain	DC	96	77	86	86	dB	AOL
*input offset voltage		± 100	± 1000	± 800	± 1000	µV	VIO
average drift		± 2	8	—	4	µV/°C	DVIO
*input bias current		12	40	20	20	µA	IB
average drift		- 100	- 250	—	- 120	nA/°C	DIB
input offset current		± 0.2	3.4	2.0	2.0	µA	IIO
average drift		± 3	± 50	—	± 25	nA/°C	DIIO
†power supply rejection ratio	DC	95	82	88	86	dB	PSRR
♠common mode rejection ratio	DC	100	88	92	90	dB	CMRR
*supply current	R_L= ∞	15	18	16	16	mA	ICC
MISCELLANEOUS PERFORMANCE							
input resistance	common-mode	2	0.6	1.6	1.6	MΩ	RINC
	differential-mode	6	1	3	3	kΩ	RIND
input capacitance	common-mode	2.5	3	3	3	pF	CINC
	differential-mode	14				pF	CIND
output resistance	closed loop	5	50	10	10	mΩ	ROUT
output voltage range	R_L= ∞	± 3.8	± 3.5	± 3.7	± 3.7	V	VO
	R_L=100Ω	± 3.4	± 2.8	± 3.2	± 3.2	V	VOL
input voltage range	common mode	± 3.8	± 3.4	± 3.5	± 3.5	V	CMIR
output current	source -55°C/-40°C	90	60/70	70	70	mA	IOP
	sink -55°C/-40°C	90	40/55	55	55	mA	ION

V_{cc}	±7V
I_{out} short circuit protected to ground, however maximum reliabiliy is obtained if I_{out} does not exceed...	150mA
common-mode input voltage	±V_{cc}
differential input current diode protected	±25mA
maximum junction temperature	+175°C
operating temperature range	
AJ/AI	-40°C to +85°C
A8/AM/AL:	-55°C to +125°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

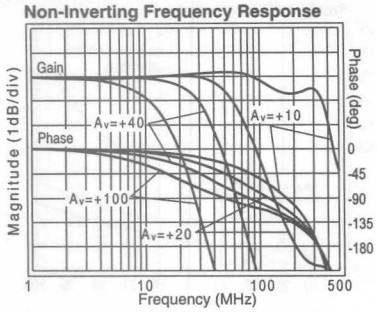
Recommended gain range ±10 to ±1,000V/V

Notes:

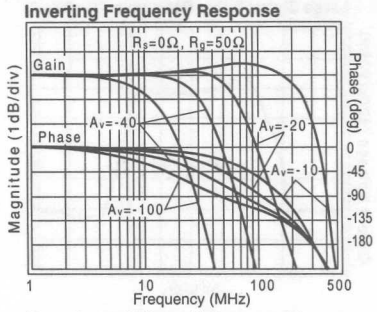
* AJ,AI : 100% tested at +25°C, sample at +85°C.
† AJ : Sample tested at +25°C.
† AI : 100% tested at +25°C.
* A8 : 100% tested at +25°C, -55°C, +125°C.
† A8 : 100% tested at +25°C, sample at -55°C, +125°C
* AL, AM : 100% wafer probed +25°C to +25°C min/max specs.
♠ SMD : Sample tested at +25°C, -55°C and +125°C.

CLC425 Typical Performance (T_A=25°C, V_{CC}=±5V, R_f=26.1Ω, R_f=499Ω, R_L=100Ω, unless noted)

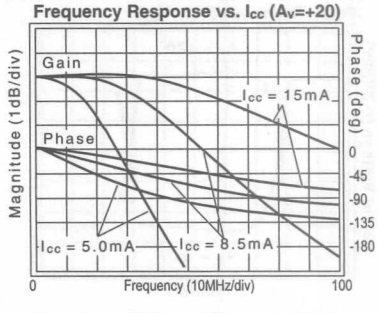
Non-Inverting Frequency Response



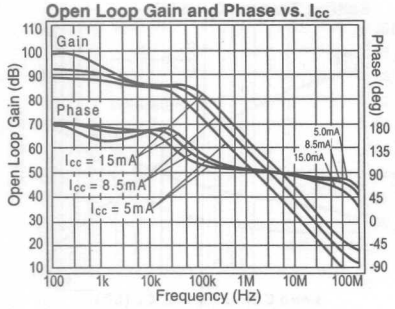
Inverting Frequency Response



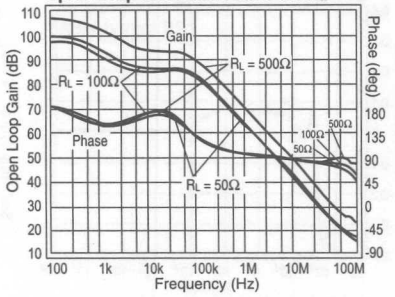
Frequency Response vs. I_{CC} (A_V=+20)



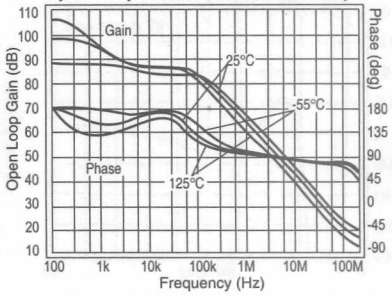
Open Loop Gain and Phase vs. I_{CC}



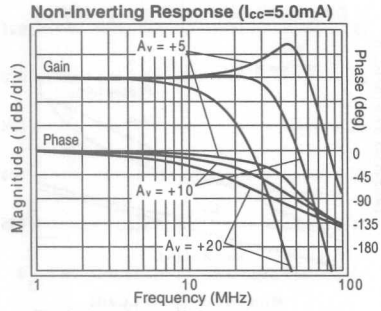
Open Loop Gain and Phase vs. R_L



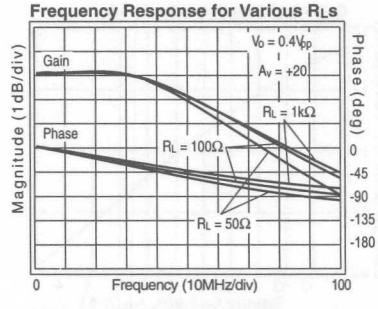
Open Loop Gain and Phase vs. Temp



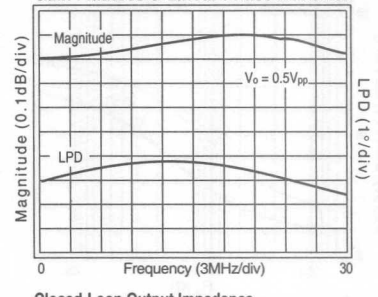
Non-Inverting Response (I_{CC}=5.0mA)



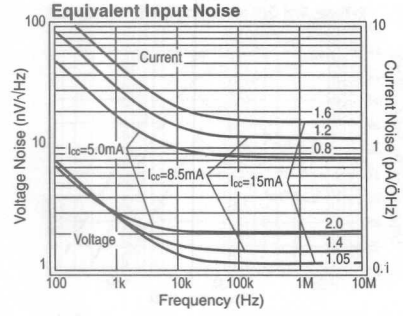
Frequency Response for Various R_{LS}



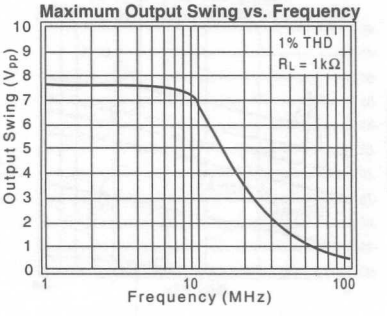
Gain Flatness & Linear Phase Deviation



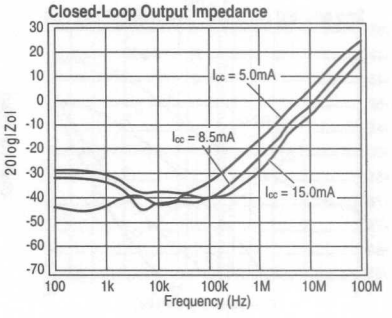
Equivalent Input Noise



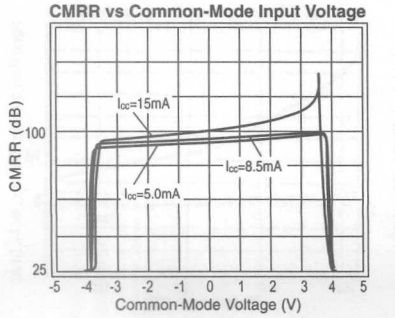
Maximum Output Swing vs. Frequency



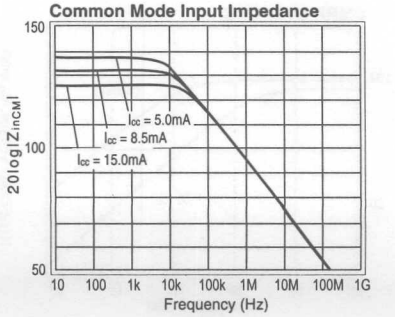
Closed-Loop Output Impedance



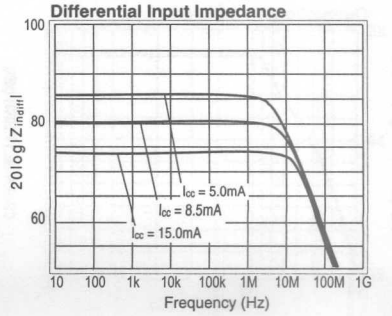
CMRR vs Common-Mode Input Voltage



Common Mode Input Impedance



Differential Input Impedance



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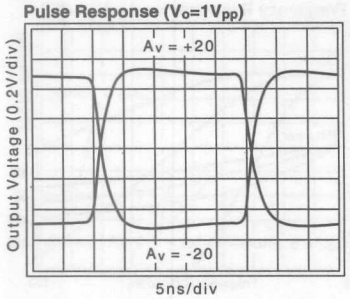
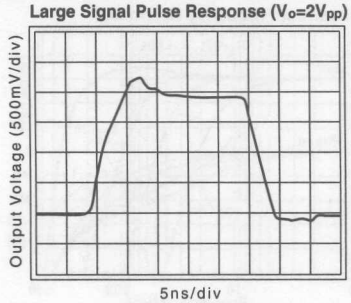
CLC425 Typical Performance (T_A=25°C, V_{cc}=±5V, R_f=26.1Ω, R_f=499Ω, R_L=100Ω, unless noted)

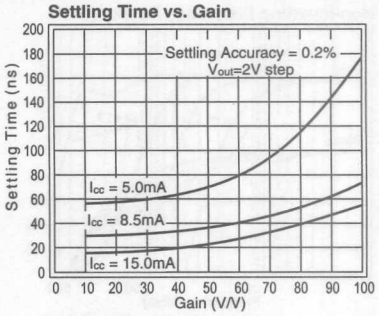
Pulse Response (V_o=1V_{pp})



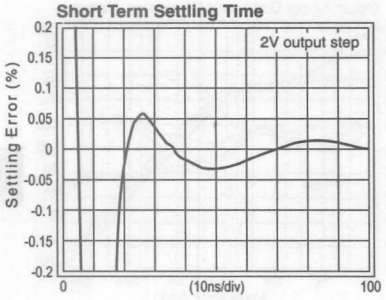
Large Signal Pulse Response (V_o=2V_{pp})



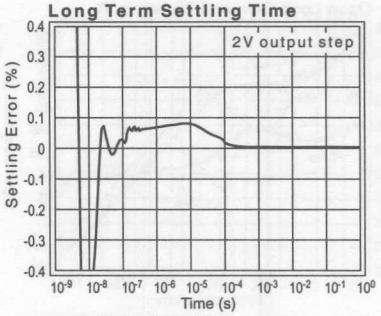
Settling Time vs. Gain



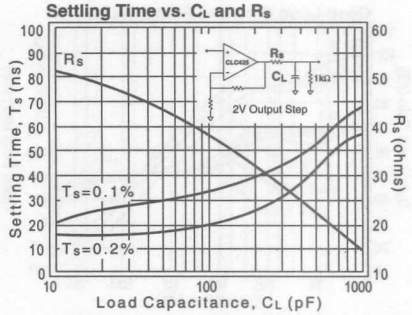
Short Term Settling Time



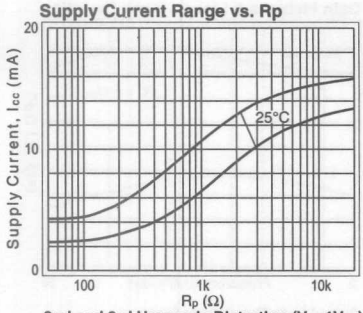
Long Term Settling Time



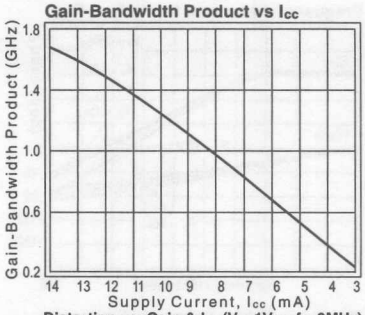
Settling Time vs. C_L and R_s



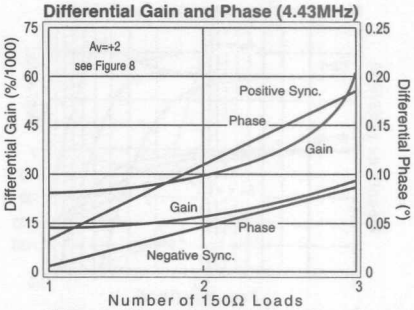
Supply Current Range vs. Rp



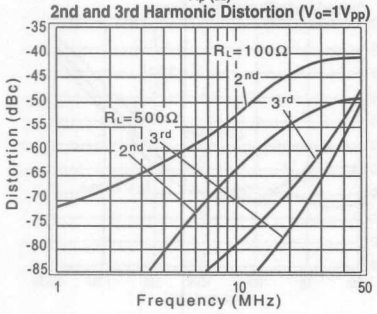
Gain-Bandwidth Product vs I_{cc}



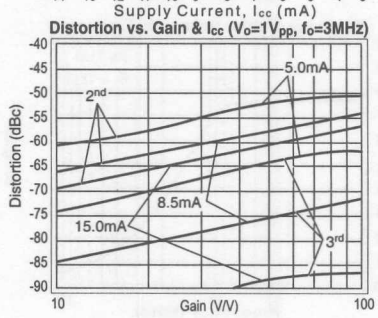
Differential Gain and Phase (4.43MHz)



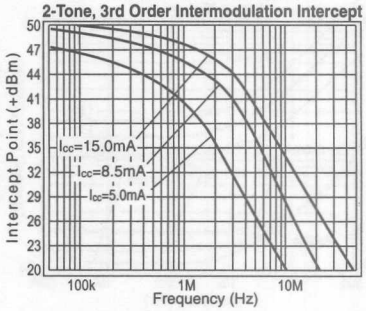
2nd and 3rd Harmonic Distortion (V_o=1V_{pp})



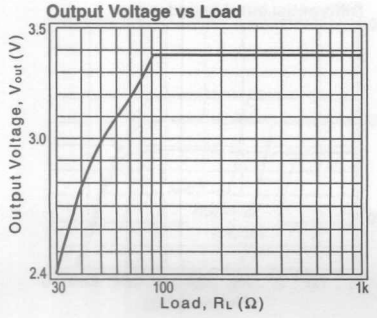
Distortion vs. Gain & I_{cc} (V_o=1V_{pp}, f_o=3MHz)



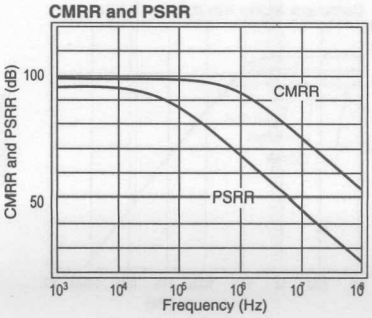
2-Tone, 3rd Order Intermodulation Intercept



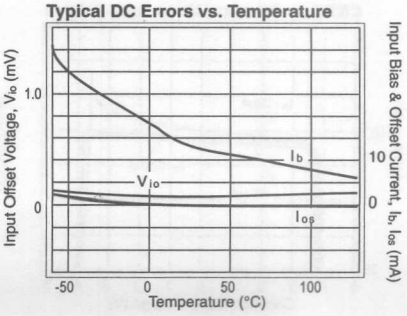
Output Voltage vs Load



CMRR and PSRR



Typical DC Errors vs. Temperature



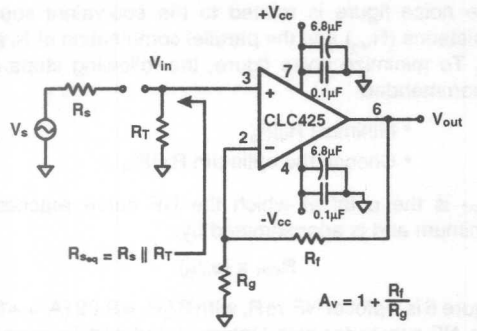


Figure 1: Non-inverting Amplifier Configuration

Introduction

The CLC425 is a very wide gain-bandwidth, ultra-low noise voltage feedback operational amplifier which enables application areas such as medical diagnostic ultrasound, magnetic tape & disk storage and fiber-optics to achieve maximum high-frequency signal-to-noise ratios. The set of characteristic plots located in the "Typical Performance" section illustrates many of the performance trade-offs. The following discussion will enable the proper selection of external components in order to achieve optimum device performance.

Bias Current Cancellation

In order to cancel the bias current errors of the non-inverting configuration, the parallel combination of the gain-setting (R_g) and feedback (R_f) resistors should equal the equivalent source resistance (R_{seq}) as defined in Figure 1. Combining this constraint with the non-inverting gain equation also seen in Figure 1, allows both R_f and R_g to be determined explicitly from the following equations: $R_f=A_vR_{seq}$ and $R_g=R_f/(A_v-1)$. When driven from a 0Ω source, such as that from the output of an op amp, the non-inverting input of the CLC425 should be isolated with at least a 25Ω series resistor.

As seen in Figure 2, bias current cancellation is accomplished for the inverting configuration by placing a resistor (R_b) on the non-inverting input equal in value to the resistance seen by the inverting input ($R_f||(R_g+R_s)$). R_b is recommended to be no less than 25Ω for best CLC425 performance. The additional noise contribution of R_b can be minimized through the use of a shunt capacitor.

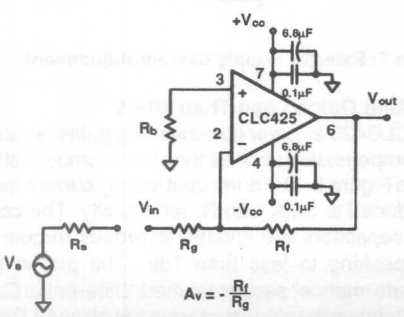
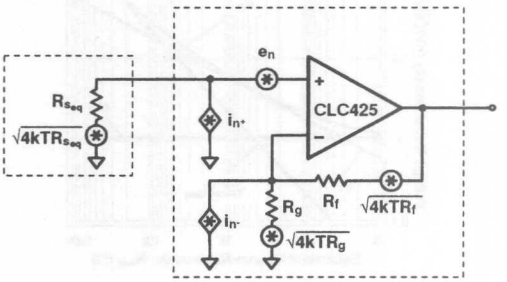


Figure 2: Inverting Amplifier Configuration

Total Input Noise vs. Source Resistance

In order to determine maximum signal-to-noise ratios from the CLC425, an understanding of the interaction between the amplifier's intrinsic noise sources and the noise arising from its external resistors is necessary.

Figure 3 describes the noise model for the non-inverting amplifier configuration showing all noise sources. In addition to the intrinsic input voltage noise (e_n) and current noise ($i_n=i_{n+}=i_{n-}$) sources, there also exists thermal voltage noise ($e_t=\sqrt{4kTR}$) associated with each of the external resistors. Equation 1 provides the general form for total equivalent input voltage noise density (e_{ni}). Equation 2 is a simplification of Equation 1 that assumes



$4kT = 16.4e-21$ *Joules @ 25°C*

Figure 3: Non-inverting Amplifer Noise Model

$$e_{ni} = \sqrt{e_n^2 + \left(i_{n+}R_{s_{eq}}\right)^2 + 4kTR_{s_{eq}} + \left(i_{n-}\left(R_f \| R_g\right)\right)^2 + 4kT\left(R_f \| R_g\right)}$$

Equation 1: General Noise Equation

$R_f||R_g = R_{seq}$ for bias current cancellation. Figure 4 illustrates the equivalent noise model using this assumption. Figure 5 is a plot of e_{ni} against equivalent source resistance (R_{seq}) with all of the contributing voltage noise sources of Equation 2 shown. This plot gives the expected e_{ni} for a given R_{seq} which assumes $R_f||R_g = R_{seq}$ for bias current cancellation. The total equivalent output voltage noise (e_{no}) is $e_{ni}*A_v$.

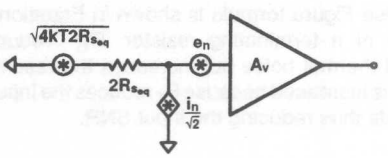


Figure 4: Noise Model with $R_f||R_g = R_{seq}$

$$e_{ni} = \sqrt{e_n^2 + 2\left(i_n R_{s_{eq}}\right)^2 + 4kT\left(2R_{s_{eq}}\right)}$$

Equation 2: Noise Equation with $R_f||R_g = R_{seq}$

As seen in Figure 5, e_{ni} is dominated by the intrinsic voltage noise (e_n) of the amplifier for equivalent source resistances below 33.5Ω. Between 33.5Ω and 6.43kΩ, e_{ni} is dominated by the thermal noise ($e_t=\sqrt{4kTR_{seq}}$) of the external resistors. Above 6.43kΩ, e_{ni} is dominated by the amplifier's current noise ($\sqrt{2}i_nR_{seq}$). The point at which the CLC425's voltage noise and current noise contribute equally occurs for R_{seq}=464Ω (i.e. $e_n/\sqrt{2}i_n$). As an example, configured with a gain of +20V/V giving a -3dB of 90MHz and driven from an R_{seq}=25Ω, the CLC425 produces a total equivalent input noise voltage ($e_{ni}*\sqrt{1.57*90MHz}$) of 16.5μV_{rms}.

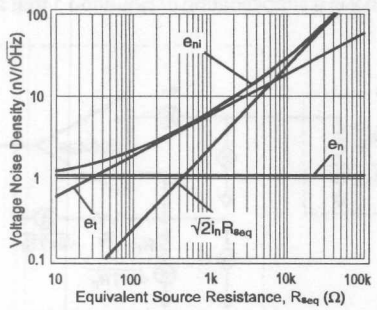


Figure 5: Voltage Noise Density vs. Source Resistance

If bias current cancellation is not a requirement, then $R_f||R_g$ does not need to equal R_{seq}. In this case, according to Equation 1, $R_f||R_g$ should be as low as possible in order to minimize noise. Results similar to Equation 1 are obtained for the inverting configuration of Figure 2 if R_{seq} is replaced by R_b and R_g is replaced by R_g+R_s. With these substitutions, Equation 1 will yield an e_{ni} refered to the non-inverting input. Refering e_{ni} to the inverting input is easily accomplished by multiplying e_{ni} by the ratio of non-inverting to inverting gains.

Noise Figure

Noise Figure (NF) is a measure of the noise degradation caused by an amplifier.

$$NF = 10LOG\left(\frac{S_i/N_i}{S_o/N_o}\right) = 10LOG\left(\frac{e_{ni}^2}{e_t^2}\right)$$

The Noise Figure formula is shown in Equation 3. The addition of a terminating resistor R_T, reduces the external thermal noise but increases the resulting NF. The NF is increased because R_T reduces the input signal amplitude thus reducing the input SNR.

$$NF = 10LOG\left(\frac{e_n^2 + i_n^2\left(R_{seq} + \left(R_f||R_g\right)^2\right) + 4kTR_{seq} + 4kT\left(R_f||R_g\right)}{4kTR_{seq}}\right)$$

R_{seq} = R_s for Unterminated Systems
R_{seq} = R_s II R_T for Terminated Systems

Equation 3: Noise Figure Equation

The noise figure is related to the equivalent source resistance (R_{seq}) and the parallel combination of R_f and R_g. To minimize noise figure, the following steps are recommended:

- Minimize $R_f||R_g$
- Choose the optimum R_s (R_{OPT})

R_{OPT} is the point at which the NF curve reaches a minimum and is approximated by:

$$R_{OPT} \cong (e_n/i_n)$$

Figure 6 is a plot of NF vs R_s with $R_f||R_g$ = 9.09 (A_v = +10). The NF curves for both Unterminated and Terminated systems are shown. The Terminated curve assumes R_s = R_T. The table indicates the NF for various source resistances including R_s = R_{OPT}.

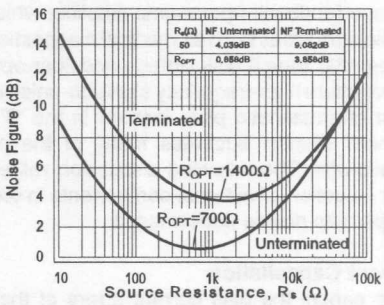


Figure 6: Noise Figure vs Source Resistance

Supply Current Adjustment

The CLC425's supply current can be externally adjusted downward from its nominal value by adding an optional resistor (R_p) between pin 8 and the negative supply as shown in Figure 7. Several of the plots found within the plot pages demonstrate the CLC425's behavior at different supply currents. The plot labeled "I_{cc} vs. R_p" provides the means for selecting R_p and shows the result of standard IC process variation which is bounded by the 25°C curve.

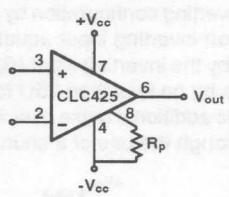


Figure 7: External Supply Current Adjustment

Non-Inverting Gains Less Than 10V/V

Using the CLC425 at lower non-inverting gains requires external compensation such as the shunt compensation as shown in Figure 8. The quiescent supply current must also be reduced to 5mA with R_p for stability. The compensation capacitors are chosen to reduce frequency response peaking to less than 1dB. The plot in the "Typical Performance" section labeled "Differential Gain and Phase" shows the video performance of the CLC425 with this compensation circuitry.

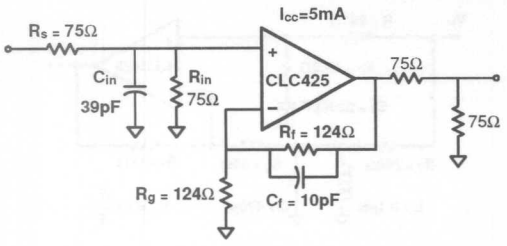


Figure 8: External Shunt Compensation

Inverting Gains Less Than 10V/V

The lag compensation of Figure 9 will achieve stability for lower gains. Placing the network between the two input terminals does not affect the closed-loop nor noise gain, but is best used for the invering configuration because of its affect on the non-inverting input impedance.

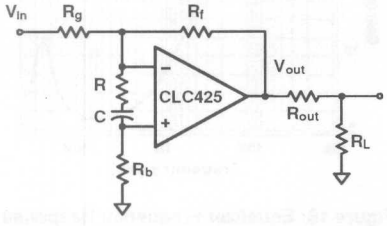


Figure 9: External Lag Compensation

Single-Supply Operation

The CLC425 can be operated with single power supply as shown iin Figure 10. Both the input and output are capacitively coupled to set the dc operating point.

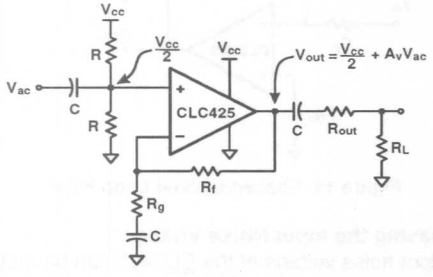


Figure 10: Single Supply Operation

Low Noise Transimpedance Amplifier

The circuit of Figure 11 implements a low-noise transimpedance amplifier commonly used with photo-diodes. The transimpedance gain is set by R_f. The simulated frequency response is shown in Figure 12 and shows the influence C_f has over gain flatness. Equation 4 provides the total input current noise density (i_{ni}) equation for the basic transimpedance configuration and is plotted against feedback resistance (R_f) showing all contributing noise sources in Figure 13. This plot indicates the expected total equivalent input current noise density (i_{ni}) for a given feedback resistance (R_f). The total equivalent output voltage noise density (e_{no}) is $i_{ni}*R_f$.

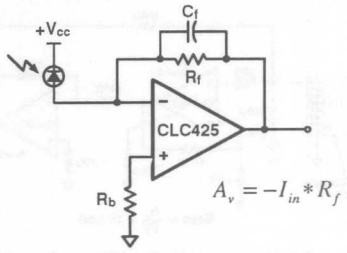


Figure 11: Transimpedance Amplifier Configuration

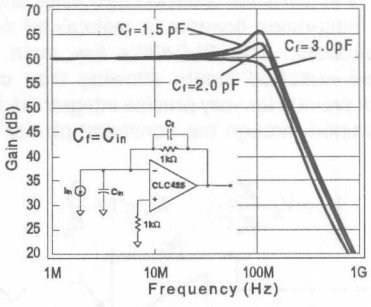


Figure 12: Transimpedance Amplifier Frequency Response

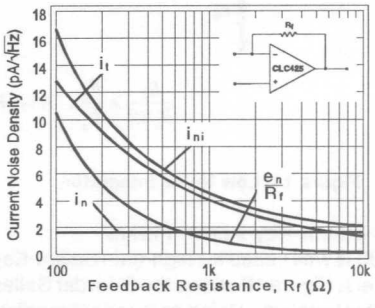


Figure 13: Current Noise Density vs. Feedback Resistance

$$i_{ni} = \sqrt{i_n^2 + \left(\frac{e_n}{R_f}\right)^2 + \frac{4kT}{R_f}}$$

Equation 4: Total Equivalent Input Refered Current Noise

Very Low Noise Figure Amplifier

The circuit of Figure 14 implements a very low Noise Figure amplifier using a step-up transformer combined with a CLC425 and a CLC404. The circuit is configured with a gain of 35.6dB. The circuit achieves measured Noise Figures of less than 2.5dB in the 10-40MHz region. 3rd order intercepts exceed +30dBm for frequencies less than 40MHz and gain flatness of 0.5dB is measured in the 1-50MHz pass bands. Application Note OA-14 provides greater detail on these low Noise Figure techniques.

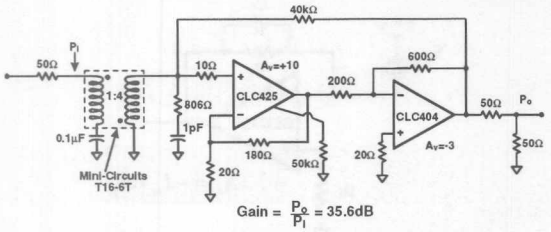
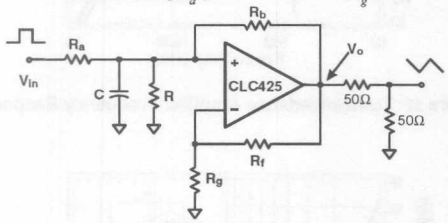


Figure 14: Very Low Noise Figure Amplifier

Low Noise Integrator

The CLC425 implements a deBoo integrator shown in Figure 15. Integration linearity is maintained through positive feedback. The CLC425's low input offset voltage and matched inputs allowing bias current cancellation provide for very precise integration. Stability is maintained through the constraint on the circuit elements.

$$V_o \cong V_{in}\frac{K_o}{sR_aC}; \qquad K_o = 1+\frac{R_f}{R_g}$$



$$\frac{R_b}{R_a \| R} \geq \frac{R_f}{R_g}, \quad R >> R_a$$

Figure 15: Low Noise Integrator

High-Gain Sallen-Key Active Filters

The CLC425 is well suited for high-gain Sallen-Key type of active filters. Figure 16 shows the 2nd order Sallen-Key low pass filter topology. Using component predistortion methods as discussed in OA-21 enables the proper selection of components for these high-frequency filters.

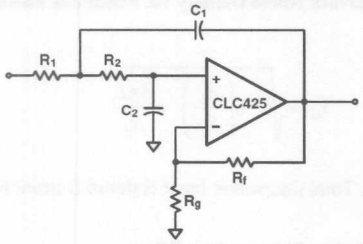
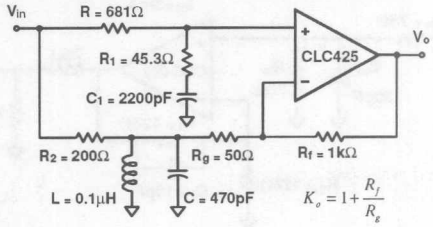


Figure 16: Sallen-Key Active Filter Topology

Low Noise Magnetic Media Equalizer

The CLC425 implements a high-performance low-noise equalizer for such applications as magnetic tape channels as shown in Figure 17. The circuit combines an integrator with a bandpass filter to produce the low-noise equalization. The circuit's simulated frequency response is illustrated in Figure 18.



$$\frac{V_o}{V_{in}} = K_o\left(\frac{sC_1R_1+1}{sC_1(R_1+R)+1} - \left(\frac{R_f}{R_f+R_g}\right)\frac{sLR_g}{s^2LCR_2R_g + sL(R_2+R_g)+R_2R_g}\right)$$

Figure 17: Low Noise Magnetic Media Equalizer

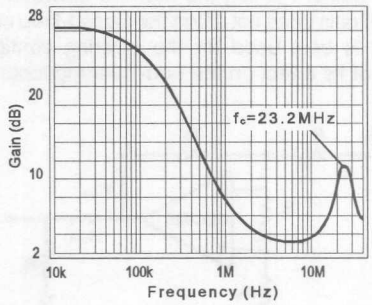


Figure 18: Equalizer Frequency Response

Low-Noise Phase-Locked Loop Filter

The CLC425 is extremely useful as a Phase-Locked Loop filter in such applications as frequency synthesizers and data synchronizers. The circuit of Figure 19 implements one possible PLL filter with the CLC425.

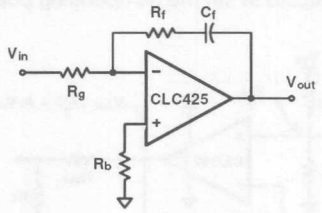


Figure 19: Phased-Locked Loop Filter

Decreasing the Input Noise Voltage

The input noise voltage of the CLC425 can be reduced from its already low $1.05nV/\sqrt{Hz}$ by slightly increasing the supply current. Using a 50kΩ resistor to ground on pin 8, as shown in the circuit of Figure 14, will increase the quiescent current to ≈17mA and reduce the input noise voltage to < $0.95nV/\sqrt{Hz}$.

Printed Circuit Board Layout

Generally, a good high-frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency response peaking and possible circuit oscillation, see OA-15 for more information. Comlinear suggests the 730013 (through-hole) or the 730027 (SOIC) evaluation board as a guide for high-frequency layout and as an aid in device testing and characterization.

Comlinear
A National Semiconductor Company

Wideband, Low-Noise, Voltage-Feedback Op Amp

CLC426

APPLICATIONS:

- Active Filters & Integrators
- Ultrasound
- Low-Power Portable Video
- ADC/DAC Buffer
- Wide Dynamic Range Amp
- Differential Amps
- Pulse/RF Amp

FEATURES:

- Wide Gain-Bandwidth product: 230MHz
- Ultra-Low Input Voltage Noise: 1.6nV/√Hz
- Very Low Harmonic Distortion: -62/-68dBc
- Fast Slew Rate: 400V/µs
- Adjustable Supply Current
- Dual ±2.5 to ±5V or Single 5 to 12V Supplies
- Externally Compensatable

DESCRIPTION

The CLC426 combines an enhanced voltage-feedback architecture with an advanced complementary bipolar process to provide a high-speed op amp with very low noise (1.6nV/√Hz & 2.0pA/√Hz) and distortion (-62/-68dBc 2nd/3rd harmonics at $1V_{pp}$ and 10MHz).

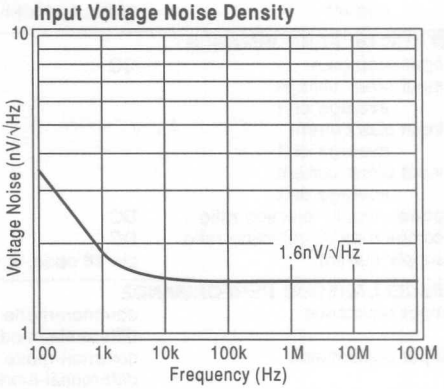
Providing a wide 230MHz gain-bandwidth product, a fast 400V/µs slew rate and very quick 16ns settling time to 0.05% , the CLC426 is the ideal choice for high speed applications requiring a very wide-dynamic range such as an input buffer for high-resolution analog-to-digital converters.

The CLC426 is internally compensated for gains ≥ 2V/V and can easily be externally compensated for unity-gain stability in applications such as wideband low-noise integrators. The CLC426 is also equipped with external supply current adjustment which allows the user to optimize power, bandwidth, noise and distortion performance for each application.

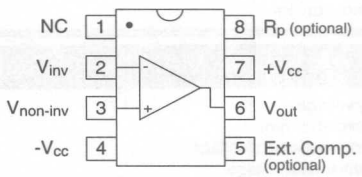
The CLC426's combination of speed, low noise and distortion and low dc errors will allow high-speed signal conditioning applications to achieve the highest signal-to-noise performance. To reduce design times and assist board layout, the CLC426 is supported by an evaluation board and SPICE simulation model available from Comlinear.

For even higher gain-bandwidth voltage-feedback op amps see the 1.9GHz CLC425 ($A_v \geq 10V/V$) or the 5.0GHz CLC422 ($A_v \geq 30V/V$).

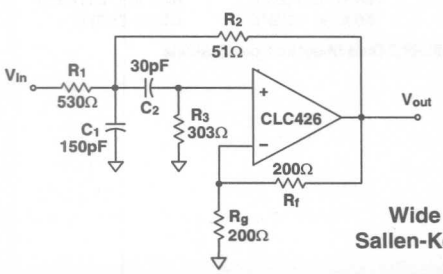
Input Voltage Noise Density



PINOUT
DIP & SOIC

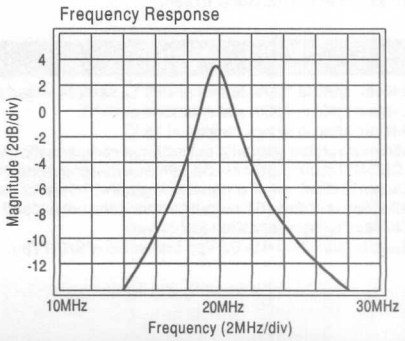


TYPICAL APPLICATION



Wide Dynamic Range Sallen-Key Band Pass Filter 2nd-Order
(20MHz, Q=10, G=2)

Frequency Response



CLC426 Electrical Characteristics (V_{CC} = ±5V; A_V = +2V/V; R_f=100Ω; R_L = 100Ω; unless noted)

PARAMETERS	CONDITIONS	TYP	GUARANTEED MIN/MAX			UNITS	NOTES
Ambient Temperature	CLC426	+25°C	+25°C	0 to +70°C	-40 to +85°C		
FREQUENCY DOMAIN RESPONSE							
gain bandwidth product	V_{out} < 0.5V_{pp}	230	170	120	100	MHz	
-3dB bandwidth, A_V=+2	V_{out} < 0.5V_{pp}	130	90	70	55	MHz	B,1,4
	V_{out} < 5.0V_{pp}	50	25	22	20	MHz	
gain flatness	V_{out} < 0.5V_{pp}						
peaking	DC to 200MHz	0.6	1.5	2.2	2.5	dB	B,4
rolloff	DC to 30MHz	0.0	0.6	1.0	1.0	dB	B,4
linear phase deviation	DC to 30MHz	0.2	1.0	1.5	1.5	°	
TIME DOMAIN RESPONSE							
rise and fall time	1V step	2.3	3.5	5.0	6.5	ns	
settling time	2V step to 0.05%	16	20	24	24	ns	
overshoot	1V step	5	15	15	18	%	
slew rate	5V step	400	300	275	250	V/µs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	1V_{pp},10MHz	- 62	- 52	- 47	- 45	dBc	B
3rd harmonic distortion	1V_{pp},10MHz	- 68	- 58	- 54	- 54	dBc	B
equivalent input noise	op amp only						
voltage	1MHz to 100MHz	1.6	2.0	2.3	2.6	nV/√Hz	
current	1MHz to 100MHz	2.0	3.0	3.6	4.6	pA/√Hz	
STATIC DC PERFORMANCE							
open-loop gain	DC	64	60	54	54	dB	
input offset voltage		1.0	2.0	2.8	2.8	mV	A
average drift		3	---	10	10	µV/°C	
input bias current		5	25	40	65	µA	A
average drift		90	---	600	700	nA/°C	
input offset current		0.3	3	5	5	µA	A
average drift		5	---	25	50	nA/°C	
power-supply rejection ratio	DC	73	65	60	60	dB	B
common-mode rejection ratio	DC	70	62	57	57	dB	
supply current	pin #8 open, R_L= ∞	11	12	13	15	mA	A
MISCELLANEOUS PERFORMANCE							
input resistance	common-mode	500	250	125	125	kΩ	
	differential-mode	750	200	50	25	kΩ	
input capacitance	common-mode	2.0	3.0	3.0	3.0	pF	
	differential-mode	2.0	3.0	3.0	3.0	pF	
output resistance	closed loop	0.07	0.1	0.2	0.2	Ω	
output voltage range	R_L= ∞	± 3.8	± 3.5	± 3.3	± 3.3	V	
	R_L=100Ω	± 3.5	± 3.2	± 2.6	± 1.3	V	
input voltage range	common mode	± 3.7	± 3.5	± 3.3	± 3.3	V	
output current		± 80	± 50	± 40	+ 35, -20	mA	

Absolute Maximum Ratings

supply voltage	±7V
short circuit current	(note 2)
common-mode input voltage	±V_{cc}
differential input voltage	±10V
maximum junction temperature	+200°C
storage temperature	-65°C to+150°C
lead temperature (soldering 10 sec)	+300°C

Notes

A) J-level: spec is 100% tested at +25°C, sample tested at +85°C.
L-level: spec is 100% wafer probed at 25°C.
B) J-level: spec is sample tested at 25°C.
1) Minimum stable gain with out external compensation is +2 or -1V/V, the CLC426 is unity-gain stable with external compensation.
2) Output is short circuit protected to ground, however maximum reliability is obtained if output current does not exceed 200mA.
3) See text for compensation techniques
4) Spec is guaranteed to 0.5Vpp but tested with 0.1Vpp.

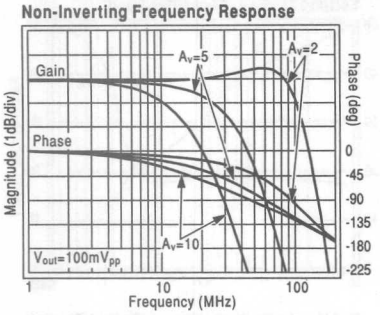
Ordering Information

Model	Temperature Range	Description
CLC426AJP	-40°C to +85°C	8-pin PDIP
CLC426AJE	-40°C to +85°C	8-pin SOIC
CLC426ALC	-40°C to +85°C	dice
CLC426AIB	-40°C to +85°C	8-pin CerDIP
CLC426A8B*	-55°C to +125°C	8-pin CerDIP, MIL-STD-883
CLC426AMC*	-55°C to +125°C	dice, MIL-STD-883
CLC426SMD*	-55°C to +125°C	DESC SMD #

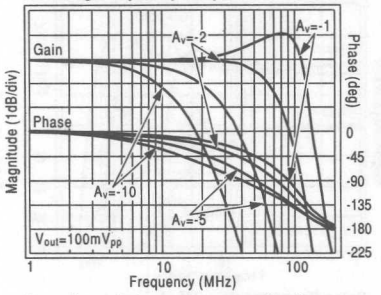
*See CLC426MIL-883 Data Sheet for Specifications

CLC426 Typical Performance (T_A=25°C, $\pm V_{CC}$=±5V, A_V=+2, R_f=100Ω, R_L=100Ω, unless noted)

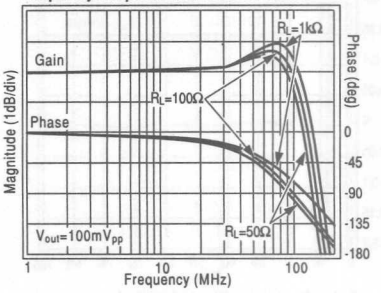
Non-Inverting Frequency Response



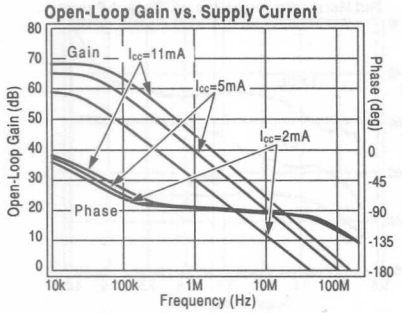
Inverting Frequency Response



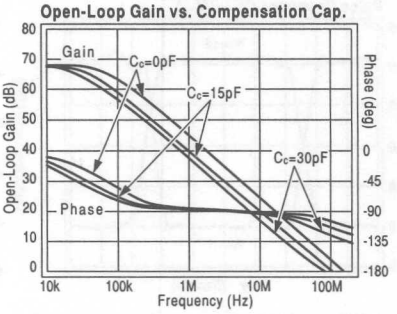
Frequency Response vs. Load Resistance



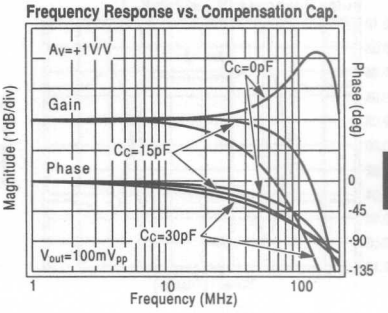
Open-Loop Gain vs. Supply Current



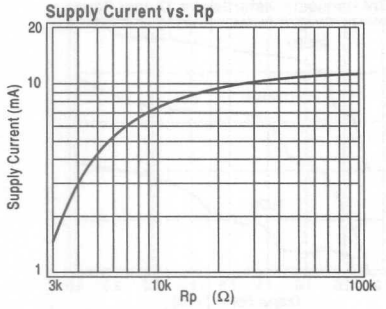
Open-Loop Gain vs. Compensation Cap.



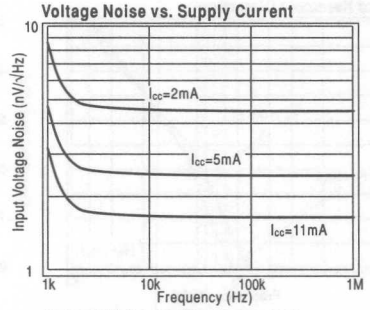
Frequency Response vs. Compensation Cap.



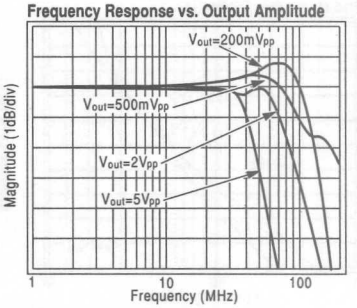
Supply Current vs. Rp



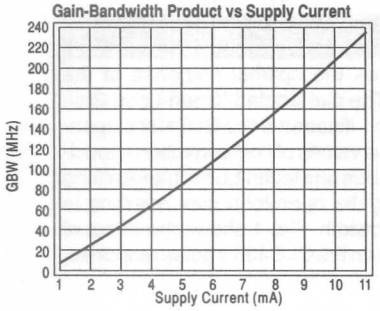
Voltage Noise vs. Supply Current



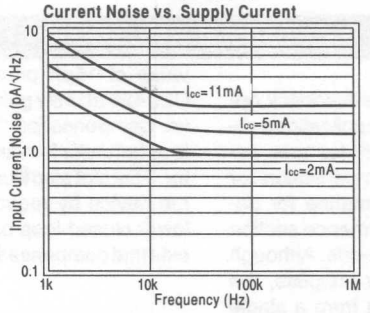
Frequency Response vs. Output Amplitude



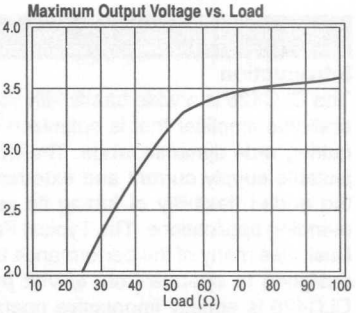
Gain-Bandwidth Product vs Supply Current



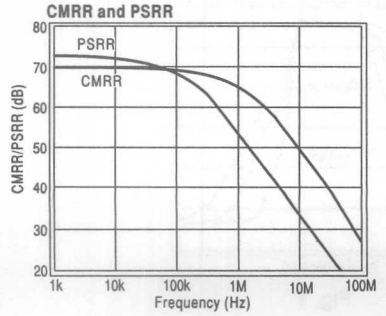
Current Noise vs. Supply Current



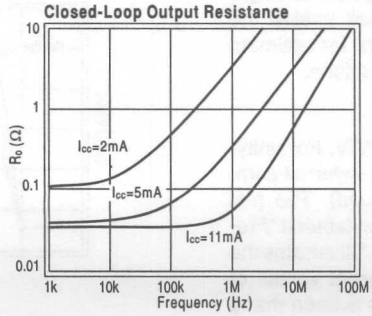
Maximum Output Voltage vs. Load



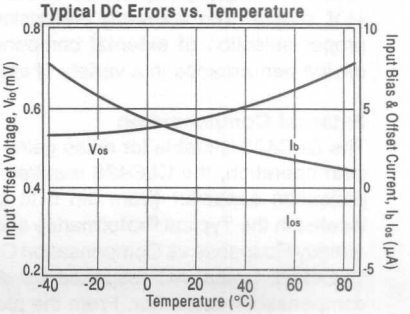
CMRR and PSRR



Closed-Loop Output Resistance

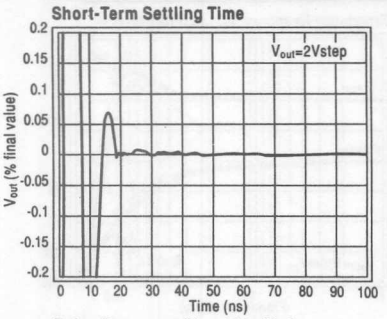


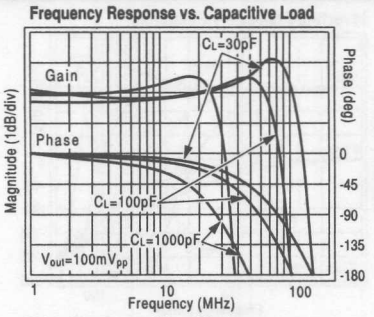
Typical DC Errors vs. Temperature

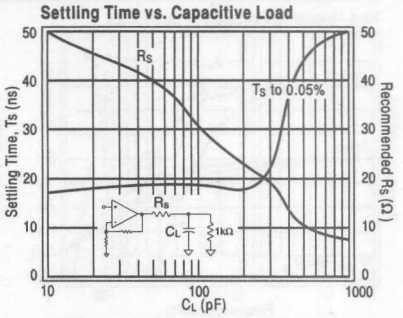


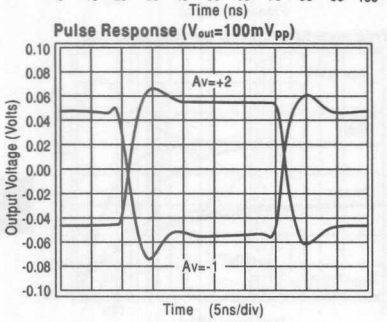
3

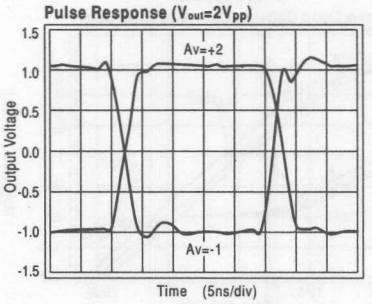
CLC426 Typical Performance (T_A=25°C, $\pm V_{CC}$=±5V, A_V=+2, R_f=100Ω, R_L=100Ω, unless noted)

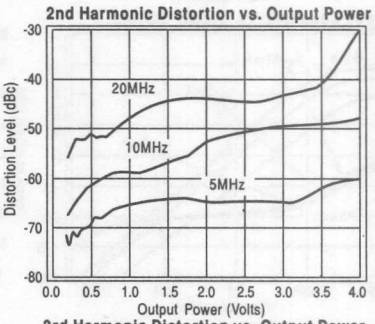


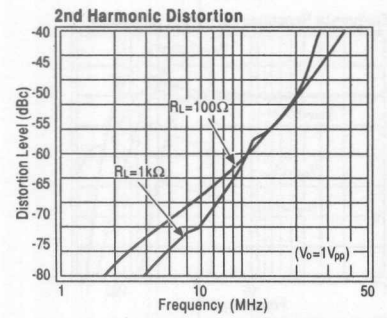


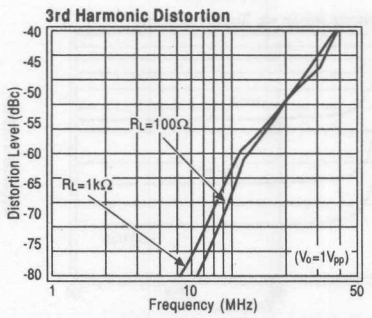


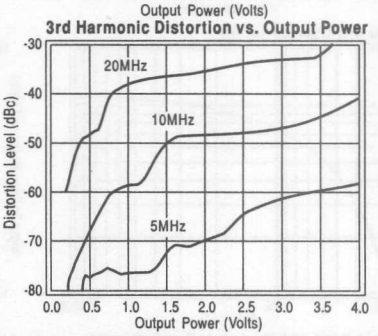












Application Discussion

Introduction

The CLC426 is a wide bandwidth voltage-feedback operational amplifier that is optimized for applications requiring wide dynamic range. The CLC426 features adjustable supply current and external compensation for the added flexibility of tuning its performance for demanding applications. The Typical Performance section illustrates many of the performance trade-offs. Although designed to operate from ±5Volt power supplies, the CLC426 is equally impressive operating from a single +5V supply. The following discussion will enable the proper selection of external components for optimum device performance in a variety of applications.

External Compensation

The CLC426 is stable for noise gains ≥2V/V. For unity-gain operation, the CLC426 requires an external compensation capacitor (from pin 5 to ground). The plot located in the Typical Performance section labeled "Frequency Response vs Compensation Cap." illustrates the CLC426's typical AC response for different values of compensation capacitor. From the plot it is seen that a value of 15pF produces the optimal response of the CLC426 at unity gain. The plot labeled "Open-Loop Gain vs. Compensation Cap." illustrates the CLC426's open-loop behavior for various values of compensation capacitor. This plot also illustrates one technique of bandlimiting the device by reducing the open-loop gain resulting in lower closed-loop bandwidth. Fig. 1 shows the effect of external compensation on the CLC426's pulse response.

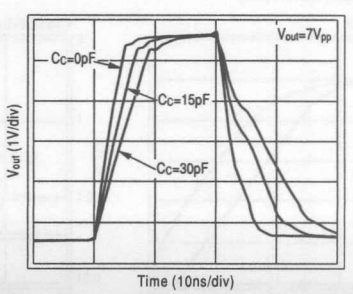


Fig. 1

Supply Current Adjustment

The CLC426's supply current can be externally adjusted downward from its nominal value to less than 2mA by adding an optional resistor (R_p) between pin 8 and the negative supply as shown in fig 2. The plot labeled "Open-Loop Gain vs. Supply Current" illustrates the influence that supply current has over the CLC426's

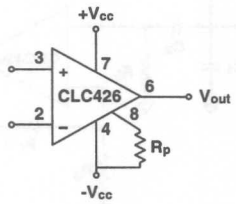


Fig. 2

open-loop response. From the plot it is seen that the CLC426 can be compensated for unity-gain stability by simply lowering its supply current. Therefore lowering the CLC426's supply current effectively reduces its open-loop gain to the point that there is adequate phase margin at unity gain crossover. The plot labeled "Supply Current vs. R_p" provides the means for selecting the value of R_p that produces the desired supply current. The curve in the plot represents nominal processing but a ±12% deviation over process can be expected. The two plots labeled "Voltage Noise vs. Supply Current" and "Current Noise vs. Supply Current" illustrate the CLC426 supply current's effect over its input-referred noise characteristics.

Driving Capacitive Loads

The CLC426 is designed to drive capacitive loads with the addition of a small series resistor placed between the

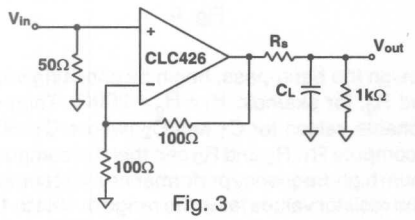


Fig. 3

output and the load as seen in fig. 3. Two plots located in the Typical Performance section illustrate this technique for both frequency domain and time domain applications. The plot labeled "Frequency Response vs. Capacitive Load" shows the CLC426's resulting AC response to various capacitive loads. The values of R_S in this plot were chosen to maximize the CLC426's AC response (limited to ≤1dB peaking).

The second plot labeled "Settling Time vs. Capacitive Load" provides the means for the selection of the value of R_S which minimizes the CLC426's settling time. As seen from the plot, for a given capacitive load R_S is chosen from the curve labeled "R_S". The resulting settling time to 0.05% can then be estimated from the curve labeled "T_S to 0.05%". The plot of fig. 4 shows the CLC426's pulse response for various capacitive loads

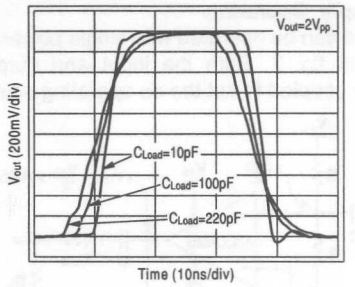


Fig. 4

where R_S has been chosen from the plot labeled "Settling Time vs. Capacitive Load".

Faster Settling

The circuit of fig. 5 shows an alternative method for driving capacitive loads that results in quicker settling times. The small series-resistor, R_S, is used to decouple the CLC426's open-loop output resistance, R_{out}, from

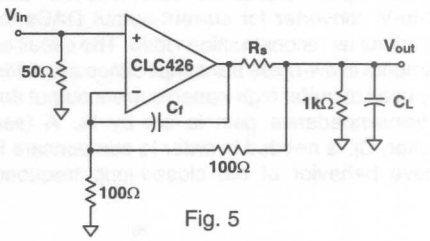


Fig. 5

the load capacitance. The small feedback-capacitance, C_f, is used to provide a high-frequency bypass between the output and inverting input. The phase lead introduced by C_f compensates for the phase lag due to C_L and therefore restores stability. The following equations provide values of R_S and C_f for a given load capacitance and closed-loop amplifier gain.

$$R_s = R_{out}\left(\frac{R_f}{R_g}\right); \quad \text{where } R_{out} \approx 6\Omega \qquad \text{Eq. 1}$$

$$C_f = \left(1+\left(\frac{R_f}{R_g}\right)\right)^2 C_L\left(\frac{R_{out}}{R_g}\right) \qquad \text{Eq. 2}$$

The plot in fig. 6 shows the result of the two methods of capacitive load driving mentioned above while driving a 100pF||1kΩ load.

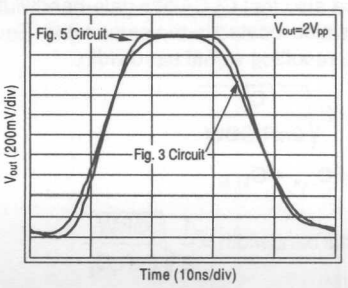


Fig. 6

Single-Supply Operation

The CLC426 can be operated with single power supply as shown in fig. 7. Both the input and output are capacitively coupled to set the dc operating point.

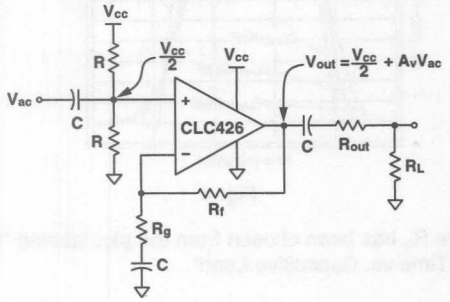


Fig. 7

DAC Output Buffer

The CLC426's quick settling, wide bandwidth and low differential input capacitance combine to form an excellent I-to-V converter for current-output DACs in such applications as reconstruction video. The circuit of fig. 8 implements a low-noise transimpedance amplifier commonly used to buffer high-speed current output devices. The transimpedance gain is set by R_f. A feedback capacitor, C_f, is needed in order to compensate for the inductive behavior of the closed-loop frequency response of this type of circuit. Equation 3 shows a means of calculating the value of C_f which will provide conditions for a maximally-flat signal frequency response with approximately 65° phase margin and 5% step-response overshoot. Notice that C_t is the sum of the DAC output capacitance and the differential input capacitance of the CLC426 which is located in its Electrical Characteristics Table. Notice also that CLC426's gain-bandwidth product (GBW) is also located in the same table. Equation 5 provides the resulting signal bandwidth.

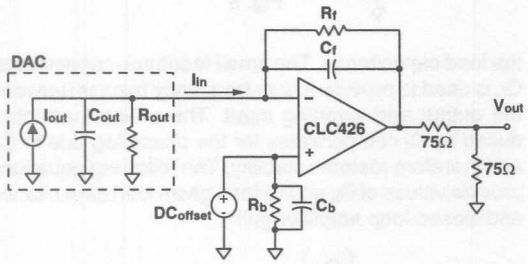


Fig. 8

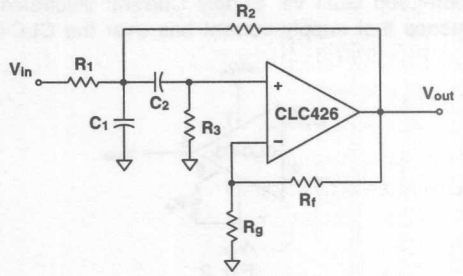
$$C_f = 2\sqrt{\frac{C_t}{2\pi R_f GBW}} \qquad \text{Eq. 3}$$

$$C_t = C_{out} + C_{in\,dif} \qquad \text{Eq. 4}$$

$$\text{signal bandwidth} = \frac{1}{2}\sqrt{\frac{GBW}{2\pi R_f C_t}} \qquad \text{Eq. 5}$$

Sallen-Key Active Filters

The CLC426 is well suited for Sallen-Key type of active filters. Fig. 9 shows the 2nd order Sallen-Key band-pass filter topology and design equations.



$$C_2 = \frac{1}{5}C_1$$

$$G = 1 + \frac{R_f}{R_g}, \text{ desired mid-band gain}$$

$$R_1 = 2\frac{Q}{GC_1(2\pi f)}, \text{ where f = desired center frequency}$$

$$R_2 = \frac{GR_1\left(\sqrt{1+4.8Q^2-2G+G^2}+1\right)}{4.8Q^2-2G+G^2}$$

$$R_3 = \frac{5GR_1\left(\sqrt{1+4.8Q^2-2G+G^2}+G-1\right)}{4Q^2}$$

Fig. 9

To design the band-pass, begin by choosing values for R_f and R_g, for example $R_f = R_g = 200\Omega$. Then choose reasonable values for C_1 and C_2 (where $C_1=5C_2$) and then compute R_1. R_2 and R_3 can then be computed. For optimum high-frequency performance it is recommended that the resistor values fall in the range of 10Ω to 1kΩ and the capacitors be kept above 10pF. The design can be further improved by compensating for the delay through the op amp. For further details on this technique, please request Application Note OA-21 from Comlinear Corporation.

Printed Circuit Board Layout

Generally, a good high-frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitances on these nodes to ground will cause frequency-response peaking and possible circuit oscillation, see OA-15 for more information. Comlinear suggests the 730013 (through-hole) or the 730027 (SOIC) evaluation board as a guide for high-frequency layout and as an aid in device testing and characterization.

Comlinear
A National Semiconductor Company

Dual Wideband, Low-Noise, Voltage-Feedback Op Amp

CLC428

APPLICATIONS:

- General purpose dual op amp
- Low noise integrators
- Low noise active filters
- Diff-in/diff-out instrumentation amp
- Driver/receiver for transmission systems
- High-speed detectors
- I/Q channel amplifiers

FEATURES:

- Wide unity-gain bandwidth: 160MHz
- Ultra-low noise: 2.0nV/√Hz
- Low distortion: -78dBc 2nd (2MHz)
  -62/-72dBc (10MHz)
- Settling time: 16ns to 0.1%
- Supply voltage range: ±2.5 to ±5 or single supply
- High output current: ±80mA

DESCRIPTION

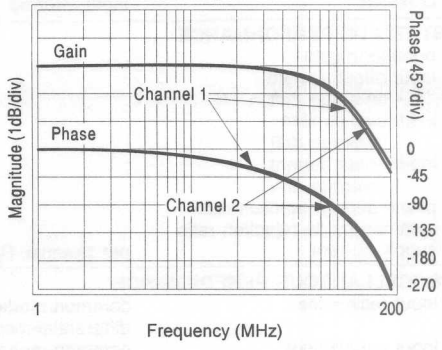
The CLC428 is a very high-speed dual op amp that offers a traditional voltage-feedback topology featuring unity-gain stability and slew-enhanced circuitry. The CLC428's ultra low noise and very low harmonic distortion combine to form a very wide dynamic-range op amp that operates from a single (5 to 12V) or dual (±5V) power supply.

Each of the CLC428's closely matched channels provides a 160MHz unity-gain bandwidth with an ultra low input voltage noise density (2nV/√Hz). Very low 2nd/3rd harmonic distortion (-62/-72dBc) as well as high channel-to-channel isolation (-62dB) make the CLC428 a perfect wide dynamic-range amplifier for matched I/Q channels.

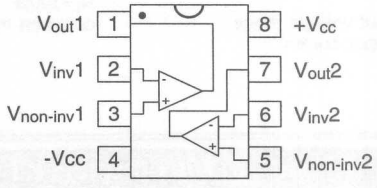
With its fast and accurate settling (16ns to 0.1%), the CLC428 is also a excellent choice for wide-dynamic range, anti-aliasing filters to buffer the inputs of hi-resolution analog-to-digital converters. Combining the CLC428's two tightly-matched amplifiers in a single eight-pin SOIC reduces cost and board space for many composite amplifier applications such as active filters, differential line drivers/receivers, fast peak detectors and instrumentation amplifiers.

To reduce design times and assist in board layout, the CLC428 is supported by an evaluation board and a SPICE simulation model available from Comlinear.

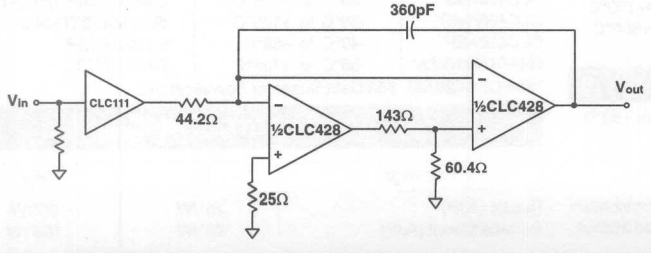
Channel Matching



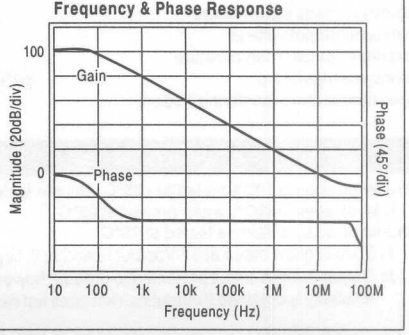
PINOUT
DIP & SOIC



TYPICAL APPLICATION
5-Decade Integrator



Frequency & Phase Response



Comlinear Corporation • 4800 Wheaton Drive • Fort Collins, CO 80525 • (800) 776-0500 • FAX (970) 226-6761 • Internet: clc_apps@cc.com

CLC428 Electrical Characteristics (V_{CC} = ±5V; A_V = +2V/V; R_f =100Ω; R_g =100Ω; R_L = 100Ω; unless noted)

PARAMETERS	CONDITIONS	TYP	GUARANTEED MIN/MAX			UNITS	NOTES
Ambient Temperature	CLC428	+25°C	+25°C	0 to +70°C	-40 to +85°C		
FREQUENCY DOMAIN RESPONSE							
gain bandwidth product	V_{out} < 0.5V_{pp}	135	100	80	70	MHz	
-3dB bandwidth, Av=+1	V_{out} < 0.5V_{pp}	160	120	90	80	MHz	
Av=+2	V_{out} < 0.5V_{pp}	80	50	40	35	MHz	B,1
	V_{out} < 5.0V_{pp}	40	25	22	20	MHz	
gain flatness	V_{out} < 0.5V_{pp}						
peaking	DC to 200MHz	0.0	0.6	0.8	1.0	dB	B,1
rolloff	DC to 20MHz	0.05	0.5	0.7	0.7	dB	B,1
linear phase deviation	DC to 20MHz	0.2	1.0	1.5	1.5	°	
TIME DOMAIN RESPONSE							
rise and fall time	1V step	5.5	7.5	9.0	10.0	ns	
settling time	2V step to 0.1%	16	20	24	24	ns	
overshoot	1V step	1	5	10	10	%	
slew rate	5V step	500	300	275	250	V/µs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	1V_{pp},10MHz	- 62	- 50	- 45	- 43	dBc	B
3rd harmonic distortion	1V_{pp},10MHz	- 72	- 60	- 56	- 56	dBc	B
equivalent input noise							
voltage	1MHz to 100MHz	2.0	2.5	2.8	2.8	nV/√Hz	
current	1MHz to 100MHz	2.0	3.0	3.6	4.6	pA/√Hz	
crosstalk	input referred, 10MHz	- 62	- 58	- 58	- 58	dB	
STATIC DC PERFORMANCE							
open-loop gain		60	56	50	50	dB	
input offset voltage		1.0	2.0	3.0	3.5	mV	A
average drift		5	---	15	20	µV/°C	
input bias current		1.5	25	40	65	µA	A
average drift		150	---	600	700	nA/°C	
input offset current		0.3	3	5	5	µA	
average drift		5	---	25	50	nA/°C	
power supply rejection ratio		66	60	55	55	dB	B
common-mode rejection ratio		63	57	52	52	dB	
supply current	per channel, R_L= ∞	11	12	13	15	mA	A
MISCELLANEOUS PERFORMANCE							
input resistance	common-mode	500	250	125	125	kΩ	
	differential-mode	200	50	25	25	kΩ	
input capacitance	common-mode	2.0	3.0	3.0	3.0	pF	
	differential-mode	2.0	3.0	3.0	3.0	pF	
output resistance	closed loop	0.05	0.1	0.2	0.2	Ω	
output voltage range	R_L= ∞	± 3.8	± 3.5	± 3.3	± 3.3	V	
	R_L=100Ω	± 3.5	± 3.2	± 2.6	± 1.3	V	
input voltage range	common mode	± 3.7	± 3.5	± 3.3	± 3.3	V	
output current		± 80	± 50	± 40	± 20	mA	

Absolute Maximum Ratings

supply voltage	±7V
short circuit current	(note 2)
common-mode input voltage	±V_{cc}
differential input voltage	±10V
maximum junction temperature	+200°C
storage temperature	-65°C to+150°C
lead temperature (soldering 10 sec)	+300°C

Notes

A) J-level: spec is 100% tested at +25°C, sample tested at +85°C.
L-level: spec is 100% wafer probed at 25°C.

B) J-level: spec is sample tested at 25°C.
1) Spec is guaranteed at 0.5Vpp but tested at 0.1Vpp.
2) Output is short circuit protected to ground, however maximum reliability is obtained if output current does not exceed 200mA.

Ordering Information

Model	Temperature Range	Description
CLC428AJP	-40°C to +85°C	8-pin PDIP
CLC428AJE	-40°C to +85°C	8-pin SOIC
CLC428ALC	-40°C to +85°C	dice
CLC428A8B*	-55°C to +125°C	8-pin CerDIP, MIL-STD-883
CLC428AMC*	-55°C to +125°C	dice, MIL-STD-883
CLC428AIB*	-40°C to +85°C	8-pin CerDIP
5962-9470801MPA*	-55°C to +125°C	DESC SMD

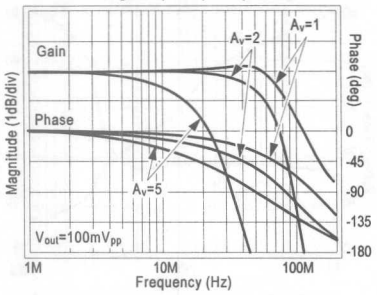
*See CLC428 MIL-883 Data Sheet for Specifications

Package Thermal Resistance

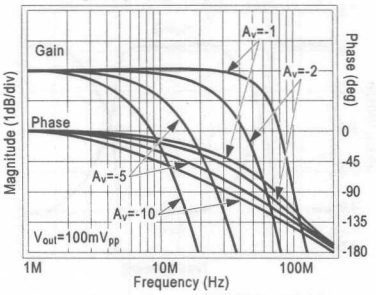
Package	θ_{jc}	θ_{jA}
Plastic (AJP)	75°/W	90°/W
Surface Mount (AJE)	90°/W	105°/W

CLC428 Typical Performance (T_A=+25°C, A_V=+2, V_{CC}=±5V, R_f=100Ω, R_L=100Ω, unless noted)

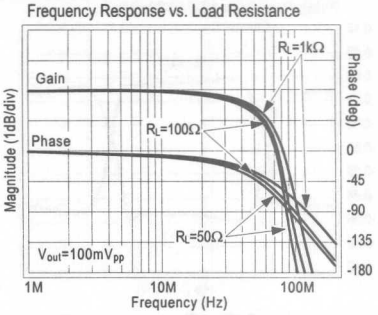
Non-Inverting Frequency Response



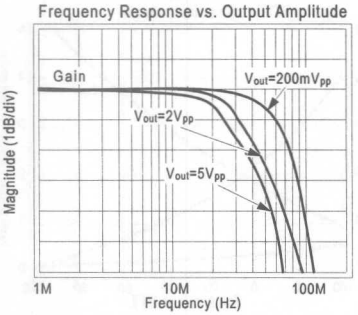
Inverting Frequency Response



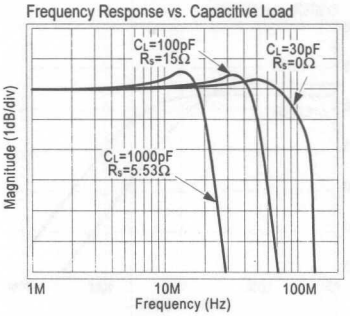
Frequency Response vs. Load Resistance



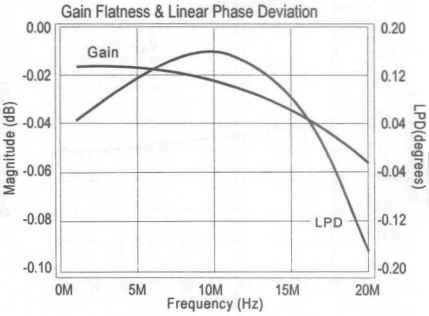
Frequency Response vs. Output Amplitude



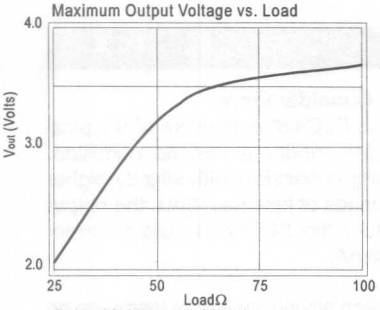
Frequency Response vs. Capacitive Load



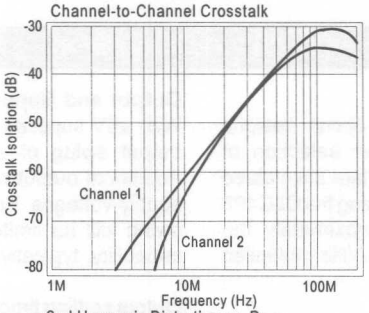
Gain Flatness & Linear Phase Deviation



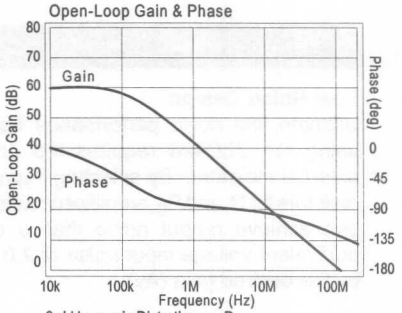
Maximum Output Voltage vs. Load



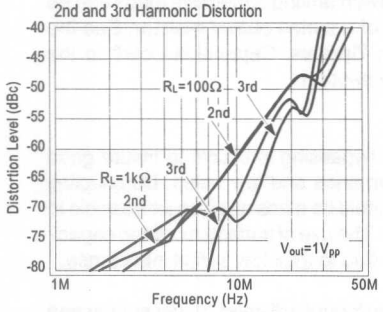
Channel-to-Channel Crosstalk



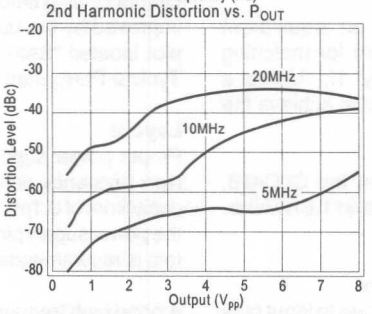
Open-Loop Gain & Phase



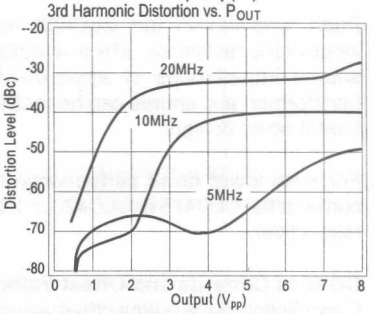
2nd and 3rd Harmonic Distortion



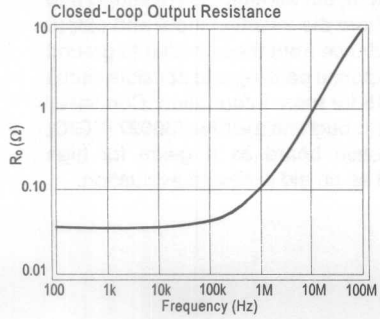
2nd Harmonic Distortion vs. P_{OUT}



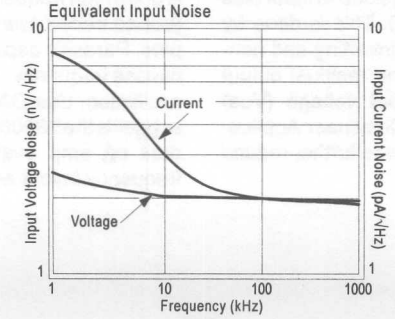
3rd Harmonic Distortion vs. P_{OUT}



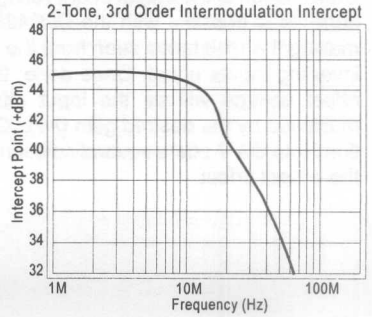
Closed-Loop Output Resistance



Equivalent Input Noise

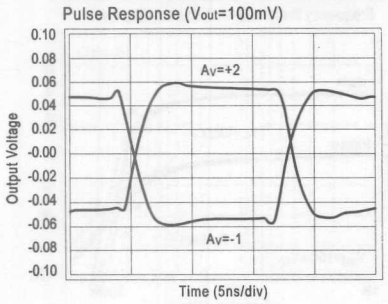


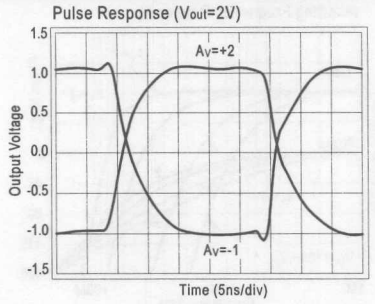
2-Tone, 3rd Order Intermodulation Intercept

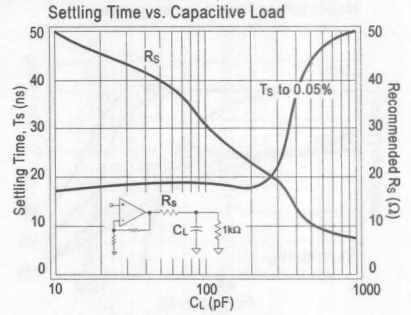


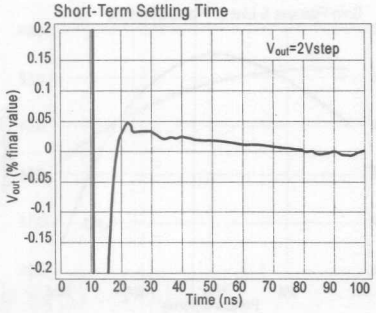
3

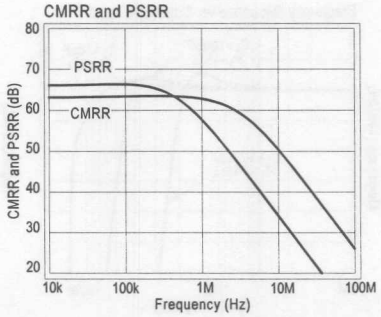
CLC428 Typical Performance (T_A=+25°C, A_V=+2, V_{CC}=±5V, R_f=100Ω, R_L=100Ω, unless noted)

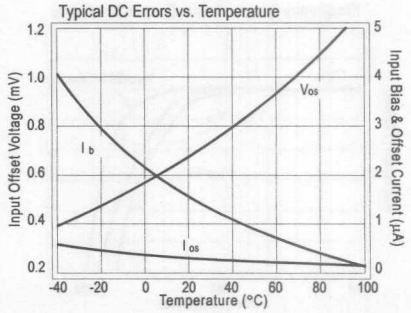












Application Discussion

Low Noise Design

Ultimate low noise performance from circuit designs using the CLC428 requires the proper selection of external resistors. By selecting appropriate low-valued resistors for R_f and R_g, amplifier circuits using the CLC428 can achieve output noise that is approximately the equivalent voltage input noise of 2.0 nV/√Hz multiplied by the desired gain (Av).

Each amplifier in the CLC428 has an equivalent input noise resistance which is optimum for matching source impedances of approximately 1k. Using a transformer, any source can be matched to achieve the lowest noise design.

For even lower noise performance than the CLC428, consider the CLC425 or CLC426 at 1.05 and 1.6 nV/√Hz, respectively.

DC Bias Currents and Offset Voltages

Cancellation of the output offset voltage due to input bias currents is possible with the CLC428. This is done by making the resistance seen from the inverting and non-inverting inputs equal. Once done, the residual output offset voltage will be the input offset voltage (Vos) multiplied by the desired gain (Av). Comlinear Application Note OA-7 offers several solutions to further reduce the output offset.

Output and Supply Considerations

With ±5V supplies, the CLC428 is capable of a typical output swing of ±3.8V under a no-load condition. Additional output swing is possible with slightly higher supply voltages. For loads of less than 50Ω, the output swing will be limited by the CLC428's output current capability, typically 80mA.

Output settling time when driving capacitive loads can be improved by the use of a series output resistor. See the plot labeled "Settling Time vs. Capacitive Load" in the Typical Performance section.

Layout

Proper power supply bypassing is critical to insure good high frequency performance and low noise. De-coupling capacitors of 0.1µF should be place as close as possible to the power supply pins. The use of surface mounted capacitors is recommended due to their low series inductance.

A good high frequency layout will keep power supply and ground traces away from the inverting input and output pins. Parasitic capacitance from these nodes to ground causes frequency response peaking and possible circuit oscillation. See OA-15 for more information. Comlinear suggests the 730036 (through-hole) or the 730027 (SOIC) dual op amp evaluation board as a guide for high frequency layout and as an aid in device evaluation.

Analog Delay Circuit (All-Pass Network)

The circuit in Figure 1 implements an all-pass network using the CLC428. A wide bandwidth buffer (CLC111) drives the circuit and provides a high input impedence for the source. As shown in Figure 2, the circuit provides a

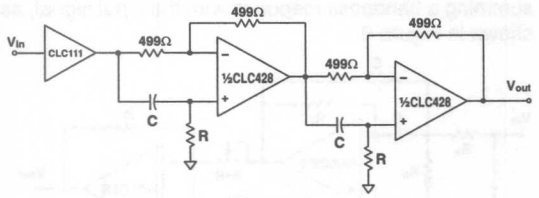


Figure 1

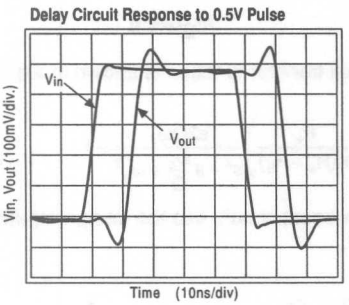


Figure 2

13.1ns delay (with R =40.2Ω, C=47pF). R_f and R_g should be of equal and low value for parasitic insensitive operation. The circuit gain is +1 and the delay is determined by the following equations.

$$\tau_{delay} = 2(2RC + T_d) \qquad \text{Eq. 1}$$

$$T_d = \frac{1}{360}\frac{d\phi}{df}; \qquad \text{Eq. 2}$$

where T_d is the delay of the op amp at A_V=+1. The CLC428 provides a typical delay of 2.8ns at its -3dB point.

Full Duplex Digital or Analog Transmission

Simultaneous transmission and reception of analog or digital signals over a single coaxial cable or twisted-pair line can reduce cabling requirements. The CLC428's wide bandwidth and high common-mode rejection in a differential amplifier configuration allows full duplex transmission of video, telephone, control and audio signals.

In the circuit shown in Figure 3, one of the CLC428's amps is used as a "driver" and the other as a difference "receiver" amplifier. The output impedance of the "driver" is essentially zero. The two R's are chosen to match the characteristic impedance of the transmission line. The "driver" op amp gain can be selected for unity or greater.

Receiver amplifier A_2 (B_2) is connected across R and forms differential amplifier for the signals transmitted by driver A_1 (B_1). If the coax cable is lossless and R_f equals R_g, receiver A_2 (B_2) will then reject the signals from driver

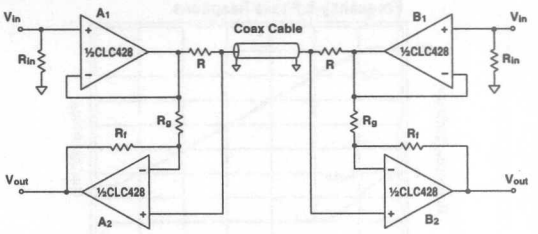


Figure 3

A_1 (B_1) and pass the signals from driver B_1 (A_1). The output of the receiver amplifier will be:

$$V_{out_{A(B)}} = \frac{1}{2}V_{in_{A(B)}}\left(1-\frac{R_f}{R_g}\right) + \frac{1}{2}V_{in_{B(A)}}\left(1+\frac{R_f}{R_g}\right) \qquad \text{Eq. 3}$$

Care must be given to layout and component placement to maintain a high frequency common-mode rejection. The plot of Figure 4 shows the simultaneous reception of signals transmitted at 1MHz and 10MHz.

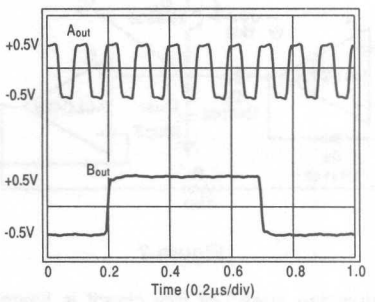


Figure 4

Five Decade Integrator

A composite integrator, as shown in Figure 5, uses the CLC428 dual op amp to increase the circuits' usable frequency range of operation. The transfer function of this circuit is:

$$V_o = \frac{1}{RC}\int V_{in}dt \qquad \text{Eq. 4}$$

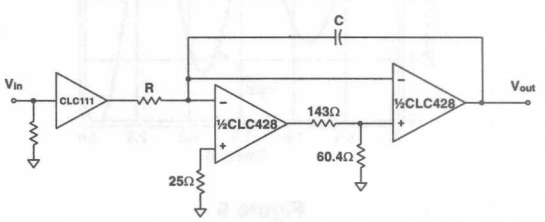


Figure 5

A resistive divider made from the 143Ω and 60.4Ω resistors was chosen to reduce the loop-gain and stabilize the network. The CLC428 composite integrator provides integration over five decades of operation. R and C set the integrator's gain. Figure 6 shows the frequency and phase response of the circuit in Figure 5 with R=44.2Ω and C=360pF.

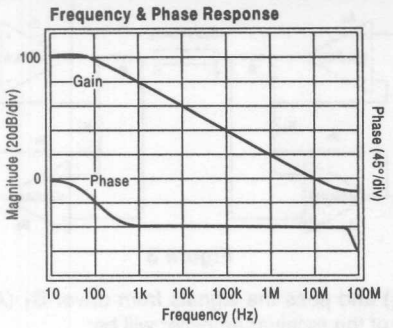


Figure 6

Positive Peak Detector

The CLC428's dual amplifiers can be used to implement a unity-gain peak detector circuit as shown in Figure 7.

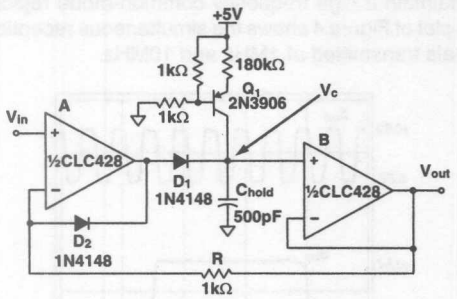


Figure 7

The acquisition speed of this circuit is limited by the dynamic resistance of the diode when charging C_{hold}. A plot of the of the circuit's performance is shown in Figure 8 with a 1MHz sinusoidal input.

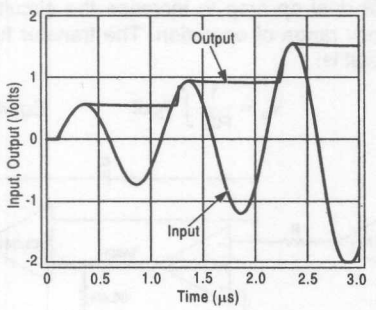


Figure 8

A current source, built around Q_1, provides the necessary bias current for the second amplifier and prevents saturation when power is applied. The resistor, R, closes the loop while diode D_2 prevents negative saturation when V_{in} is less than V_c. A MOS-type switch (not shown) can be used to reset the capacitor's voltage.

The maximum speed of detection is limited by the delay of the op amps and the diodes. The use of Schottky diodes will provide faster response.

Adjustable or Bandpass Equalizer

A "boost" equalizer can be made with the CLC428 by summing a bandpass response with the input signal, as shown in Figure 9.

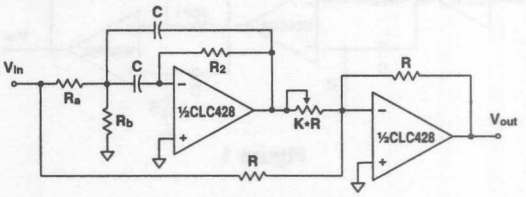


Figure 9

The overall transfer function is shown in Eq. 5.

$$\frac{V_{out}}{V_{in}} = \left(\frac{R_b}{K(R_a+R_b)}\right)\frac{s2Q\omega_o}{s^2+s\frac{\omega_o}{Q}+{\omega_o}^2} - 1 \qquad \text{Eq. 5}$$

To build a boost circuit, use the design equations Eq. 6 and Eq. 7.

$$\frac{R_2C}{2} = \frac{Q}{\omega_o}, \quad 2C(R_a \| R_b) = \frac{1}{Q\omega_o} \qquad \text{Eq. 6,7}$$

Select R_2 and C using Eq. 6. Use reasonable values for high frequency circuits - R_2 between 10Ω and 5kΩ, C between 10pF and 2000pF. Use Eq. 7 to determine the parallel combination of R_a and R_b. Select R_a and R_b by either the 10Ω to 5kΩ criteria or by other requirements based on the impedance V_{in} is capable of driving. Finish the design by determining the value of K from Eq. 8.

$$\text{Peak Gain} = \frac{V_{out}}{V_{in}}(\omega_o) = \frac{R_2}{2KR_a} - 1 \qquad \text{Eq. 8}$$

Figure 10 shows an example of the response of the circuit of Figure 9, where f_o is 2.3MHz. The component values are as follows: R_a =2.1kΩ, R_b =68.5Ω, R_2 =4.22kΩ, R =500Ω, KR =50Ω, C =120pF.

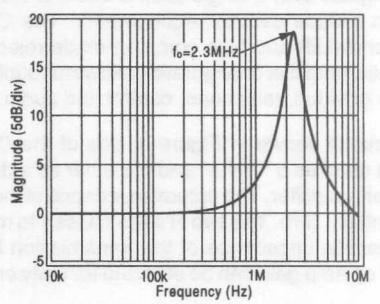


Figure 10

Comlinear
A National Semiconductor Company

General Purpose 100MHz Op Amp

CLC430

APPLICATIONS:

- Video Distribution
- CCD Clock Driver
- Multimedia Systems
- DAC Output Buffers
- Imaging Systems

FEATURES:

- 0.1dB Gain Flatness to 20MHz (Av=+2)
- 100MHz Bandwidth (Av=+1)
- 2000V/µs Slew Rate
- 0.03%/0.05° Differential Gain/Phase
- ±5V, ±15V or Single Supplies
- 100ns Disable to High-Impedance Output
- Wide Gain Range
- Low Cost

3

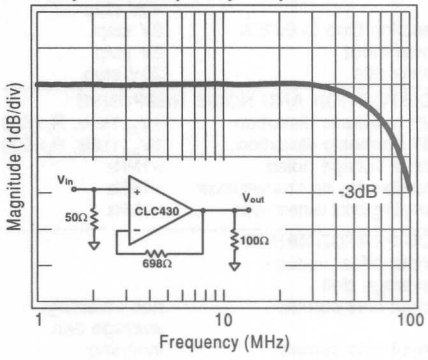
DESCRIPTION

The CLC430 is a low-cost, wideband monolithic amplifier for general purpose applications. The CLC430 utilizes Comlinear's patented current feedback circuit topology to provide an op amp with a slew rate of 2000V/µs, 100MHz unity-gain bandwidth and fast output disable function. Like all current feedback op amps, the CLC430 allows the frequency response to be optimized (or adjusted) by the selection of the feedback resistor. For demanding video applications, the 0.1dB bandwidth to 20MHz and differential gain/phase of 0.03%/0.05° make the CLC430 the preferred component for broadcast quality NTSC and PAL video systems.

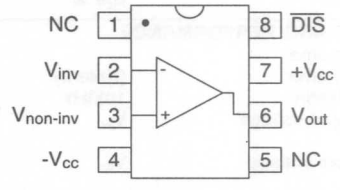
The large voltage swing ($28V_{pp}$), continuous output current (85mA) and slew rate (2000V/µs) provide high-fidelity signal conditioning for applications such as CCDs, transmission lines and low impedance circuits. Even driving loads of 100Ω, the CLC430 provides very low 2nd and 3rd harmonic distortion at 1MHz (-76/-82dBc).

Video distribution, multimedia and general purpose applications will benefit from the CLC430's wide bandwidth and disable feature. Power is reduced and the output becomes a high impedance when disabled. The wide gain range of the CLC430 makes this general purpose op amp an improved solution for circuits such as active filters, differential-to-single-ended drivers, DAC transimpedance amplifiers and MOSFET drivers.

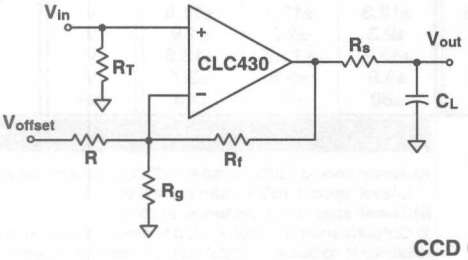
Unity-Gain Frequency Response



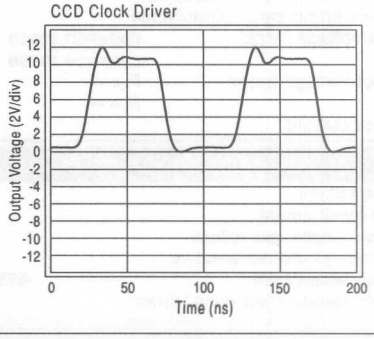
PINOUT
DIP & SOIC



TYPICAL APPLICATION



CCD Clock Driver



CLC430 Electrical Characteristics (V_{CC} = ±15V; A_V = +2V/V; R_f =604Ω; R_L = 100Ω; unless noted)

PARAMETERS	CONDITIONS	V_{CC}	TYP	GUARANTEED MIN/MAX			UNITS	NOTES
Ambient Temperature	CLC430		25°C	25°C	0 to 70°C	-40 to 85°C		
FREQUENCY DOMAIN RESPONSE								
unity-gain bandwidth	V_{out} < 1.0V_{pp}	±15	100				MHz	
small-signal bandwidth	V_{out} < 1.0V_{pp}	±15	75	50	45	42	MHz	
	V_{out} < 1.0V_{pp}	±5	55	35			MHz	
0.1dB bandwidth	V_{out} < 1.0V_{pp}	±15	20	7			MHz	
	V_{out} < 1.0V_{pp}	±5	16				MHz	
large-signal bandwidth	V_{out} = 10V_{pp}		30	22	20	19	MHz	
gain flatness	V_{out} < 1.0V_{pp}							
peaking	DC to 10MHz		0.0	0.1	0.2	0.2	dB	
rolloff	DC to 20MHz		0.1	0.7	1.0	1.2	dB	
linear phase deviation	DC to 20MHz		0.5	1.8	2.0	2.1	°	
differential gain	4.43MHz, R_L=150Ω	±15	0.03	0.05	0.06	0.06	%	
	4.43MHz, R_L=150Ω	±5	0.03	0.05			%	
differential phase	4.43MHz, R_L=150Ω	±15	0.05	0.09	0.12	0.13	°	
	4.43MHz, R_L=150Ω	±5	0.09	0.19			°	
TIME DOMAIN RESPONSE								
rise and fall time	2V step		5	7	7	7	ns	
	10V step		10	14	14	14	ns	
settling time to 0.05%	2V step		35	50	55	55	ns	
overshoot	2V step		5	15	15	15	%	
slew rate	20V step		2000	1500	1450	1450	V/µs	
DISTORTION AND NOISE RESPONSE								
2nd harmonic distortion	1V_{pp}, 1MHz, R_L=500		-89				dBc	
3rd harmonic distortion	1V_{pp}, 1MHz, R_L=500		-92				dBc	
input voltage noise	>1MHz		3.0	3.5	3.7	3.8	nV/√Hz	
non-inverting input current noise	>1MHz		3.2	6.0	6.3	6.8	pA/√Hz	
inverting input current noise	>1MHz		15	18	20	21	pA/√Hz	
DC PERFORMANCE								
input offset voltage		±15	1.0	7.5	9.0	10.0	mV	A
average drift			25	---	50	50	µV/ C	
input bias current	non-inverting	±15,±5	3	14	16	20	µA	A
	average drift		10	---	100	100	nA/°C	
input bias current	inverting	±15,±5	3	14	15	17	µA	A
average drift			10	---	60	90	nA/°C	
power-supply rejection ratio	DC		62	56	54	53	dB	B
common-mode rejection ratio	DC		62	54	53	52	dB	
supply current	R_L= ∞	±15,±5	11, 8.5	12	13	14.5	mA	A
disabled	R_L= ∞	±15,±5	1.5	2.0	2.2	2.4	mA	A
SWITCHING PERFORMANCE								
turn on time			200	300	320	340	ns	
turn off time	(Note 2)		100	200	200	200	ns	
off isolation	10MHz		59	56	56	56	dB	
high input voltage	V_{IH}	±15	11.8	12.5	12.7		V	
		±5	1.8	2.5	2.7		V	
low input voltage	V_{IL}	±15	10.8	10.5	10.0		V	
		±5	0.8	0.6	0.1		V	
MISCELLANEOUS PERFORMANCE								
Non-inverting input resistance			8.0	3.0	2.5	1.7	MΩ	
Non-inverting input capacitance				0.5	1.0	1.0	1.0	pF
input voltage range	common mode	±15	±12.5	±12.3	±12.1	±11.8	V	
	common mode	±5	±2.5	±2.3	±2.2	±1.9	V	
output voltage range	R_L= ∞	±15	±14	±13.7	±13.7	±13.6	V	
	R_L= ∞	±5	±4.0	±3.9	±3.8	±3.7	V	
output current			±85	±60	±50	±45	mA	

Absolute Maximum Ratings

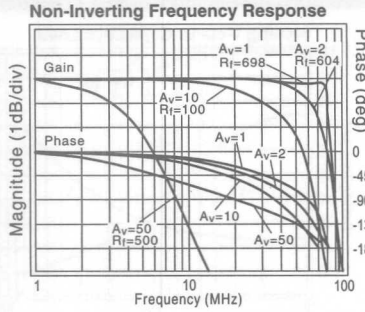
supply voltage	±16.5V
short circuit current	(note 1)
common-mode input voltage	±V_{cc}
maximum junction temperature	+200°C
storage temperature	-65°C to+150°C
lead temperature (soldering 10 sec)	+300°C

Notes

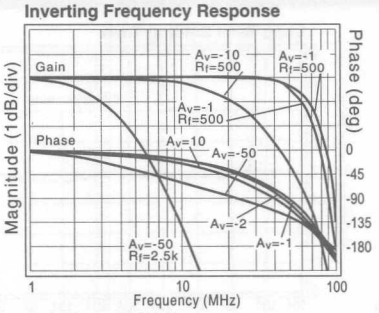
A) J-level: spec is 100% tested at +25°C, sample tested at +85°C.
L-level: spec is 100% wafer probed at 25°C.
B) J-level: spec is sample tested at 25°C.
1) Output is short circuit protected to ground, however maximum reliability is obtained if output current does not exceed 125mA.
2) To>50dB attenuation @ 10MHz.

CLC430 Typical Performance (V_{CC} = ±15V; A_V = +2V/V; R_f =604Ω; R_L = 100Ω; unless noted)

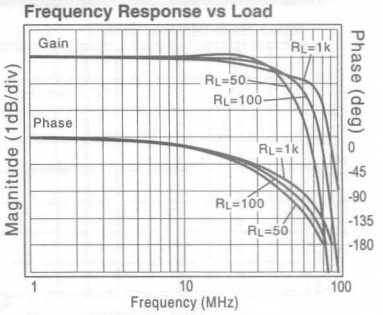
Non-Inverting Frequency Response



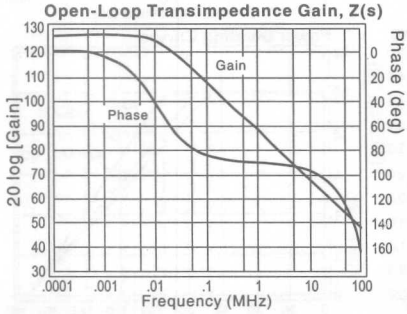
Inverting Frequency Response



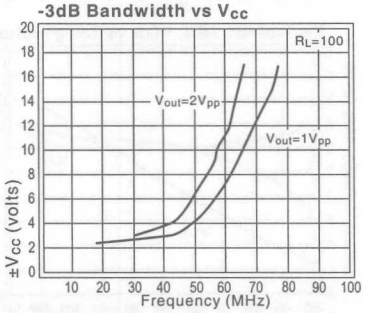
Frequency Response vs Load



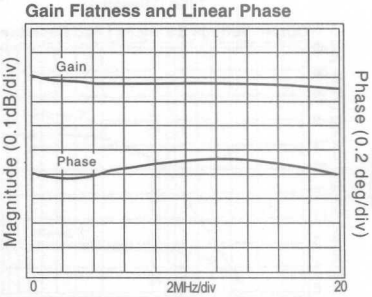
Open-Loop Transimpedance Gain, Z(s)



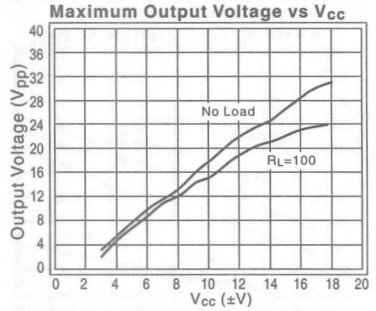
-3dB Bandwidth vs V_{CC}



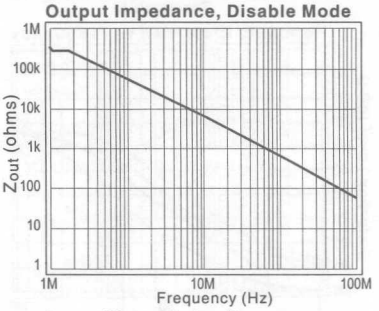
Gain Flatness and Linear Phase



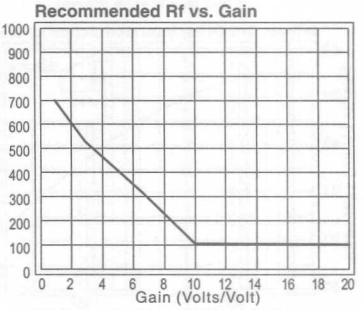
Maximum Output Voltage vs V_{CC}



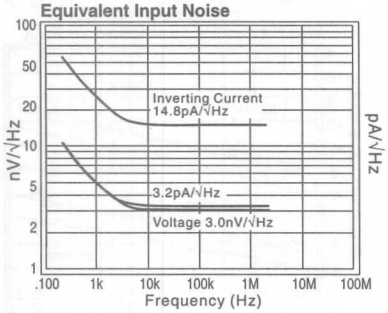
Output Impedance, Disable Mode



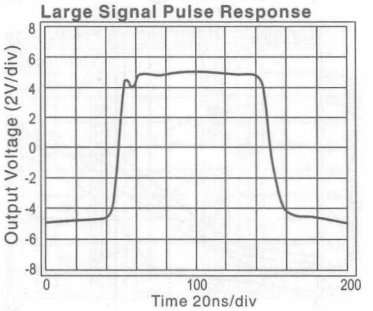
Recommended Rf vs. Gain



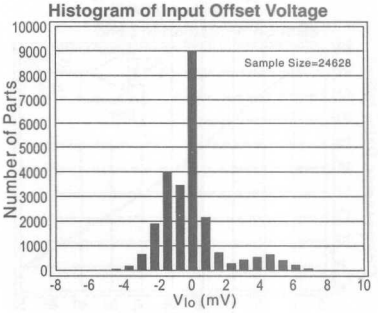
Equivalent Input Noise



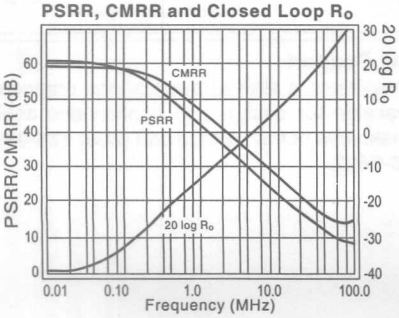
Large Signal Pulse Response



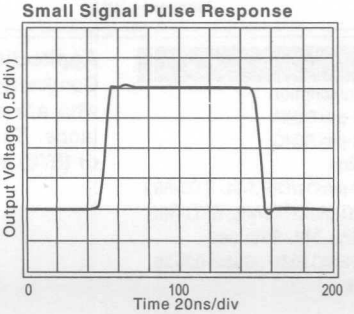
Histogram of Input Offset Voltage



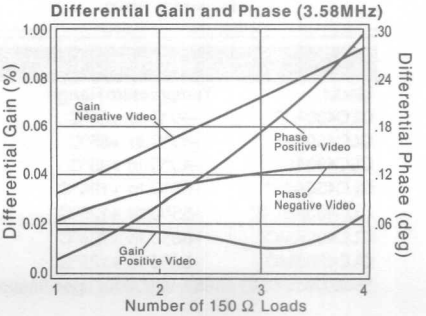
PSRR, CMRR and Closed Loop R_o



Small Signal Pulse Response

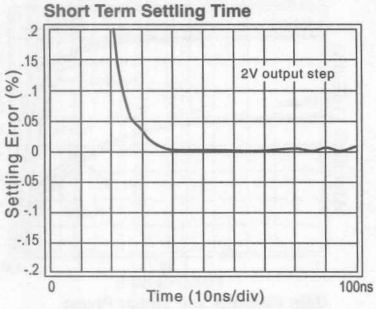


Differential Gain and Phase (3.58MHz)

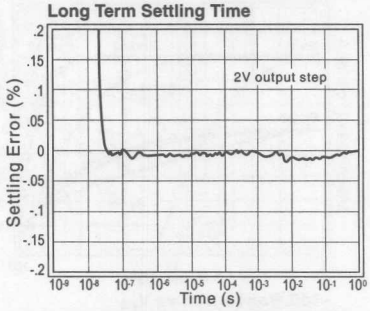


CLC430 Typical Performance (V_{CC} = ±15V; A_V = +2V/V; R_f =604Ω; R_L = 100Ω; unless noted)

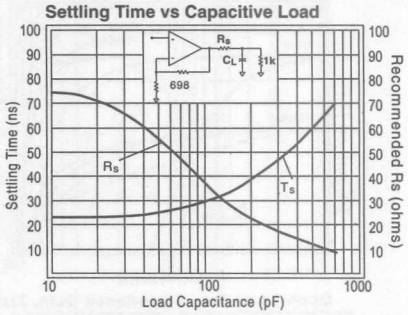
Short Term Settling Time



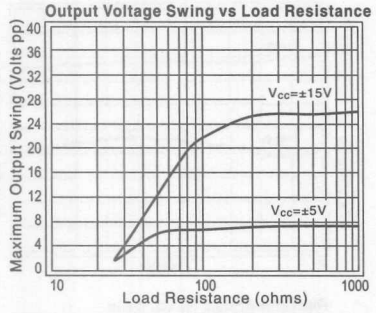
Long Term Settling Time



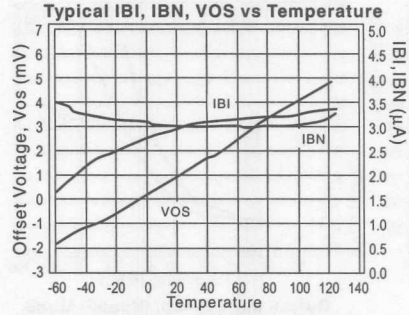
Settling Time vs Capacitive Load



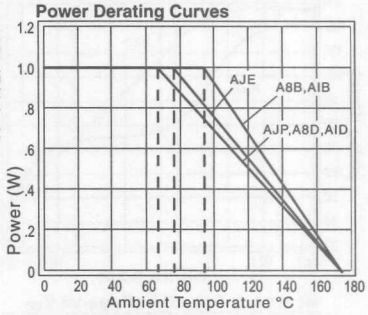
Output Voltage Swing vs Load Resistance



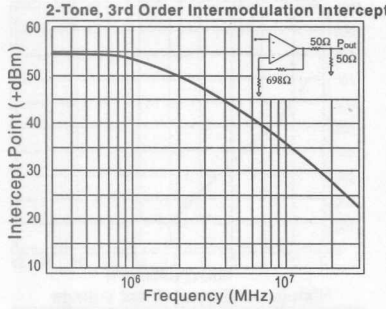
Typical IBI, IBN, VOS vs Temperature



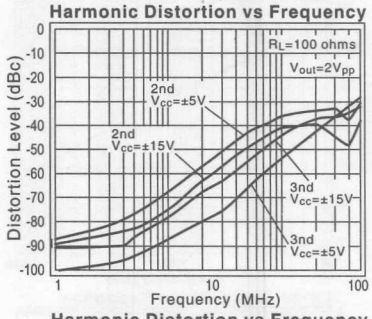
Power Derating Curves



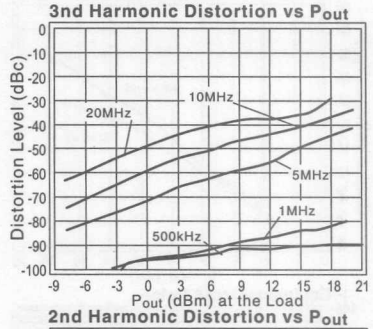
2-Tone, 3rd Order Intermodulation Intercept



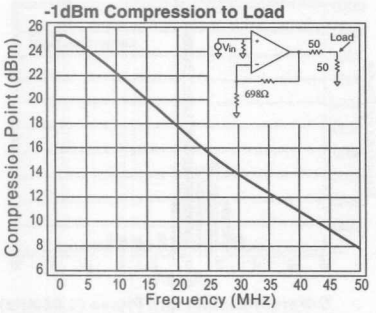
Harmonic Distortion vs Frequency



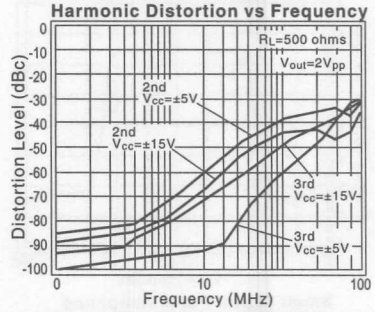
3nd Harmonic Distortion vs Pout



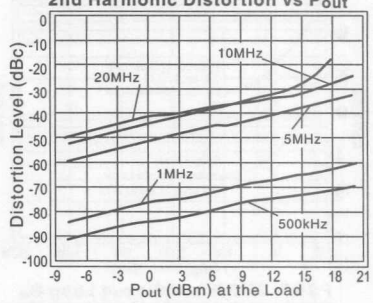
-1dBm Compression to Load



Harmonic Distortion vs Frequency



2nd Harmonic Distortion vs Pout



Ordering Information

Model	Temperature Range	Description
CLC430AJP	-40°C to +85°C	8-pin PDIP
CLC430AJE	-40°C to +85°C	8-pin SOIC
CLC430ALC	-40°C to +85°C	dice
CLC430A8B*	-55°C to +125°C	8-pin CerDIP, MIL-STD-883
CLC430A8L-2*	-55°C to +125°C	20-pin LCC, MIL-STD-883
CLC430AMC*	-55°C to +125°C	dice, MIL-STD-883
CLC430SMD	-55°C to +125°C	DESC SMD #5962-92030

*See Desc SMD #5962-92030 for specifications

Applications Support

Comlinear maintains a staff of applications engineers who are available for design and applications assistance. To make use of this service **call (800) 776-0500 or (970) 255-7422.**

General Design Considerations

The CLC430 is a general purpose current-feedback amplifier for use in a variety of small- and large-signal applications. Use the feedback resistor to fine tune the gain flatness and -3dB bandwidth for any gain setting. Comlinear provides information for the performance at a gain of +2 for small and large signal bandwidths. The plots show feedback resistor values for selected gains.

Gain

Use the following equations to set the CLC430's non-inverting or inverting gain:

$$\text{Non-Inverting Gain} = 1+\frac{R_f}{R_g}$$

$$\text{Inverting Gain} = -\frac{R_f}{R_g}$$

Choose the resistor values for non-inverting or inverting gain by the following steps.

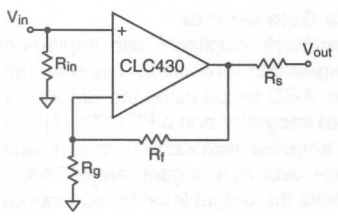


Fig. 0 Component Identification

1) Select the recommended feedback resistor R_f (refer to plot in the plot section entitled *R_f vs Gain*).
2) Choose the value of R_g to set gain.
3) Select R_s to set the circuit output impedance.
4) Select R_{in} for input impedance and input bias.

High Gains

Current feedback closed-loop bandwidth is independent of gain-bandwidth-product for small gain changes. For larger gain changes the optimum feedback register R_f is derived by the following:

$$R_f = 724\Omega - 60\Omega \cdot (Av)$$

As gain is increased, the feedback resistor allows bandwidth to be held constant over a wide gain range. For a more complete explanation refer to application note OA-25 Stability Analysis of Current-Feedback Amplifiers.

Resistors have varying parasitics that affect circuit performance in high-speed design. For best results, use leaded metal-film resistors or surface mount resistors. A SPICE model for the CLC430 is available to simulate overall circuit performance.

Enable / Disable Function

The CLC430 amplifier features an enable/disable function that changes the output and inverting input from low to high impedance. The pin 8 enable/disable logic levels are as follows:

V_{cc}	±15V	±5V
Enable	>12.7V	>2.7V
Disable	<10.0V	<0.8V

The amplifier is enabled with pin 8 left open due to the 2kΩ pull-up resistor, shown in Fig. 1.

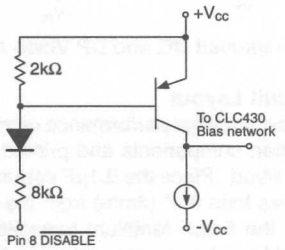


Fig. 1 Pin 8 Equivalent Disable Circuit

Open-collector or CMOS interfaces are recommended to drive pin 8. The turn-on and off time depends on the speed of the digital interface.

The equivalent output impedance when disabled is shown in Fig. 2. With R_g connected to ground, the sum of R_f and R_g dominates and reduces the disabled output impedance. To raise the output impedance in the disabled state, connect the CLC430 as a unity-gain voltage follower by removing R_g. Current-feedback op-amps need the recommended R_f in a unity-gain follower circuit. For high density circuit layouts consider using the dual CLC431 (with disable) or the dual CLC432 (without disable).

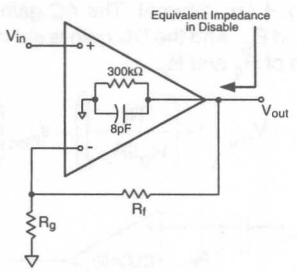


Fig. 2 Equivalent Disabled Output Impedance

2nd and 3rd Harmonic Distortion

To meet low distortion requirements, recognize the effect of the feedback resistor. Increasing the feedback resistor will decrease the loop gain and increase distortion. Decreasing the load impedance increases 3rd harmonic distortion more than 2nd.

Differential Gain and Differential Phase

The CLC430 has low DG and DP errors for video applications. Add an external pulldown resistor to the CLC430's output to improve DG and DP as seen in Fig.3. A 604Ω R_P will improve DG and DP to 0.01% and 0.02°.

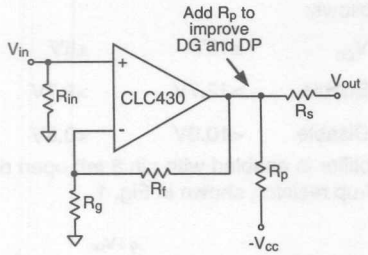


Fig. 3 Improved DG and DP Video Amplifier

Printed Circuit Layout

To get the best amplifier performance careful placement of the amplifier, components and printed circuit traces must be observed. Place the 0.1µF ceramic decoupling capacitors less than 0.1" (3mm) from the power supply pins. Place the 6.8µF tantalum capacitors less than 0.75" (20mm) from the power supply pins. Shorten traces between the inverting pin and components to less than 0.25" (6mm). Clear ground plane 0.1" (3mm) away from pads and traces that connect to the inverting, non-inverting and output pins. Do not place ground or power plane beneath the op-amp package. Comlinear provides literature and evaluation boards 730013 DIP or 730027 SOIC illustrating the recommended op-amp layout.

Applications Circuits

Level Shifting

The circuit shown in Fig. 4 implements level shifting by AC coupling the input signal and summing a DC voltage. The resistor R_{in} and the capacitor C set the high-pass break frequency. The amplifier closed-loop bandwidth is fixed by the selection of R_f. The DC and AC gains for circuit of Fig. 4 are different. The AC gain is set by the ratio of R_f and R_g. And the DC gain is set by the parallel combination of R_g and R_2.

$$V_{out} = V_{in_{AC}}\left(1+\left(\frac{R_f}{R_g \| R_2}\right)\right) - V_{in_{DC}}\left(\frac{R_f}{R_2}\right)$$

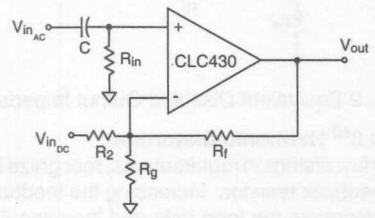


Fig. 4 Level Shifting Circuit

Multiplexing

Multiple signal switching is easily handled with the disable function of the CLC430. Board trace capacitance at the output pin will affect the frequency response and switching transients. To lessen the effects of output capacitance place a resistor (R_o) within the feedback loop to isolate the outputs as shown in Fig. 5. To match the mux output impedance to a transmission line, add a resistor (R_s) in series with the output.

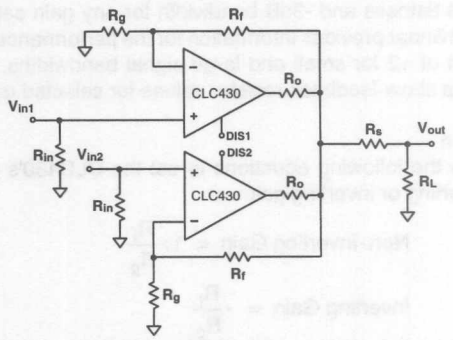
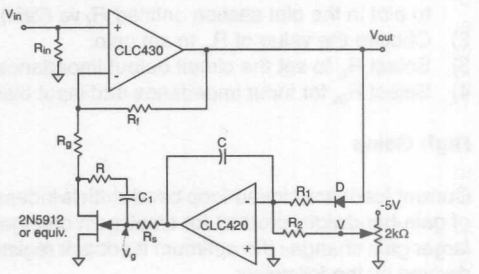


Fig. 5 Output Connection

Automatic Gain Control

Current-feedback amplifiers can implement very fast automatic-gain control circuits. The circuit shown in Fig. 6 shows an AGC circuit using the CLC430, a half-wave rectifier, an integrator and a FET. The CLC430 current-feedback amplifier maintains constant bandwidth and linear phase over AGC's gain range. This circuit effectively controls the output level for continuous signals.

Fig. 6 AGC Circuit



The bandwidth of the CLC430 AGC is limited by R_f, the feedback resistor. The FET gate voltage is limited to a range of:

$$-2.5 < V_g < -1$$

R of 750Ω and C1 of 1.0µF gives a useful R_{ds} range of approximately 150 to 2K ohms. Scaling the integrator gain or adding attenuation before the diode D accommodates large signal swings. Determine the overall gain by:

$$1+\frac{R_f}{R_g+R_{ds}}$$

The integrator sets the loop time constant.

Comlinear
A National Semiconductor Company

Dual Wideband Monolithic Op Amps

CLC431 and CLC432

APPLICATIONS:

- Video Signal Multiplexing
- Twisted-Pair Differential Driver
- CCD Buffer & Level Shifting
- Discrete Gain-Select Amplifier
- Transimpedance Amplifier

FEATURES:

- Wide Bandwidth: 92MHz (A_V=+1)
  62MHz (A_V=+2)
- Fast Slew Rate: 2000V/µs
- Fast Disable: 1µs to high-Z output
- High Channel Isolation: 70dB at 10MHz
- Single or Dual Supplies: ±5V to ±16.5V

DESCRIPTION

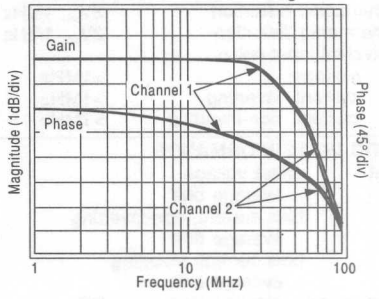
The CLC431 and CLC432 current-feedback amplifiers provide wide bandwidths and high slew rates for applications where board density and power are key considerations. These amplifiers provide dc-coupled small signal bandwidths exceeding 92MHz while consuming only 7mA per channel. Operating from ±15V supplies, the CLC431/432's enhanced slew rate circuitry delivers large-signal bandwidths with output voltage swings up to $28V_{pp}$. A wide range of bandwidth-insensitive gains are made possible by virtue of the CLC431 and CLC432's current-feedback topology.

The large common-mode input range and fast settling time (70ns to 0.05%) make these amplifiers well suited for CCD & data telecommunication applications. The disable of the CLC431 can accommodate ECL or TTL logic levels or a wide range of user definable inputs. With its fast enable/disable time (0.2µs/1µs) and high channel isolation of 70dB at 10MHz, the CLC431 can easily be configured as a 2:1 MUX. Many high performance video applications requiring signal gain and/or switching will be satisfied with the CLC431/432 due to their very low differential gain and phase errors (less than 0.1% and 0.1°; A_V=+2V/V at 4.43MHz into 150Ω load).

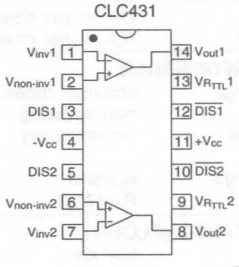
Quick 8ns rise and fall times on 10V pulses allow the CLC431/432 to drive either twisted pair or coaxial transmission lines over long distances.

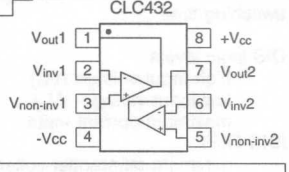
The CLC431/432's combination of low input voltage noise, wide common-mode input voltage range and large output voltage swings make them especially well suited for wide dynamic range signal processing applications.

CLC431/CLC432 Channel Matching

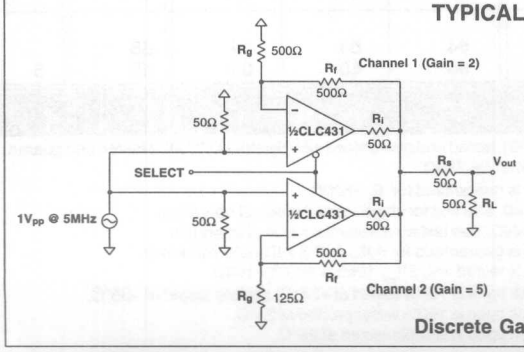


PINOUT
PDIP & SOIC



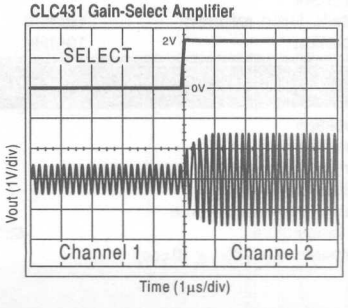


TYPICAL APPLICATION



Discrete Gain Select Amplifier

CLC431 Gain-Select Amplifier



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CLC431/432 Electrical Characteristics (V_{CC} = ±15V; A_V= +2; R_f = R_g =750Ω; R_L = 100Ω; unless noted)

PARAMETERS	CONDITIONS	TYP	GUARANTEED MIN/MAX			UNITS	NOTES
Ambient Temperature	CLC431 & CLC432	+25	+25	0 to +70	-40 to +85	°C	1
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth	V_{out} < 4.0V_{pp}	62	42	37	36	MHz	B
V_{CC}=±5V	V_{out} < 4.0V_{pp}	62				MHz	
	V_{out} < 10V_{pp}	28	21	20	20	MHz	2
gain flatness	V_{out} < 4.0V_{pp}						
peaking	DC to 100MHz	0.05	0.5	0.7	0.7	dB	B
rolloff	DC to 20MHz	0.0	0.8	0.8	0.8	dB	B
linear phase deviation	DC to 30MHz	0.3	1.8	2.0	2.1	°	
differential gain	4.43MHz, R_L=150Ω	0.12	0.18	0.2	0.2	%	
differential phase	4.43MHz, R_L=150Ω	0.12	0.18	0.23	0.25	°	
TIME DOMAIN RESPONSE							
rise and fall time	10V step	8	12	13	13	ns	2
overshoot	2V step	5	10	12	12	%	
settling time	2V step to 0.05%	70	100	110	110	ns	
slew rate	V_{out} = ±10V	2000	1500	1450	1400	V/µs	2
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 1MHz	- 65				dBc	6
3rd harmonic distortion	2V_{pp}, 1MHz	- 75				dBc	6
equivalent input noise							
voltage	>1MHz	3.3	4.2	4.4	4.5	nV/√Hz	
current, inverting	>1MHz	13	16	17	18	pA/√Hz	
current, non-inverting	>1MHz	2.0	2.5	2.6	2.8	pA/√Hz	
STATIC DC PERFORMANCE							
input offset voltage		3	6	7	7	mV	A
average drift		20	---	50	50	µV/°C	
bias current, non-inverting		2	8	10	16	µA	A
average drift		25	---	100	150	nA/°C	
bias current, inverting		2	6	6	8	µA	A
average drift		8	---	25	40	nA/°C	
power supply rejection ratio	DC	64	59	59	59	dB	B
common-mode rejection ratio	DC	63	58	57	56	dB	
supply current	R_L= ∞, per channel	7.1	7.9	8.5	9.6	mA	A
CLC431 disabled	R_L= ∞, per channel	0.8	1.2	1.3	1.45	mA	A
MISCELLANEOUS PERFORMANCE							
input voltage range	common mode	± 12.2	± 12.0	± 11.8	± 11.6	V	
resistance	non-inverting	24	16	10	6	MΩ	
capacitance	non-inverting	0.5	1	1	1	pF	
output current		± 60	± 38	± 35	± 30	mA	
voltage range	R_L≥5kΩ	± 14.0	± 13.6	± 13.4	± 13.2	V	
	R_L=100Ω	± 6.0	± 3.7	± 3.7	± 2.9	V	
SWITCHING PERFORMANCE (CLC431)							
switching time	turn on	0.1	0.15	0.155	0.165	µs	
	turn off	0.7	1.0	1.2	1.2	µs	
DIS logic levels	single-ended mode						3
high input voltage (V_{IH})		> 2.0	> 2.0	> 2.0	> 2.0	V	
low input voltage (V_{IL})		< 0.8	< 0.8	< 0.8	< 0.8	V	
maximum current input	V_{IH} > DIS > V_{IL}	150	180	190	205	µA	
IDIS-$\overline{DIS}$I	differential mode						4
minimum differential voltage		0.3	0.4	0.4	0.4	V	
ISOLATION							
crosstalk, input referred	10MHz	70	64	64	64	dB	
off isolation	10MHz	64	60	60	60	dB	5

Absolute Maximum Ratings

supply voltage	±16.5V
short circuit current	100mA
common-mode input voltage	±V_{cc}
differential input voltage	±10V
maximum junction temperature	+200°C
storage temperature	-65°C to+150°C
lead temperature (soldering 10 sec)	+300°C

Notes

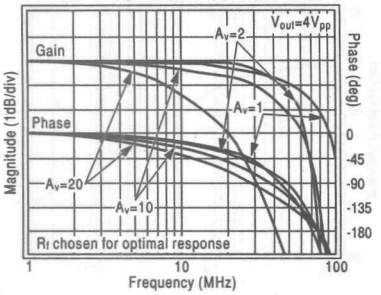
1) CLC431 tested and guaranteed with R_f=866Ω.CLC432 tested and guaranteed with R_f=750Ω.
2) Spec is guaranteed for R_L≥500Ω.
3) V_{RTTL}=0, See text for single-ended mode of operation.
4) V_{RTTL}=NC, See text for differential mode of operation
5) Spec is guaranteed for AJE; AJP & AIB yield 7dB lower.
6) Spec is tested with 2V_{pp}, 10MHz and R_L=100Ω.

A) J-level: spec is 100% tested at +25°C, sample tested at +85°C.
L-level: spec is 100% wafer probed at 25°C.

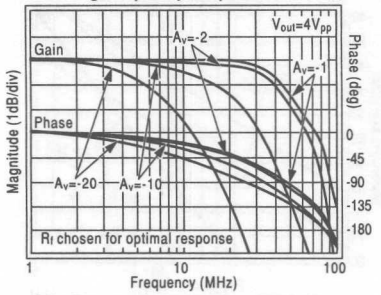
B) J-level: spec is sample tested at 25°C.

CLC431/432 Typical Performance Characteristics (T_A=+25°C, A_V=+2, V_{CC}=±15V, unless noted)

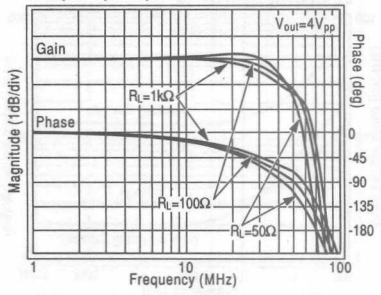
Non-Inverting Frequency Response



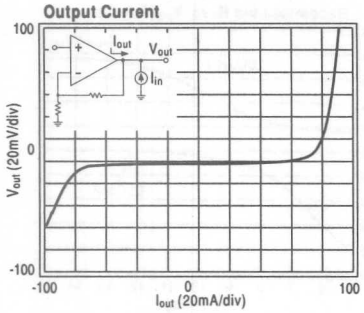
Inverting Frequency Response



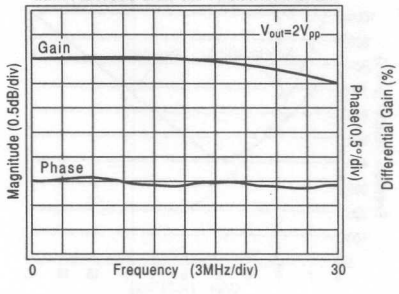
Frequency Response vs. Load Resistance



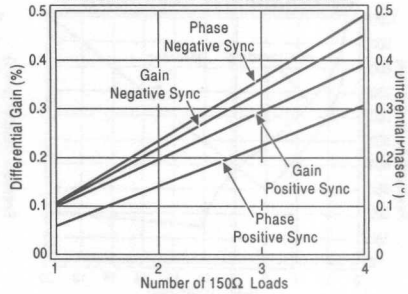
Output Current



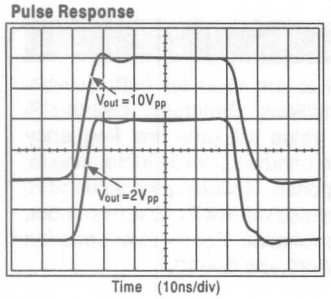
Gain Flatness & Linear Phase Deviation



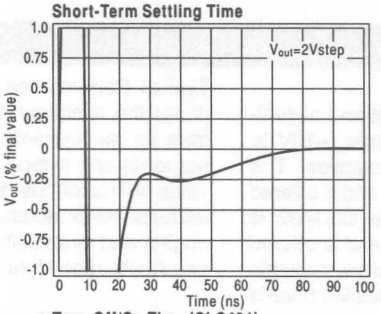
Differential Gain and Phase at 3.58MHz



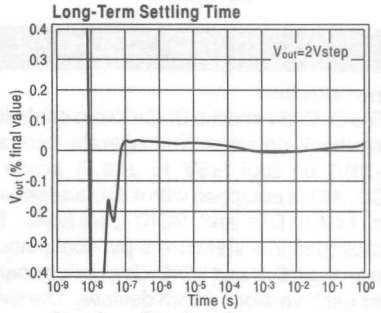
Pulse Response



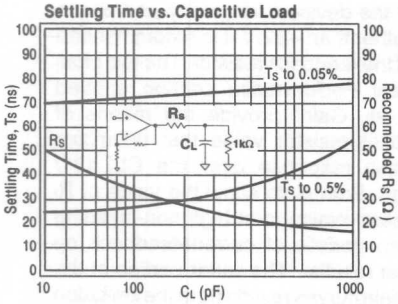
Short-Term Settling Time



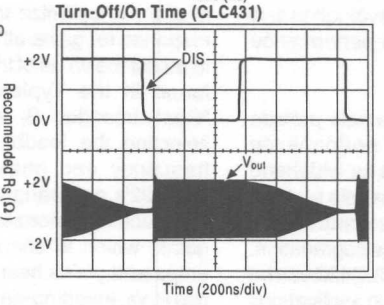
Long-Term Settling Time



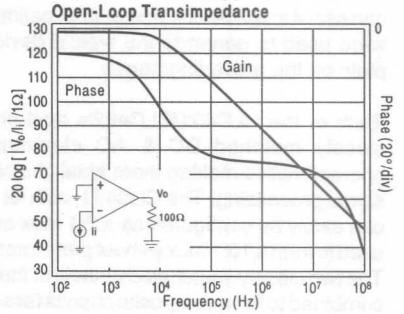
Settling Time vs. Capacitive Load



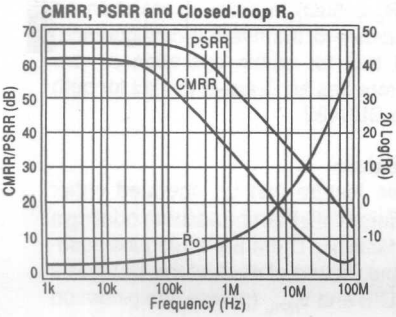
Turn-Off/On Time (CLC431)



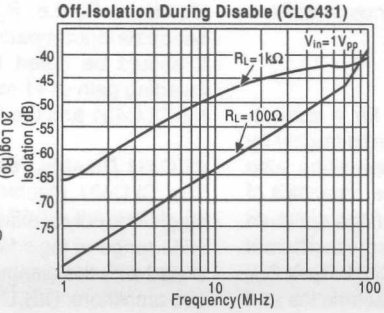
Open-Loop Transimpedance



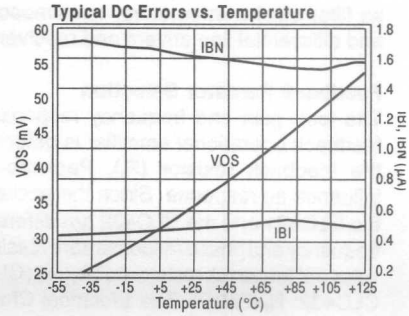
CMRR, PSRR and Closed-loop R_o



Off-Isolation During Disable (CLC431)

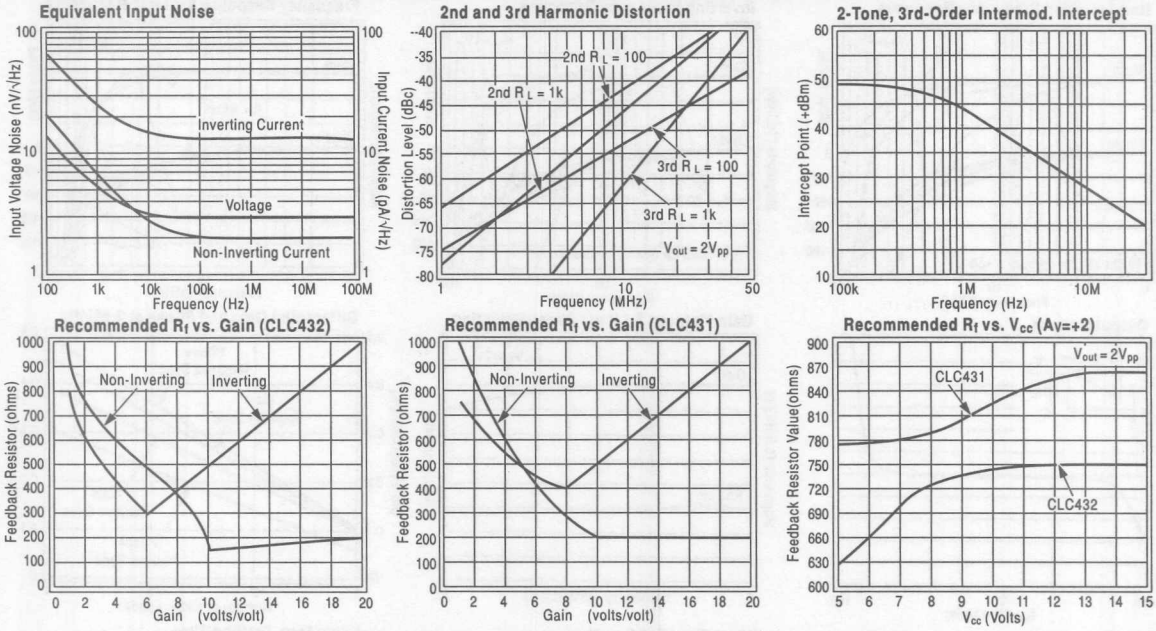


Typical DC Errors vs. Temperature



3

CLC431/432 Typical Performance Characteristics (T_A=+25°C, A_V=+2, V_{CC}=±15V, unless noted)



Application Discussion

Introduction

The CLC431 and the CLC432 are dual wideband current-feedback op amps that operate from single (+10V to +33V) or dual (±5V to ±16.5) power supplies. The CLC431 is equipped with a disable feature and is offered in 14-pin DIP and SOIC packages. The CLC432 is packaged in a standard 8-pin dual pinout and is offered in an 8-pin DIP and SOIC. Evaluation boards are available for each version of both devices. The evaluation boards can assist in the device and/or application evaluation and were used to generate the typical device performance plots on the preceding pages.

Each of the CLC431/CLC432's dual channels provide closely matched DC & AC electrical performance characteristics making them ideal choices for wideband signal processing. The CLC431, with its disable feature, can easily be configured as a 2:1 mux or several can be used to form a 10:1 mux without performance degradation. The two closely-matched channels of the CLC432 can be combined to form composite circuits for such applications as filter blocks, integrators, transimpedance amplifiers and differential line drivers and receivers.

Feedback Resistor Selection

The loop gain and frequency response for a current-feedback operational amplifier is determined largely by the feedback resistor (R_f). Package parasitics also influence ac response. Since the package parasitics of the CLC431 and the CLC432 are different, the optimum frequency and phase responses are obtained with different values of feedback resistor (for A_V=+2; CLC431: R_f=866Ω, CLC432: R_f=750Ω). The Electrical Characteristics and Typical Performance plots are valid for both devices under the specified conditions. Generally, lowering R_f from its recommended value will peak the frequency response and extend the bandwidth while increasing its value will roll off the response. Reducing the value of R_f too far below its recommended value will cause overshoot, ringing and eventually oscillation. For more information see Application Note OA-20 and OA-13.

In order to optimize the devices' frequency and phase response for gains other than +2V/V it is recommended to adjust the value of the feedback resistor. The two plots found in the Typical Performance section entitled "Recommended R_f vs. Gain" provide the means of selecting the feedback-resistor value that optimizes frequency and phase response over the CLC431/CLC432's gain range. Both plots show the value of R_f approaching a nonzero minimum at high non-inverting gains, which is characteristic of current-feedback op amps and yields best results. The linear portion of the two R_f vs. Inverting-gain curves results from the limitation placed on R_g (i.e. $R_g \geq 50\Omega$) in order to maintain an adequate input impedance for the inverting configuration. It should be noted that for stable operation a non-inverting gain of +1 requires an R_f equal to 1kΩ for both the CLC431 and the CLC432.

CLC431 Disable Feature

The CLC431 disable feature can be operated either single-endedly or differentially thereby accommodating a wide range of logic families. There are three pins associated with the disable feature of each of the CLC431's two amplifiers: DIS, $\overline{DIS}$ and V_{RTTL} (please see pinout on

front page). Also note that both amplifiers are guaranteed to be enabled if all three of these pins are unconnected.

Fig. 1 illustrates the single-ended mode of the CLC431's disable feature for logic families such as TTL and CMOS. In order to operate properly, V_{RTTL} must be grounded, thereby biasing $\overline{DIS}$ to approximately +1.4V through the two internal series diodes. For single-ended operation, $\overline{DIS}$ should be left floating. Applying a TTL or CMOS logic "high" (i.e. >2.0Volts) to DIS will switch the tail current of the differential pair to Q1 and "shut down" Q2 which results in the *disabling* of that channel of the CLC431. Alternatively, applying a logic "low" (i.e. <0.8Volts) to DIS will switch the tail current from Q1 to Q2 effectively *enabling* that channel. If DIS is left floating under single-ended operation, then the associated amplifier is guaranteed to be *disabled*.

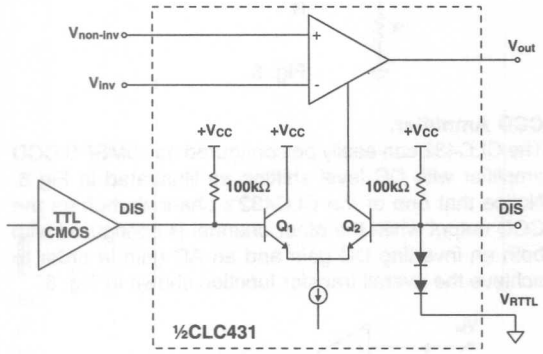


Fig. 1

The disable feature of the CLC431 is such that DIS and $\overline{DIS}$ have common-mode input voltage ranges of ($+V_{CC}$) to ($-V_{CC}+3V$) and are so guaranteed over the commercial temperature range. Internal clamps (not shown) protect the DIS input from excessive input voltages that could otherwise cause damage to the device. This condition occurs when enough source current flows into the node so as to allow DIS to rise to V_{CC}. This clamp is activated once DIS exceeds $\overline{DIS}$ by 1.5Volts and guarantees that V_{DIS} (ground referenced) does not exceed 4.7Volts.

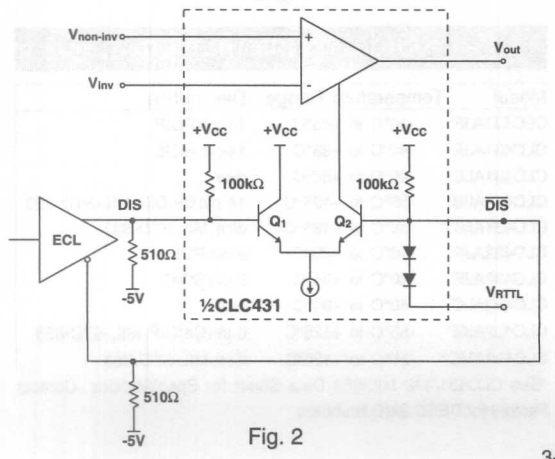


Fig. 2

Fig. 2 illustrates the differential mode of the CLC431's disable feature for ECL-type logic. In order for this mode to operate properly, V_{RTTL} must be left floating while DIS and $\overline{DIS}$ are to be connected directly to the ECL gate as illustrated. Applying a differential logic "high" (DIS - $\overline{DIS}$ ≥ 0.4Volts) switches the tail current of the differential pair from Q2 to Q1 and results in the *disabling* of that CLC431 channel. Alternatively, applying a differential logic "low" (DIS - $\overline{DIS}$ ≤ -0.4Volts) switches the tail current of the differential pair from Q1 to Q2 and results in the *enabling* of that same channel. The internal clamp, mentioned above, also protects against excessive differential voltages up to 30Volts while limiting input currents to <3mA.

DC Performance

A current-feedback amplifier's input stage does not have equal nor correlated bias currents, therefore they cannot be cancelled and each contributes to the total DC offset voltage at the output by the following equation:

$$V_{offset} = \pm\left(I_{bn}*R_s\left(1+\frac{R_f}{R_g}\right)+V_{io}\left(1+\frac{R_f}{R_g}\right)+I_{bi}*R_f\right)$$

The input resistor R_s is that resistance seen when looking from the non-inverting input back towards the source. For inverting DC-offset calculations, the source resistance seen by the input resistor R_g must be included in the output offset calculation as a part of the non-inverting gain equation. Application note OA-7 gives several circuits for DC offset correction.

Layout Considerations

It is recommended that the decoupling capacitors (0.1μF ceramic and 6.8μF electrolytic) should be placed as close as possible to the power supply pins to insure a proper high-frequency low impedance bypass. Careful attention to circuit board layout is also necessary for best performance. Of particular importance is the control of parasitic capacitances (to ground) at the output and invering input pins. See CLC431/432 Evaluation Board literature for more information.

Applications Circuits

2:1 Video Mux (CLC431)

Fig. 3 illustrates the connections necessary to configure the CLC431 as a 2:1 multiplexer in a 75Ω system. Each of the two CLC431's amplifiers is configured with a non-inverting gain of +2V/V using 634Ω feedback (R_f) and gain-setting (R_g) resistors. The feedback resistor value is lower than that recommended in order to compensate for the reduction of loop-gain that results from the inclusion of the 50Ω resistor (R_i) in the feedback loop. This 50Ω resistor serves to isolate the output of the active channel from the impedance of the inactive channel yet does not affect the low output impedance of the active channel. Notice that for proper operation V_{RTTL} 1 (pin 13) is grounded and V_{RTTL} 2 (pin 9) is unconnected. The pins associated with the disable feature are to be connected as follows: DIS1 and $\overline{DIS2}$ (pins 3 & 10) are connected together as well as DIS2 and $\overline{DIS1}$ (pins 5 & 12). Channel 1 is selected with the application of a logic "low" to SELECT while a logic "high" selects Channel 2.

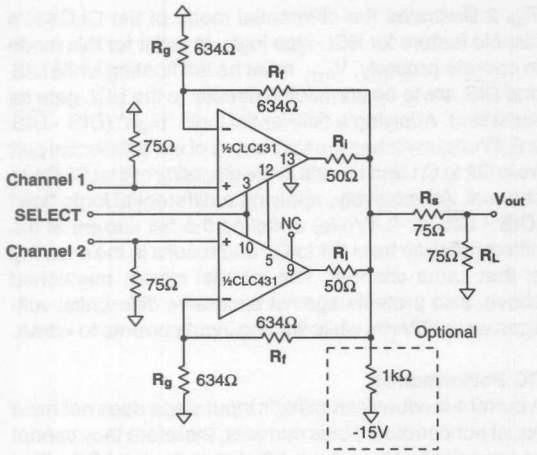


Fig. 3

The optional 1kΩ pull-down resistor connected from the output of the 2:1 mux to the negative power supply ($-V_{CC}$) results in improved differential gain and phase performance (0.02% and 0.01°) at PAL video levels.

Switched Gain Amplifier (CLC431)

As seen from the front page, the CLC431 can also be configured as a switched-gain amplifier that is similar to the 2:1 mux. Configuring each of the two CLC431's amplifiers with different non-inverting gains and tying the two inputs together (eliminating one of the input-terminating resistors) allows the CLC431 to switch an input signal between two different gains.

Inactive Channel Impedances (CLC431)

The impedance that is seen when looking into the output of a disabled CLC431 is typically represented as 1MΩ||16pF. The inverting input impedance becomes very high, essentially open. Therefore, the impedance presented by a disabled channel is $(R_f+R_g)||(R_i+(1M\Omega||16pF))$ as illustrated in Fig. 4. It should also be noted that any trace capacitance that is associated with the common output connection will add in parallel to that presented by the CLC431's inactive channel.

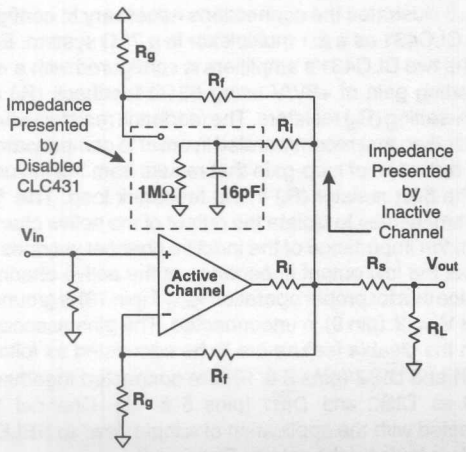


Fig. 4

Twisted-Pair Driver.

Twisted-pair cables are used in many applications such as telephony, video and data communications. The CLC432's two matched channels make it well suited for such applications and is illustrated in Fig. 5.

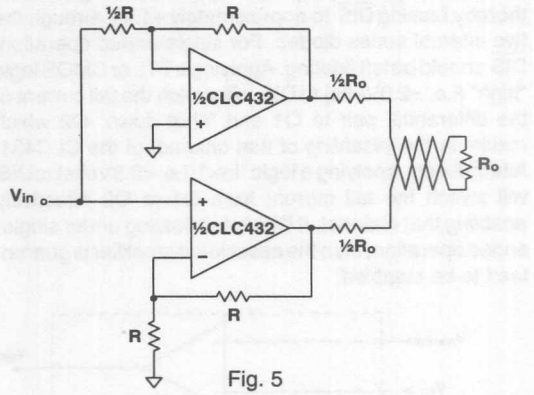
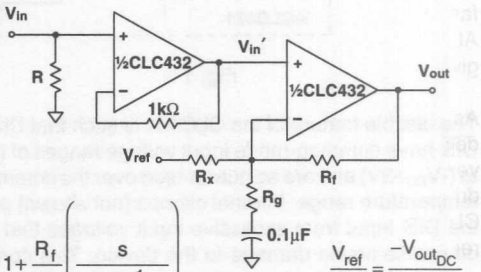


Fig. 5

CCD Amplifier.

The CLC432 can easily be configured as 10MSPS CCD amplifier with DC level shifting as illustrated in Fig 6. Notice that one of the CLC432's channels buffers the CCD output while the other channel is configured with both an inverting DC gain and an AC gain in order to achieve the overall transfer function shown in Fig. 6.



$$\frac{V_{out}}{V_{in}'} = 1 + \frac{R_f}{R_g}\left(\frac{s}{s+\frac{1}{R_gC_g}}\right) \qquad \frac{V_{ref}}{R_x} = \frac{-V_{out_{DC}}}{R_f}$$

for $R_x >> R_g$ $\qquad R_x >> \frac{1}{2\pi f_{in}C_g}$

Fig. 6

Ordering Information

Model	Temperature Range	Description
CLC431AJP	-40°C to +85°C	14-pin PDIP
CLC431AJE	-40°C to +85°C	14-pin SOIC
CLC431ALC	-40°C to +85°C	dice
CLC431A8B*	-55°C to +125°C	14-pin CerDIP, MIL-STD-883
CLC431AMC*	-55°C to +125°C	dice, MIL-STD-883
CLC432AJP	-40°C to +85°C	8-pin PDIP
CLC432AJE	-40°C to +85°C	8-pin SOIC
CLC432ALC	-40°C to +85°C	dice
CLC432A8B*	-55°C to +125°C	8-pin CerDIP, MIL-STD-883
CLC432AMC*	-55°C to +125°C	dice, MIL-STD-883

*See CLC431/432 MIL-883 Data Sheet for Specifications. Contact Factory for DESC SMD Numbers.

Comlinear
A National Semiconductor Company

200MHz, ±15V, Low-Power Voltage Feedback Op Amp

Advance Data CLC436

APPLICATIONS:
- Video ADC driver
- Desktop Multimedia
- Low powered cable driver
- Video DAC buffer
- Active filters
- NTSC & PAL video systems

FEATURES:
- 2.3mA supply current
- 200MHz unity-gain bandwidth
- 2400V/µs slew rate
- 115dB common-mode rejection ratio
- 100mA drive current
- $20V_{pp}$ output swing
- ±5V or ±15V supplies

3

DESCRIPTION

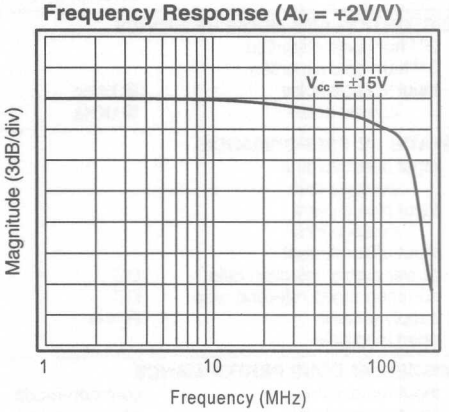
The CLC436 is a high-performance voltage-feedback operational amplifier that has been designed for low-cost general-purpose applications. It can operate from dual ±5V up to ±15V power supplies. Operating from split ±5V rails, the CLC436 consumes a mere 20mW.

Operating from ±15V power supplies, the CLC436 uses only 2.3mA to provide a wide 200MHz unity-gain bandwidth, a very fast 2400V/µs slew rate and quick 16ns rise/fall times (5V pulse). At ±15V, the device also provides larger signal swings ($20V_{pp}$) to give greater dynamic range and higher signal-to-noise ratios.

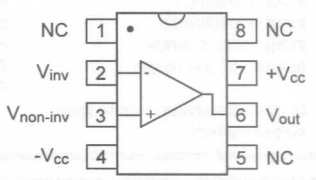
As a low-power NTSC or PAL video line-driver, the CLC436 delivers low differential gain and phase errors (0.1%, 1.0°) and very high output drive current of 100mA. Also, as a video ADC driver, the CLC436 offers low THD and high SFDR. And, the CLC436 can be configured as an excellent active filter for video-reconstruction DACs.

The CLC436's combination of low cost and high performance in addition to its low-power voltage-feedback topology make it a versatile signal conditioning building block for a wide range of consumer-type applications.

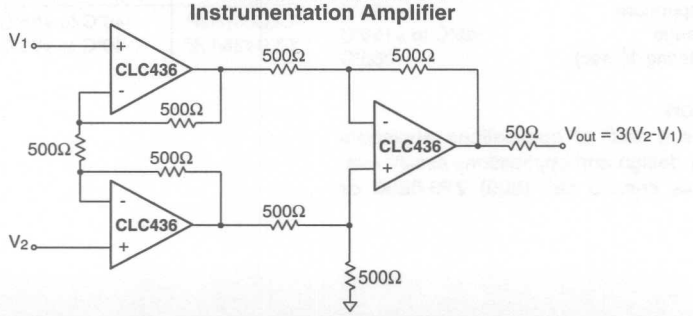
Frequency Response (A_V = +2V/V)



PINOUT
DIP & SOIC



TYPICAL APPLICATION
Instrumentation Amplifier



CLC436 Electrical Characteristics (Av = +2, $R_f = R_g = 499\Omega$; unless specified)

PARAMETERS	CONDITIONS	AMBIENT TEMP TYP +25°				UNITS
	CLC436AJ	±5V Supply $R_L = 100\Omega$	±15V Supply $R_L = 100\Omega$	±5V Supply $R_L = 1.0k\Omega$	±15V Supply $R_L = 1.0k\Omega$	
FREQUENCY DOMAIN RESPONSE						
-3dB bandwidth	$V_{out} < 2.0V_{pp}$	27	33	55	100	MHz
	$V_{out} < 10V_{pp}$	–	–	–	25	MHz
-3dB bandwidth $A_V = +1$	$V_{out} < 2.0V_{pp}$, $R_f = 0$	45	61	150	200	MHz
gain flatness	$V_{out} < 2.0V_{pp}$					
rolloff	DC to 10MHz	1.9	1.5			dB
peaking	DC to 20MHz	0	0			dB
linear phase deviation	DC to 10MHz	–	–			deg
differential gain	4.43MHz, R_L=150Ω	0.15	0.10			%
differential phase	4.43MHz, R_L=150Ω	1.1	1.0			deg
gain bandwidth product	$V_{out} < 2.0V_{pp}$	55	67	100	200	MHz
TIME DOMAIN RESPONSE						
rise and fall time	2V step, t_r(in) = 5ns	12	12			ns
	5V step, t_r(in) = 5ns	16	16			ns
settling time to 0.05%	2V step, t_r(in) = 5ns	48	42			ns
overshoot	2V step, t_r(in) = 5ns	3	2			%
slew rate	5V step, t_r(in) = 5ns	850	2400			V/µs
DISTORTION AND NOISE RESPONSE						
2nd harmonic distortion		–	–			dBc
3rd harmonic distortion		–	–			dBc
input voltage noise	@1KHz	11	11			nV/√Hz
current noise	@1KHz	1	1			pA/√Hz
STATIC DC PERFORMANCE						
input offset voltage		1.4	1.6			mV
average drift		6	6			µV/°C
input bias current		1.0	0.9			µA
average drift		2	2			nA/°C
input offset current		150	130			nA
power supply rejection ratio	DC	85	90			dB
common-mode rejection ratio	DC	110	115			dB
supply current	$R_L = \infty$	2.0	2.3			mA
open loop gain		80	83			dB
MISCELLANEOUS PERFORMANCE						
input resistance	common-mode	40	40			MΩ
input capacitance	common-mode	–	–			pF
input resistance	differential-mode	5	5			MΩ
input capacitance	differential-mode	–	–			pF
input voltage range	common-mode	3.0	11			V
output voltage range	$R_L = 100\Omega$	2.8	+9.9/-8.4			V
	$R_L = \infty$	3.4	9.9			V
output resistance, closed loop		0.01	0.01			Ω
output current		80	100			mA

Absolute Maximum Ratings

supply voltage	±18.0V
maximum junction temperature	+150°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+260°C

Ordering Information

Model	Temperature Range	Description
CLC436AJP	-40°C to +85°C	8-pin PDIP
CLC436AJE	-40°C to +85°C	8-pin SOIC

Applications Support

Comlinear maintains a staff of applications engineers who are available for design and applications assistance. To make use of this service call **(800) 776-0500 or (970) 225-7422**.

Comlinear
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High-Speed, Low-Power Voltage Feedback Op Amp

CLC440

APPLICATIONS:
- Professional video
- Graphics workstations
- Test equipment
- Video switching & routing
- Communications
- Medical imaging
- A/D drivers
- Photo diode transimpedance amplifiers
- Improved replacement for CLC420 or OPA620

FEATURES:
- Unity-gain stable
- High unity-gain bandwidth: 750MHz
- Ultra-low differential gain: 0.015%
- Very low differential phase: 0.025°
- Low power: 70mW
- Extremely fast slew rate: 1500V/µs
- High output current: 90mA
- Low noise: 3.5nV/√Hz
- Dual ±2.5V to ±6V
  or single 5V to 12V supplies

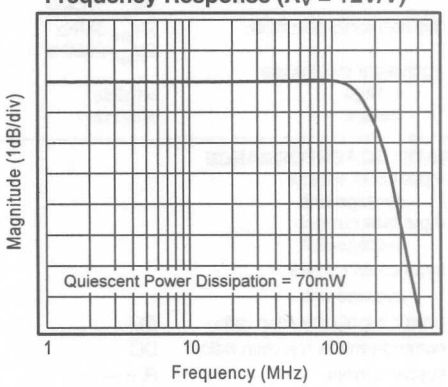
DESCRIPTION

The CLC440 is a wideband, low-power, voltage feedback op amp that offers 750MHz unity-gain bandwidth, 1500V/µs slew rate, and 90mA output current. For video applications, the CLC440 sets new standards for voltage feedback monolithics by offering the impressive combination of 0.015% differential gain and 0.025° differential phase errors while dissipating a mere 70mW.

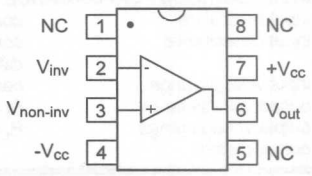
The CLC440 incorporates the proven properties of Comlinear's current feedback amplifiers (high bandwidth, fast slewing, etc.) into a "classical" voltage feedback architecture. This amplifier possesses truly differential and fully symmetrical inputs both having a high 900kΩ impedance with matched low input bias currents. Furthermore, since the CLC440 incorporates voltage feedback, a specific R_f is not required for stability. This flexibility in choosing R_f allows for numerous applications in wideband filtering and integration.

Unlike several other high-speed voltage feedback op amps, the CLC440 operates with a wide range of dual or single supplies allowing for use in a multitude of applications with limited supply availability. The CLC440's low 3.5nV/√Hz(e_n) and 2.5pA/√Hz(i_n) noise sets a very low noise floor.

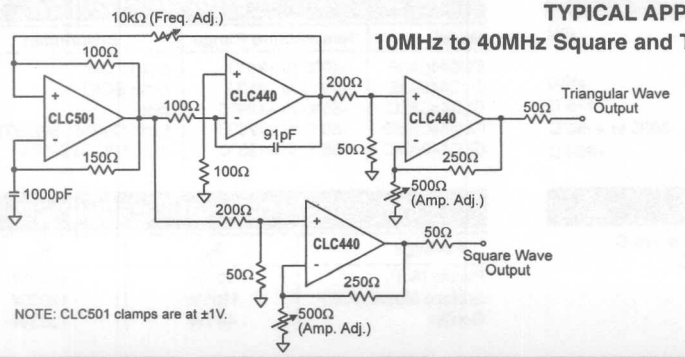
Frequency Response (A_V = +2V/V)



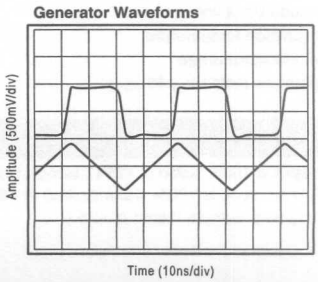
PINOUT
DIP & SOIC



TYPICAL APPLICATION
10MHz to 40MHz Square and Triangular Wave Generator



Generator Waveforms



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CLC440 Electrical Characteristics (A_V = +2, R_f = R_g = 250Ω: V_{cc} = ± 5V, R_L = 100Ω unless specified)

PARAMETERS	CONDITIONS	TYP	GUARANTEED MIN/MAX			UNITS	NOTES
Ambient Temperature	CLC440	+25°C	+25°C	0 to 70°C	-40 to 85°C		
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth A_V =+2	V_{out} < 0.2V_{pp}	260	190	165	160	MHz	B
	V_{out} < 4.0V_{pp}	190	150	135	130	MHz	
-3dB bandwidth A_V =+1	V_{out} < 0.2V_{pp}	750				MHz	
gain bandwidth product	V_{out} < 0.2V_{pp}	230				MHz	
gain flatness	V_{out} < 2.0V_{pp} DC to 75MHz	0.05	0.15	0.20	0.20	dB	
linear phase deviation	V_{out} < 2.0V_{pp} DC to 75MHz	0.8	1.2	1.5	1.5	deg	
differential gain	4.43MHz, R_L=150Ω	0.015	0.03	0.04	0.04	%	
differential phase	4.43MHz, R_L=150Ω	0.025	0.05	0.06	0.06	deg	
TIME DOMAIN RESPONSE							
rise and fall time	2V step	1.5	2.0	2.2	2.5	ns	
	4V step	3.2	4.2	4.5	5.0	ns	
settling time to 0.05%	2V step	10	14	16	16	ns	
overshoot	4V step	7	13	13	13	%	
slew rate	4V step, ±0.5V crossing	1500	900	750	600	V/µs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 5MHz	-69	-59	-59	-59	dBc	
	2V_{pp}, 20MHz	-57	-48	-48	-48	dBc	B
3rd harmonic distortion	2V_{pp}, 5MHz	-70	-65	-64	-64	dBc	
	2V_{pp}, 20MHz	-51	-46	-44	-44	dBc	B
equivalent input noise							
voltage	>1MHz	3.5	4.5	5.0	5.0	nV/√Hz	
current	>1MHz	2.5	3.5	4.0	4.0	pA/√Hz	
STATIC DC PERFORMANCE							
input offset voltage		1.0	3.0	3.5	3.5	mV	A
average drift		5.0		10	10	µV/°C	
input bias current		10	30	35	40	µA	A
average drift		30		50	60	nA/°C	
input offset current		0.5	1.0	2.0	2.0	µA	A
average drift		3.0		10	10	nA/°C	
power supply rejection ratio	DC	65	58	58	58	dB	A
common-mode rejection ratio	DC	80	65	60	60	dB	
supply current	R_L= ∞	7.0	7.5	8.0	8.0	mA	A
MISCELLANEOUS PERFORMANCE							
input resistance	common-mode	900	500	400	300	kΩ	
input capacitance	common-mode	1.2	2.0	2.0	2.0	pF	
	differential-mode	0.5	1.0	1.0	1.0	pF	
input voltage range	common-mode	±3.0	±2.8	±2.7	±2.7	V	
output voltage range	R_L= 100Ω	±2.5	±2.3	±2.2	±2.2	V	
output voltage range	R_L= ∞	±3.0	±2.8	±2.7	±2.6	V	
output current		±90	±80	±65	±45	mA	

Absolute Maximum Ratings

voltage supply	±6V
I_{out} is short circuit protected to ground	
common-mode input voltage	±Vcc
maximum junction temperature	+175°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

Notes

A) J-level: spec is 100% tested at +25°C, sample tested at +85°C.
LC/MC-level: spec is 100% wafer probed at +25°C.

B) J-level: spec is sample tested at +25°C.

Ordering Information

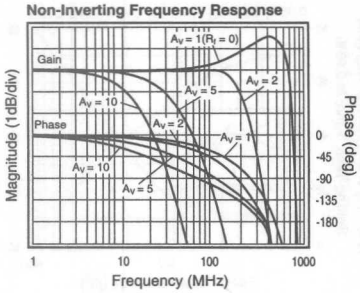
Model	Temperature Range	Description
CLC440AJP	-40°C to +85°C	8-pin PDIP
CLC440AJE	-40°C to +85°C	8-pin SOIC
CLC440ALC	-55°C to +125°C	dice
CLC440SMD	-55°C to +125°C	8-pin CerDIP, MIL-STD-883
CLC440AMC	-55°C to +125°C	dice, MIL-STD-883

Package Thermal Resistance

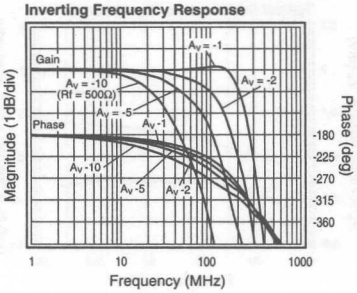
Package	θ_{jc}	θ_{ja}
Plastic (AJP)	90°/W	105°/W
Surface Mount (AJE)	110°/W	130°/W
CerDip	40°/W	130°/W

CLC440 Typical Performance Characteristics (A_V = +2, R_f = 250Ω: V_{cc} = ± 5V, R_L = 100Ω unless specified)

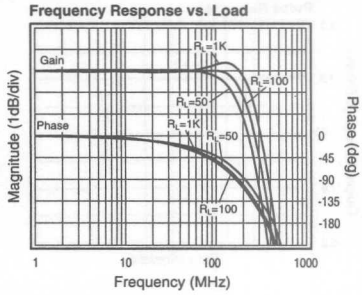
Non-Inverting Frequency Response



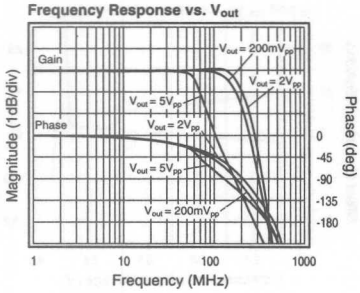
Inverting Frequency Response



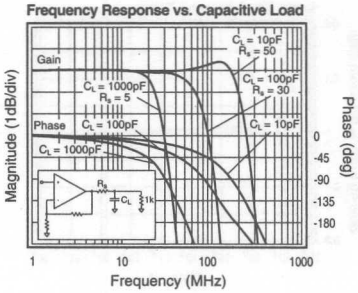
Frequency Response vs. Load



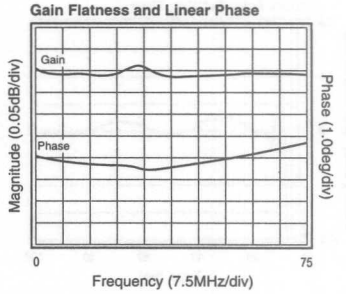
Frequency Response vs. V_{out}



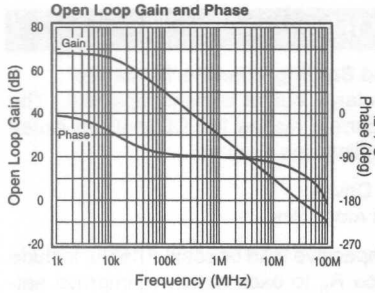
Frequency Response vs. Capacitive Load



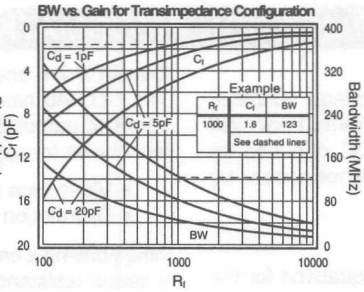
Gain Flatness and Linear Phase



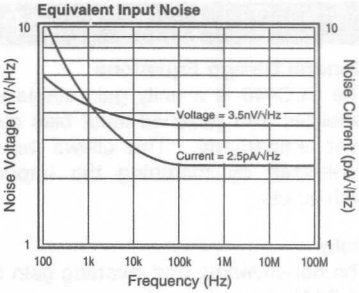
Open Loop Gain and Phase



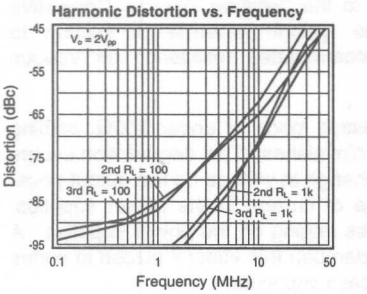
BW vs. Gain for Transimpedance Configuration



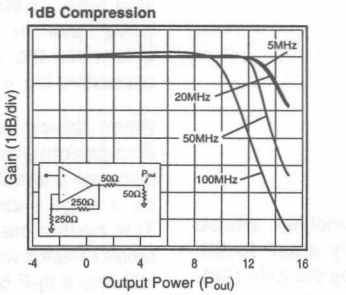
Equivalent Input Noise



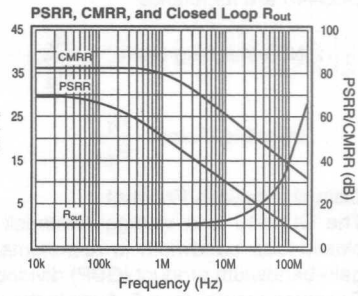
Harmonic Distortion vs. Frequency



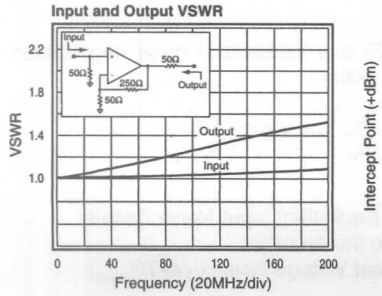
1dB Compression



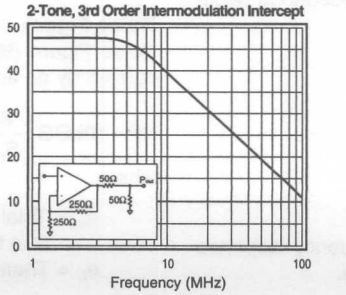
PSRR, CMRR, and Closed Loop R_{out}



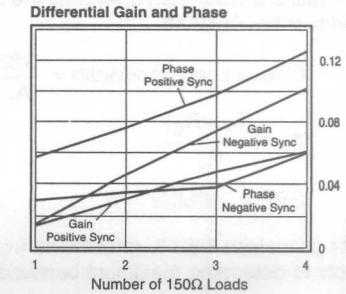
Input and Output VSWR



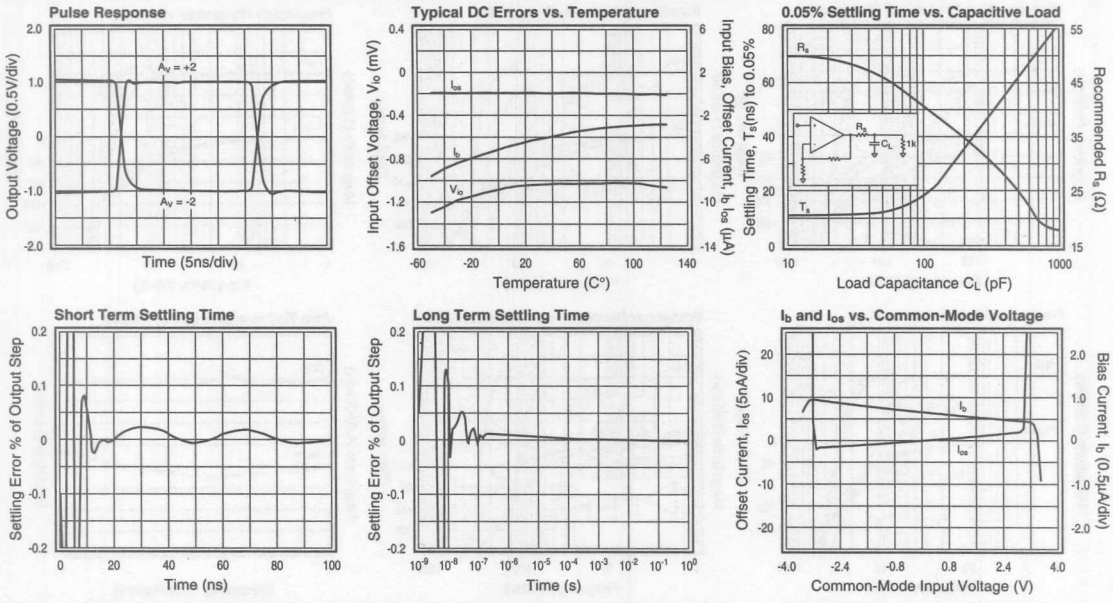
2-Tone, 3rd Order Intermodulation Intercept



Differential Gain and Phase



CLC440 Typical Performance Characteristics (A_V = +2, R_f = 250Ω: V_{cc} = ± 5V, R_L = 100Ω unless specified)



APPLICATION INFORMATION

General Design Equations

The CLC440 is a unity gain stable voltage feedback amplifier. The matched input bias currents track well over temperature. This allows the DC offset to be minimized by matching the impedance seen by both inputs.

Gain

The non-inverting and inverting gain equations for the CLC440 are as follows:

$$\text{Non-inverting Gain: } 1+\frac{R_f}{R_g}$$

$$\text{Inverting Gain: } -\frac{R_f}{R_g}$$

Gain Bandwidth Product

The CLC440 is a voltage feedback amplifier, whose closed-loop bandwidth is approximately equal to the gain-bandwidth product (GBP) divided by the gain (Av). For gains greater than 5, Av sets the closed-loop bandwidth of the CLC440.

$$\text{Closed Loop Bandwidth} = \frac{GBP}{A_v}$$

$$A_v = \frac{(R_f + R_g)}{R_g}$$

GBP = 230MHz

For gains less than 5, refer to the frequency response plots to determine maximum bandwidth.

Output Drive and Settling Time Performance

The CLC440 has large output current capability. The 90mA of output current makes the CLC440 an excellent choice for applications such as:

- Video Line Drivers
- Distribution Amplifiers

When driving a capacitive load or coaxial cable, include a series resistance R_S to back match or improve settling time. Refer to the "Settling Time vs Capacitive Load" plot in the typical performance section to determine the recommended resistance for various capacitive loads.

When driving resistive loads of under 500Ω, settling time performance diminishes. This degradation occurs because a small change in voltage on the output causes a large change of current in the power supplies. This current creates ringing on the power supplies. A small resistor will dampen this effect if placed in series with the 6.8μF bypass capacitor.

Noise Figure

Noise Figure (NF) is a measure of noise degradation caused by an amplifier.

$$NF = 10LOG\left(\frac{S_i/N_i}{S_o/N_o}\right) = 10LOG\left(\frac{e_{ni}^2}{e_t^2}\right)$$

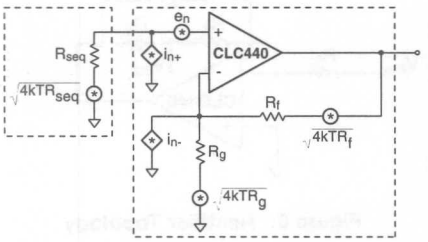
where,

e_{ni} = Total Equivalent Input Noise Density Due to the Amplifier

e_t = Thermal Voltage Noise ($\sqrt{4kTR}_{seq}$)

Figure 1 shows the noise model for the non-inverting amplifier configuration. The model includes all of the following noise sources:

- Input voltage noise (e_n)
- Input current noise ($i_n = i_{n+} = i_{n-}$)
- Thermal Voltage Noise (e_t) associated with each external resistor



$R_{seq} = R_s$ for Unterminated Systems
$R_{seq} = R_s$ II R_T for Terminated Systems

Figure 1: Non-inverting Amplifier Noise Model

The total equivalent input noise density is calculated by using the noise model shown. Equations 1 and 2 represent the noise equation and the resulting equation for noise figure.

$$e_{ni} = \sqrt{e_n^2 + i_n^2\left(R_{seq}^2 + \left(R_f \text{II} R_g\right)^2\right) + 4kTR_{seq} + 4kT\left(R_f \text{II} R_g\right)}$$

Equation 1: Noise Equation

$$NF = 10LOG\left(\frac{e_n^2 + i_n^2\left(R_{seq}^2 + \left(R_f \text{II} R_g\right)^2\right) + 4kTR_{seq} + 4kT\left(R_f \text{II} R_g\right)}{4kTR_{seq}}\right)$$

Equation 2: Noise Figure Equation

The noise figure is related to the equivalent source resistance (R_{seq}) and the parallel combination of R_f and R_g. To minimize noise figure, the following steps are recommended:

- Minimize R_fIIR_g
- Choose the optimum R_s (R_{OPT})

R_{OPT} is the point at which the NF curve reaches a minimum and is approximated by:

$$R_{OPT} \cong \frac{e_n}{i_n}$$

Figure 2 is a plot of NF vs R_s with $R_f = 0$, $R_g = \infty$ ($A_V = +1$). The NF curves for both Unterminated and Terminated systems are shown. The Terminated curve assumes $R_s = R_T$. The table indicates the NF for various source resistances including $R_s = R_{OPT}$.

Layout Considerations

A proper printed circuit layout is essential for achieving high frequency performance. Comlinear provides evaluation boards for the CLC440 (730055-DIP, 730060-SOIC) and suggests their use as a guide for high frequency layout and as an aid in device testing and characterization.

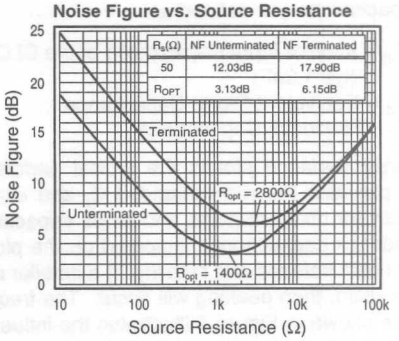


Figure 2: Noise Figure vs. Source Resistance

These boards were laid out for optimum, high-speed performance. The ground plane was removed near the input and output pins to reduce parasitic capacitance. And all trace lengths were minimized to reduce series inductances.

Supply bypassing is required for the amplifiers performance. The bypass capacitors provide a low impedance return current path at the supply pins. They also provide high frequency filtering on the power supply traces. 6.8µF tantalum, 0.01µF ceramic, and 500pF ceramic capacitors are recommended on both supplies. Place the 6.8µF capacitors within 0.75 inches of the power pins, and the 0.01µF and 500pF capacitors less than 0.1 inches from the power pins.

Dip sockets add parasitic capacitance and inductance which can cause peaking in the frequency response and overshoot in the time domain response. If sockets are necessary, flush-mount socket pins are recommended. The device holes in the 730055 evaluation board are sized for Cambion P/N 450-2598 socket pins, or their functional equivalent.

Applications Circuits

Transimpedance Amplifier

The low 2.5pA/√Hz input current noise and unity gain stability make the CLC440 an excellent choice for transimpedance applications. Figure 3 illustrates a low noise transimpedance amplifier that is commonly implemented with photo diodes. R_f sets the transimpedance gain. The photo diode current multiplied by R_f determines the output voltage.

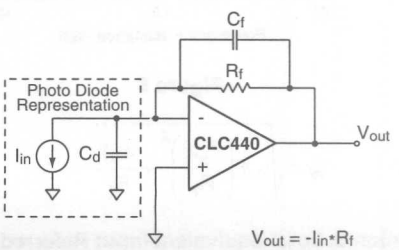


Figure 3: Transimpedance Amplifier Configuration

The capacitances are defined as:

- C_{in} = Internal Input Capacitance of the CLC440 (typ 1.2pF)
- C_d = Equivalent Diode Capacitance
- C_f = Feedback Capacitance

The transimpedance plot in the typical performance section provides the recommended C_f and expected bandwidth for different gains and diode capacitances. The feedback capacitances indicated on the plot give optimum gain flatness and stability. If a smaller capacitance is used, then peaking will occur. The frequency response shown in Figure 4 illustrates the influence of the feedback capacitance on gain flatness.

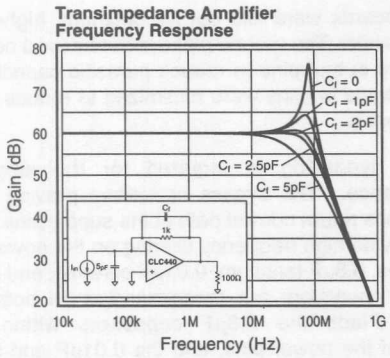


Figure 4

The total input current noise density (i_{ni}) for the basic transimpedance configuration is shown in Equation 3. The plot of current noise density versus feedback resistance is shown in Figure 5.

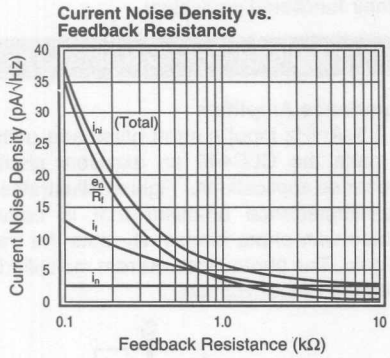


Figure 5

$$i_{ni} = \sqrt{i_n + \left(\frac{e_n 2}{R_f}\right)^2 + \frac{4kT}{R_f}}$$

Equation 3: Total Equivalent Input Referred Current Noise Density

Rectifier

The large bandwidth of the CLC440 allows for high speed rectification. A common rectifier topology is shown in Figure 6. R_1 and R_2 set the gain of the rectifier. V_{out} for a 5MHz, $2V_{pp}$ sinusoidal input is shown in Figure 7.

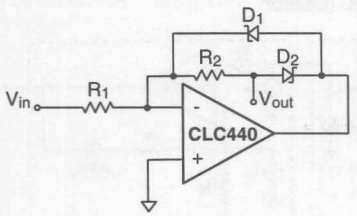


Figure 6: Rectifier Topology

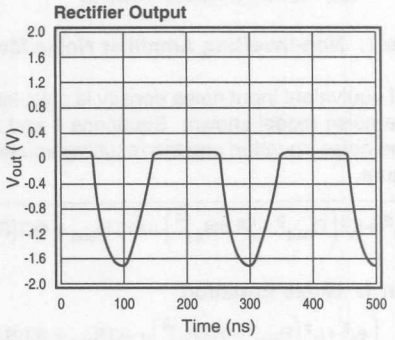


Figure 7: Rectifier Output

Tunable Low Pass Filter

The center frequency of the low pass filter (LPF) can be adjusted by varying the CLC522 gain control voltage, V_g.

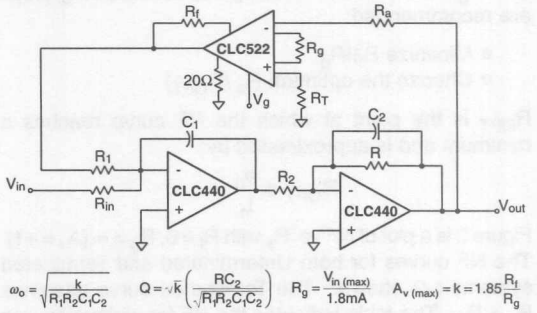


Figure 8: Tunable Low Pass Filter

Applications Support

Comlinear maintains a staff of applications engineers who are available for design and application assistance. To make use of this service call **(800) 776-0500 or (970) 225-7422**.

Comlinear
A National Semiconductor Company

400MHz (A_V = +2), 50mW Current Feedback Op Amp

Advance Data CLC446

APPLICATIONS:
- High resolution video
- ADC driver
- Medical imaging
- Communications
- Pulse amplifier
- RF/IF amplifier
- Instrumentation

FEATURES:
- 400MHz small signal bandwidth (A_V = +2V/V)
- 170MHz large signal bandwidth (A_V = +2V/V)
- 2600V/µs slew rate
- 0.8ns rise/fall time (2V step)
- 5mA supply current
- -75/-77 HD2/HD3 ($2V_{pp}$, 5MHz, R_L = 100Ω)
- 96mA output current

3

DESCRIPTION

The CLC446 is a very high-speed unity-gain stable current-feedback operational amplifier that uses only 50mW quiescent power from split 5V rails or a single 10V rail. It provides a very wideband 400MHz small-signal bandwidth (A_V = +2, R_L = 100Ω), a 2600V/µs slew rate and 0.8ns rise/fall times (2V step). The CLC446 achieves its superior speed/power ratio using an advanced complementary bipolar process and Comlinear's current-feedback architecture.

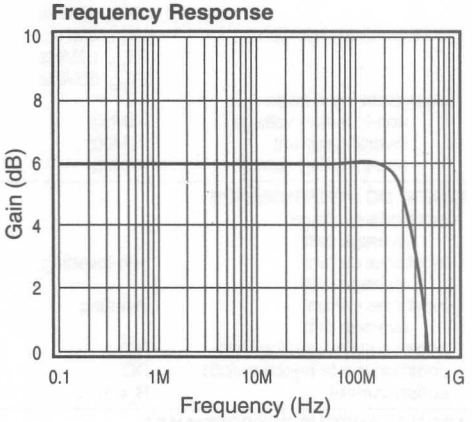
The CLC446 is designed for power-sensitive applications that demand the highest levels of performance. As a pulse amplifier for applications such as high-resolution RGB video, the CLC446 delivers 0.8ns rise/fall times with less than 5% overshoot.

With very low -75dB 2nd harmonic distortion (5MHz, $2V_{pp}$,100Ω) and a quick 20ns settling time to 0.1% (2V step). The CLC446 makes an excellent low-power flash ADC driver.

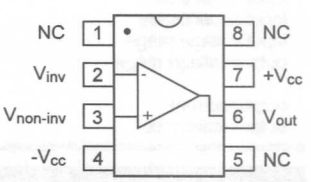
The CLC446 also provides very high non-inverting input impedance (2.5MΩ) and very low output impedance (0.007Ω). For demanding loads it can deliver 96mA continuous output current. And into 100Ω, the CLC446 drives $6.2V_{pp}$.

With its combination of low-power, high-speed and low DC errors, the CLC446 is the perfect choice for high-speed signal conditioning circuit functions such as active filters, differentiators, and simple gain blocks.

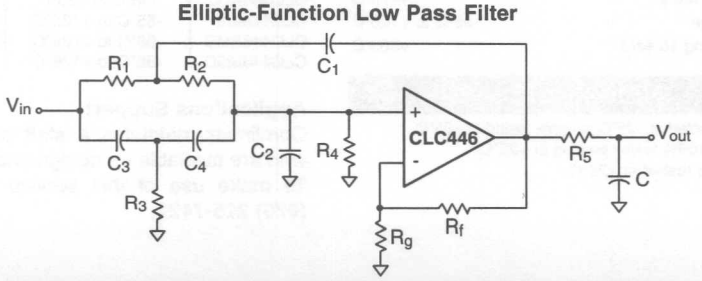
Frequency Response



PINOUT
DIP & SOIC



TYPICAL APPLICATION
Elliptic-Function Low Pass Filter



CLC446 Electrical Characteristics (A_V = +2, R_f = 250Ω: V_{cc} = ± 5V, R_L = 100Ω unless specified)

PARAMETERS	CONDITIONS	TYP	GUARANTEED MIN/MAX			UNITS	NOTES
Ambient Temperature	CLC446	+25°C	+25°C	0 to 70°C	-40 to 85°C		
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth	V_{out} < 0.20V_{pp}	400				MHz	
	V_{out} < 4.0V_{pp}	170				MHz	
gain flatness V_{out} < 2.0V_{pp}	DC to 30 MHz	±0.02				dB	
	DC to 100 MHz	±0.13				dB	
gain peaking V_{out} < 2.0V_{pp}	>100MHz	0.13				dB	
differential gain	NTSC, R_L=150Ω					%	
differential phase	NTSC, R_L=150Ω					deg	
TIME DOMAIN RESPONSE							
rise and fall time	2V step	0.8				ns	
	4V step	1.3				ns	
settling time to 0.1%	2V step	20				ns	
overshoot	4V step	5				%	
slew rate	4V step	2600				V/µs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 5MHz	-75				dBc	
	2V_{pp}, 20MHz	-50				dBc	
	2V_{pp}, 50MHz	-36				dBc	
3rd harmonic distortion	2V_{pp}, 5MHz	-77				dBc	
	2V_{pp}, 20MHz	-57				dBc	
	2V_{pp}, 50MHz	-42				dBc	
equivalent input noise							
non-inverting voltage	>1MHz	4.4				nV/√Hz	
inverting current	>1MHz	16.5				pA/√Hz	
non-inverting current	>1MHz	2.7				pA/√Hz	
STATIC DC PERFORMANCE							
input offset voltage		0.6				mV	
average drift		–				µV/°C	
input bias current	non-inverting	4				nA	
average drift		–				nA/°C	
input bias current	inverting	9				µA	
average drift		–				nA/°C	
power supply rejection ratio	DC	54				dB	
common-mode rejection ratio	DC	50				dB	
supply current	R_L = ∞	5				mA	
MISCELLANEOUS PERFORMANCE							
input resistance	non-inverting	2.5				MΩ	
input capacitance	non-inverting	–				pF	
input voltage range	common-mode	±2.2				V	
output voltage range	R_L = 100Ω	±3.1				V	
	R_L = ∞	±3.2				V	
output current		96				mA	
output resistance	closed loop	7				mΩ	

Absolute Maximum Ratings

voltage supply	±6V
I_{out} is short circuit protected to ground	
common-mode input voltage	±Vcc
maximum junction temperature	+175°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

Notes

A) J-level: spec is 100% tested at +25°C, sample tested at +85°C.
LC/MC-level: spec is 100% wafer probed at +25°C.
B) J-level: spec is sample tested at +25°C.

Ordering Information

Model	Temperature Range	Description
CLC446AJP	-40°C to +85°C	8-pin PDIP
CLC446AJE	-40°C to +85°C	8-pin SOIC
CLC446ALC	-40°C to +85°C	dice
CLC446A8B	-55°C to +125°C	8-pin CerDIP, MIL-STD-883
CLC446AMC	-55°C to +125°C	dice, MIL-STD-883
CLC446SMD	-55°C to +125°C	DESC SMD#

Applications Support

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Comlinear
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1.2GHz Ultra-Wideband Monolithic Op Amp

CLC449

APPLICATIONS:

- High Performance RGB Video
- RF/IF Amplifier
- Instrumentation
- Medical Electronics
- Active Filters
- High-Speed A/D & D/A Converters

FEATURES:

- 1.2GHz small-signal bandwidth (A_V = +2)
- 2500V/µs slew rate
- 0.03%, 0.02° D_G, D_Φ
- 6ns settling time to 0.2%
- 3rd order intercept, 30dBm @ 70MHz
- Dual ±5V or single 10V supply
- High output current: 90mA

DESCRIPTION

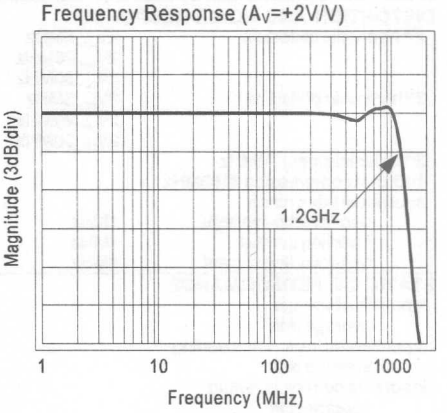
The CLC449 is an ultra-high-speed monolithic op amp, with a typical -3dB bandwidth of 1.2GHz at a gain of +2. This wideband op amp supports rise and fall times less than 1ns, settling time of 6ns (to 0.2%) and slew rate of 2500V/µs. The CLC449 achieves 2nd harmonic distortion of -63dBc at 5MHz at a low supply current of only 12mA. This performance advantage has been achieved through improvements in Comlinear's proven current feedback topology combined with a high-speed complementary bipolar process.

The DC to 1.2GHz bandwidth of the CLC449 is suitable for many IF and RF applications as a versatile op amp building block for replacement of AC coupled discrete designs. Operational amplifier functions such as active filters, gain blocks, differentiation, addition, subtraction and other signal conditioning functions take full advantage of the CLC449's unity-gain stable closed-loop performance.

The CLC449 performance provides greater headroom for lower frequency applications such as component video, high-resolution workstation graphics, and LCD displays. The amplifier's 0.1dB gain flatness to beyond 200MHz, plus 0.8ns 2V rise and fall times are ideal for improving time domain performance. In addition, the 0.03%/0.02° differential gain/phase performance allows system flexibility for handling standard NTSC and PAL signals.

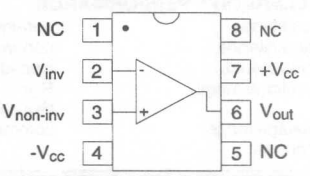
In applications using high-speed flash A/D and D/A converters, the CLC449 provides the necessary wide bandwidth (1.2GHz), settling (6ns to 0.2%) and low distortion into 50Ω loads to improve SFDR.

Frequency Response (A_V=+2V/V)



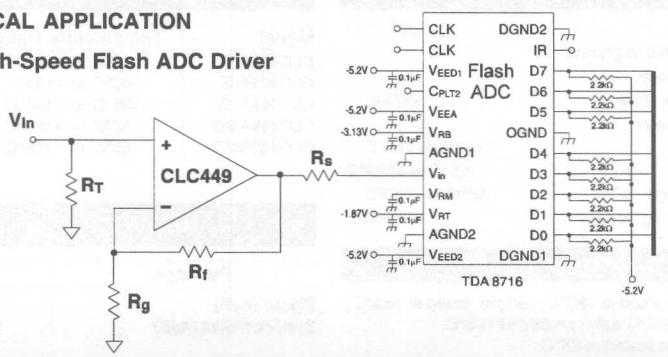
PINOUT

DIP & SOIC



TYPICAL APPLICATION

120MSPS High-Speed Flash ADC Driver



CLC449 Electrical Characteristics (A_v = +2; R_f = 250Ω; V_{cc} =± 5V; R_L = 100Ω)

PARAMETERS	CONDITIONS	TYP	GUARANTEED MIN/MAX			UNITS	NOTES
Ambient Temperature	CLC449	+25°C	+25°C	0 to 70°C	-40 to 85°C		
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth							
small signal	<0.2V_{pp}	1200	---	---	---	MHz	
large signa l	<2V_{pp}	500	400	400	380	MHz	
±0.1 dB bandwidth	<2V_{pp}	200				MHz	
gain flatness							
peaking	DC to 200MHz	0				dB	
rolloff	DC to 200MHz	0.1				dB	
linear phase deviation	<200MHz	0.8				deg	
differential gain	4.43MHz, R_L=150Ω	0.03	0.05	0.05	0.05	%	
differential phase	4.43MHz, R_L=150Ω	0.02	0.02	0.05	0.05	deg	
TIME DOMAIN RESPONSE							
rise and fall time	2V step	0.8	1.1	1.1	1.1	ns	
settling time to 0.2%	2V step	6				ns	
settling time to 0.1%	2V step	11				ns	
overshoot	2V step	10	18	18	18	%	
slew rate	4V step	2500	2000	2000	2000	V/µs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 5MHz	-63				dBc	
	2V_{pp}, 20MHz	-52	-48	-48	-48	dBc	B
	2V_{pp}, 50MHz	-44				dBc	
3rd harmonic distortion	2V_{pp}, 5MHz	-84				dBc	
	2V_{pp}, 20MHz	-73	-66	-64	-64	dBc	B
	2V_{pp}, 50MHz	-62				dBc	
3rd order intercept 70MHz		30				dBm	
1dB gain compression @50MHz		16				dBm	
equivalent input noise							
non-inverting voltage	1MHz	2				nV/√Hz	
inverting current	1MHz	15				pA/√Hz	
non-inverting current	1MHz	3				pA/√Hz	
STATIC DC PERFORMANCE							
input offset voltage		3	7	9	9	mV	A
average drift		25				µV/°C	
input bias current non-inverting		6	30	45	45	µA	A
average drift		50				nA/°C	
input bias current inverting		2	20	25	25	µA	A
average drift		25				nA/°C	
power supply rejection ratio	DC	48	43	41	41	dB	A
common-mode rejection ratio	DC	47	44	45	46	dB	
supply current	R_L= ∞	12	13.5	14	14	mA	A
MISCELLANEOUS PERFORMANCE							
input resistance	non-inverting	400	200	200	150	kΩ	
input capacitance	non-inverting	1.3				pF	
output resistance	closed loop	0.1	.15	.15	.25	Ω	
output voltage range	R_L= ∞	3.3	3.1	3.1	3.1	V	
	R_L=100Ω	2.9	2.8	2.8	2.8	V	
input voltage range	common mode	2.4	2.2	2.1	1.9	V	
output current		90	60	50	40	mA	

Absolute Maximum Ratings

V_{oc}	±6V
I_{out} is short circuit protected to ground	
common-mode input voltage	±V_{cc}
maximum junction temperature	+175°C
operating temperature range	
AJ	-40°C to +85°C
SMD/AM/AL	-55°C to +125°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

Notes

A) J-level: spec is 100% tested at +25°C, sample tested at +85°C.
LC/MC-level: spec is 100% wafer probed at +25°C.
B) J-level: spec is sample tested at 25°C.

Ordering Information

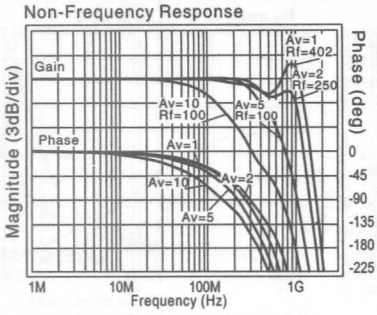
Model	Temperature Range	Description
CLC449AJP	-40°C to +85°C	8-pin PDIP
CLC449AJE	-40°C to +85°C	8-pin SOIC
CLC449ALC	-55°C to +125°C	dice
CLC449AMC	-55°C to +125°C	dice, MIL-STD-883
CLC449SMD	-55°C to +125°C	DESC SMD #

Thermal Package Resistance

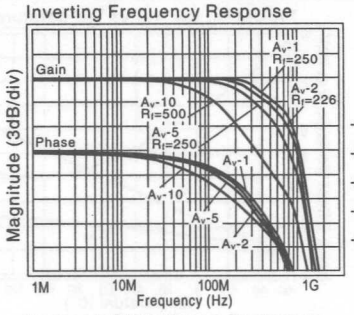
Package	θ_{jc}	θ_{jA}
Plastic (AJP)	90°/W	105°/W
Surface Mount (AJE)	110°/W	130°/W

CLC449 Typical Performance Characteristics (T_A=25°C, V_{CC}=±5V, Rf=250, Av=+2, R_L=100Ω)

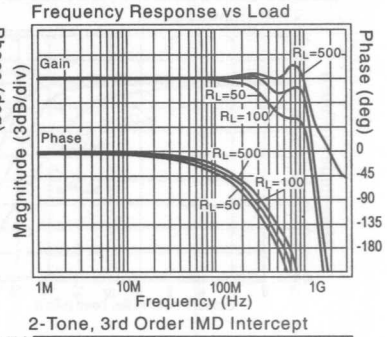
Non-Frequency Response



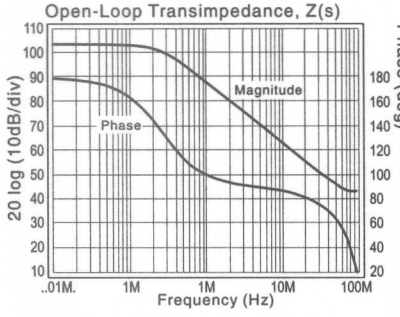
Inverting Frequency Response



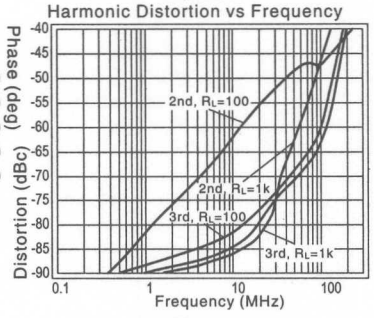
Frequency Response vs Load



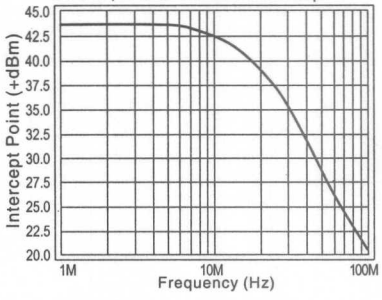
Open-Loop Transimpedance, Z(s)



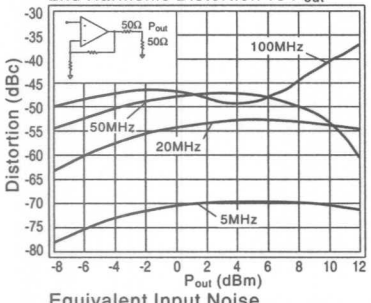
Harmonic Distortion vs Frequency



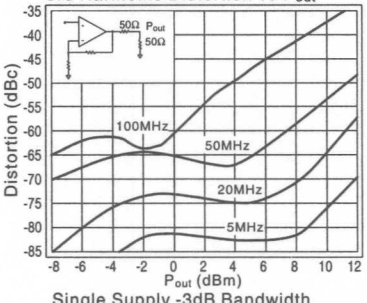
2-Tone, 3rd Order IMD Intercept



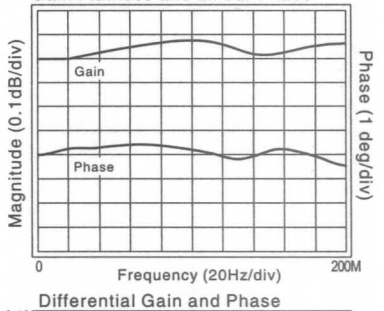
2nd Harmonic Distortion vs P_{out}



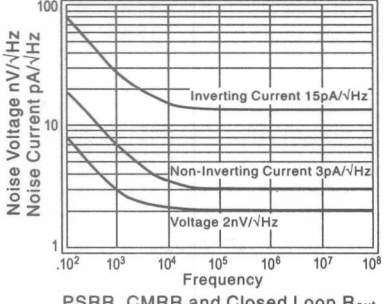
3rd Harmonic Distortion vs P_{out}



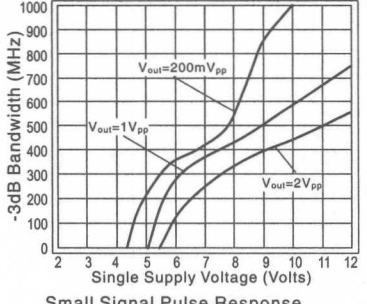
Gain Flatness and Linear Phase



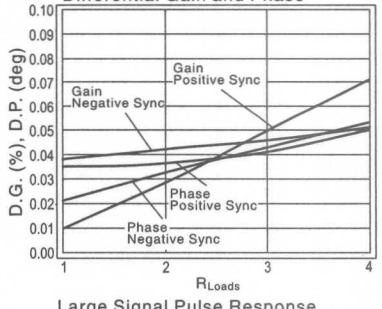
Equivalent Input Noise



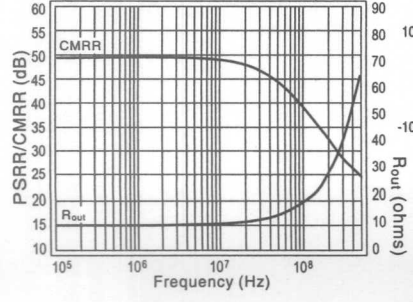
Single Supply -3dB Bandwidth



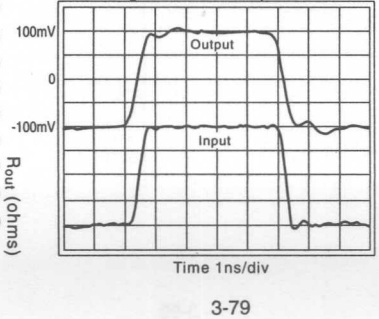
Differential Gain and Phase



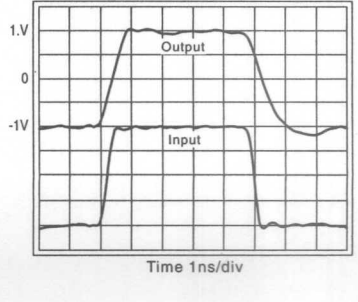
PSRR, CMRR and Closed Loop R_{out}



Small Signal Pulse Response



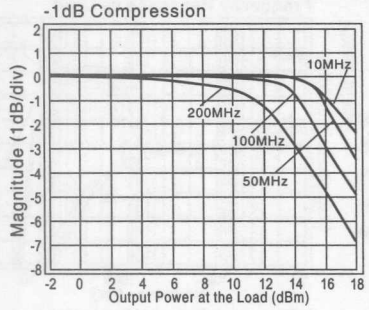
Large Signal Pulse Response



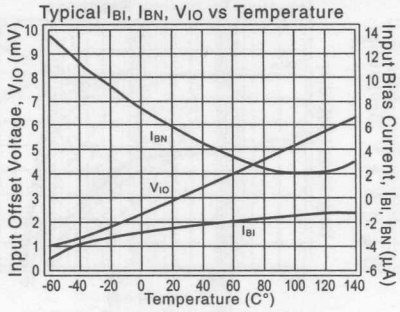
3

CLC449 Typical Performance Characteristics (T_A=25°C, V_{CC}=±5V, Rf=250, Av=+2, R_L=100Ω)

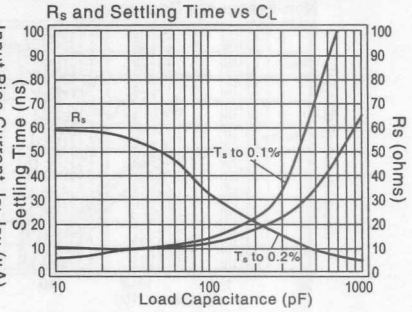
-1dB Compression



Typical I_{BI}, I_{BN}, V_{IO} vs Temperature



R_S and Settling Time vs C_L



Variable Gain Amplifiers
Contents

4

Comlinear
A National Semiconductor Company

Wideband Variable-Gain Amplifier

CLC522

APPLICATIONS:
- variable attenuators
- pulse amplitude equalizers
- HF modulators
- automatic gain control & leveling loops
- video production switching
- differential line receivers
- voltage controlled filters

FEATURES:
- 330MHz signal bandwidth: A_{Vmax}= 2
- 165MHz gain-control bandwidth
- 0.3° to 60MHz linear phase deviation
- 0.04% (-68dB) signal-channel non-linearity
- >40dB gain-adjustment range
- differential or single-end voltage inputs
- single-ended voltage output

DESCRIPTION

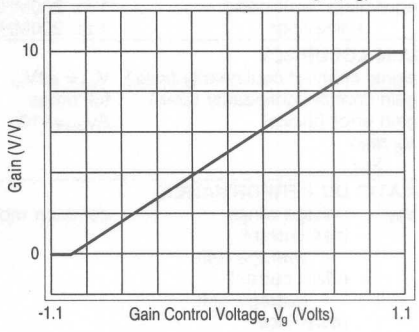
The CLC522 variable gain amplifier (VGA) is a dc-coupled, two-quadrant multiplier with differential voltage inputs and a single-ended voltage output. Two input buffers and an output operational amplifer are integrated with the multiplier core to make the CLC522 a complete VGA system that does not require external buffering.

The CLC522 provides the flexibility of externally setting the maximum gain with only two external resistors. Greater than 40dB gain control is easily achieved through a single high impedance voltage input. The CLC522 provides a linear (in Volts per Volt) relationship between the amplifier's gain and the gain-control input voltage.

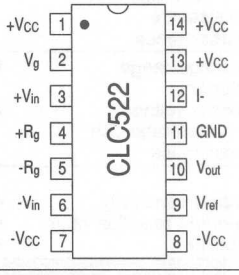
The CLC522's maximum gain may be set anywhere over a nominal range of 2V/V to 100V/V. The gain control input then provides attenuation from the maximum setting. For example, set for a maximum gain of 100V/V, the CLC522 will provide a 100V/V to 1V/V gain control range by sweeping the gain control input voltage from +1 to -0.98V.

Set at a maximum gain of 10V/V, the CLC522 provides a 165MHz signal channel bandwidth and a 165MHz gain control bandwidth. Gain nonlinearity over a 40dB gain range is 0.5% and gain accuracy at A_{Vmax} = 10V/V is typically ±0.3%.

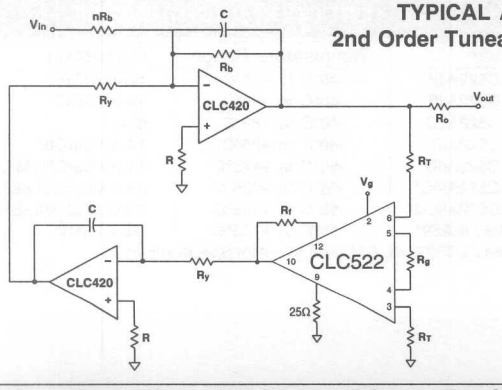
Gain vs. Gain Control Voltage (V_g)



PINOUT
DIP & SOIC



TYPICAL APPLICATION
2nd Order Tuneable Bandpass Filter



$$\frac{V_o}{V_{in}} = \left(-\frac{1}{n}\right)\frac{s\frac{1}{CR_b}}{s^2 + s\frac{1}{CR_b} + \frac{k}{C^2R_y^2}}$$

$$k = 1.85\frac{R_f}{R_g}, \quad Q = \frac{\sqrt{kR_b}}{R_y}, \quad \omega_o = \frac{\sqrt{k}}{CR_y}$$

CLC522 Electrical Characteristics (V_{CC} = ±5V; A_{Vmax} = +10; R_f =1kΩ; R_g =182Ω; R_L = 100Ω; V_g=+1.1V)

PARAMETERS	CONDITIONS	TYP	GUARANTEED MIN/MAX			UNITS	NOTES
Ambient Temperature	AJE,AJP	+25	+25	0 to +70	-40 to +85	°C	1
FREQUENCY DOMAIN RESPONSE							
-3dB bandwidth	V_{out} < 0.5V_{pp}	165	120	115	110	MHz	3
	V_{out} < 5.0V_{pp}	150	100	95	90	MHz	
gain control bandwidth	V_{out} < 0.5V_{pp}	165	120	115	110	MHz	4
gain flatness	V_{out} < 0.5V_{pp}						
peaking	DC to 30MHz	0	0.1	0.1	0.1	dB	3
rolloff	DC to 30MHz	0.05	0.25	0.25	1.3	dB	3
linear phase deviation	DC to 60MHz	0.3	1.0	1.1	1.2	°	
feedthrough	30MHz	- 62	- 57	- 57	-57	dB	3,5
TIME DOMAIN RESPONSE							
rise and fall time	0.5V step	2.2	2.9	3.0	3.2	ns	
	5.0V step	3.0	5.0	5.0	5.0	ns	
settling time	2.0V step to 0.1%	12	18	18	18	ns	
overshoot	0.5V step	2	15	15	15	%	
slew rate	4.0V step	2000	1400	1400	1400	V/µs	
DISTORTION AND NOISE RESPONSE							
2nd harmonic distortion	2V_{pp}, 20MHz	- 50	- 44	- 44	-44	dBc	3
3rd harmonic distortion	2V_{pp}, 20MHz	- 65	- 58	- 56	-54	dBc	3
equivalent input noise	1 to 200MHz	5.8	6.2	6.5	6.8	nV/√Hz	
noise floor	1 to 200MHz	- 152	- 150	- 149	- 149	dBm_{1Hz}	
GAIN ACCURACY							
signal channel nonlinearity (SGNL)	V_{out} = ±2V_{pp}	0.04	0.1	0.1	0.1	%	2
gain control nonlinearity (GCNL)	full range	0.5	2.0	2.2	3.0	%	2
gain error (GACCU)	A_{Vmax}=+10	± 0.0	± 0.5	± 0.5	± 1.0	dB	2
V_g high		+ 990	+ 990±60	+ 990±60	+ 990±60	mV	
low		- 975	- 975±80	- 975±80	- 975±80	mV	
STATIC DC PERFORMANCE							
V_{in} voltage range	common mode	± 2.2	± 1.2	± 1.2	± 1.4	V	
bias current		9	21	26	45	µA	2
average drift		65	---	175	275	nA/°C	
offset current		0.2	2.0	3.0	4.0	µA	
average drift		5	---	30	40	nA/°C	
resistance		1500	650	450	175	kΩ	
capacitance		1.0	2.0	2.0	2.0	pF	
V_g bias current		15	38	47	82	µA	
average drift		125	---	300	600	nA/°C	
resistance		100	38	30	15	kΩ	
capacitance		1.0	2.0	2.0	2.0	pF	
output voltage range	R_L= ∞	± 4.0	± 3.7	± 3.6	± 3.5	V	
current		± 70	± 47	± 40	± 25	mA	
offset voltage	A_{Vmax}=+10	25	85	95	120	mV	2
average drift		100	---	350	400	µV/°C	
resistance		0.1	0.2	0.3	0.6	Ω	
I_{Rgmax}		1.8	1.37	1.26	1.15	mA	
power supply sensitivity	output referred	10	40	40	40	mV/V	3
common-mode rejection ratio	input referred	70	59	59	59	dB	
supply current	R_L= ∞	46	61	62	63	mA	2

Absolute Maximum Ratings

supply voltage	±7V
short circuit current	96mA
common-mode input voltage	±V_{cc}
maximum junction temperature	+200°C
storage temperature	-65°C to+150°C
lead temperature (soldering 10 sec)	+300°C

Notes

1) AJE (SOIC) is tested/guaranteed with R_f=866Ω and R_g= 165Ω.
2) J-level, spec is 100% tested at +25°C, sample tested at +85°C. L-level, spec is 100% wafer probed at 25°C.
3) J-level, spec is sample tested at 25°C.
4) Tested with V_{in} = 0.2V and V_g < 0.5V_{pp}.
5) Feedtrough is tested at maximum attenuation (i.e V_g =-1.1V)

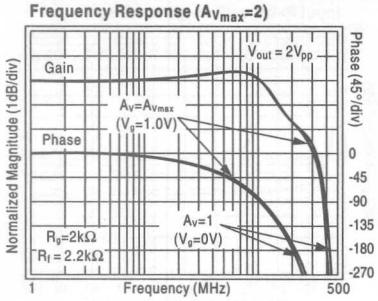
Ordering Information

Model	Temperature Range	Description
CLC522AJP	-40°C to +85°C	14-pin PDIP
CLC522AJE	-40°C to +85°C	14-pin SOIC
CLC522ALC	-40°C to +85°C	dice
CLC522AIB	-40°C to +85°C	14-pin CerDIP
CLC522A8D*	-55°C to +125°C	14-pin CerDIP, MIL-STD-883
CLC522AMC*	-55°C to +125°C	dice, MIL-STD-883
CLC522A8L-2*	-55°C to +125°C	20pin LCC, MIL-STD-883
#5962-93259*	-55°C to +125°C	DESC SMD

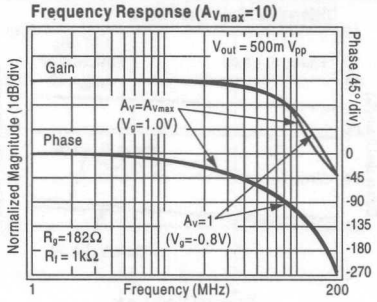
*See CLC522 MIL-883 Data Sheet for Specifications

CLC522 Typical Performance (T_A=+25°C, V_{CC}=±5V, A_V=+10, V_g=1.1V, R_L=100Ω; unless noted)

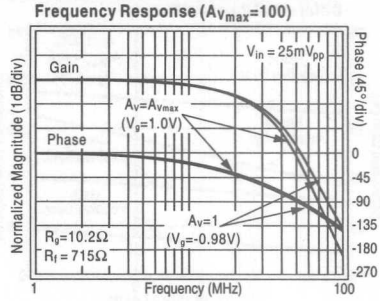
Frequency Response ($A_{V_{max}}$=2)



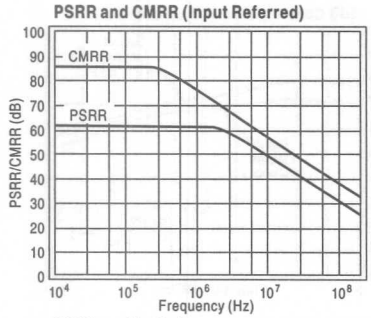
Frequency Response ($A_{V_{max}}$=10)



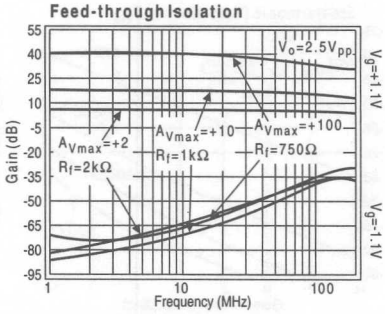
Frequency Response ($A_{V_{max}}$=100)



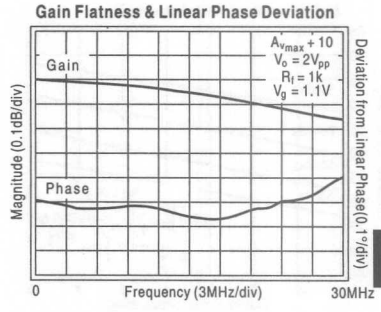
PSRR and CMRR (Input Referred)



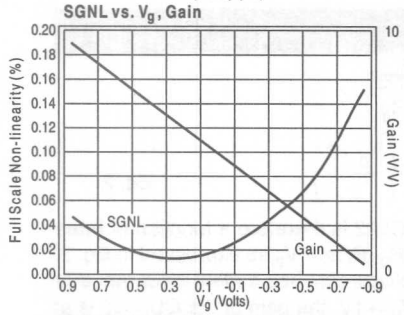
Feed-through Isolation



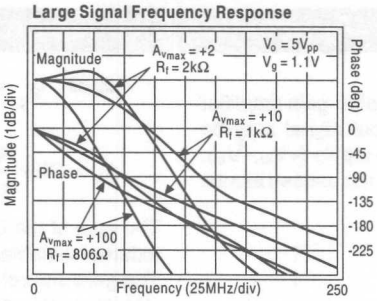
Gain Flatness & Linear Phase Deviation



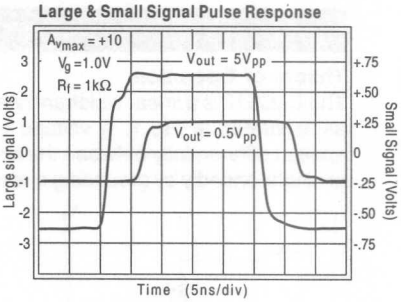
SGNL vs. V_g, Gain



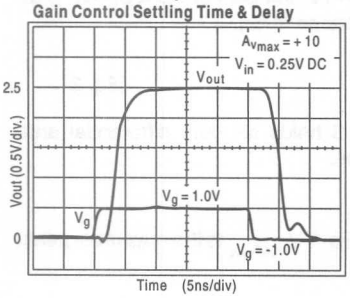
Large Signal Frequency Response



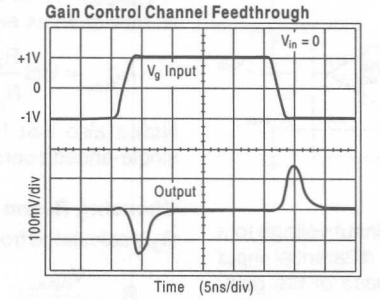
Large & Small Signal Pulse Response



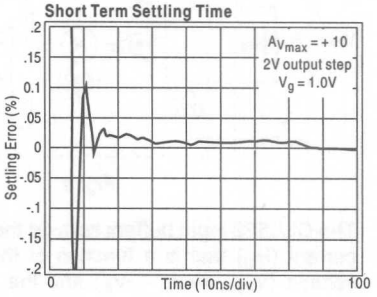
Gain Control Settling Time & Delay



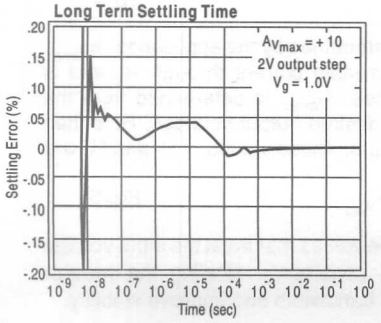
Gain Control Channel Feedthrough



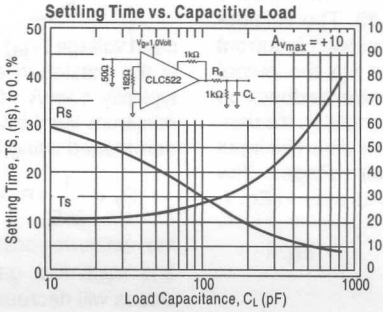
Short Term Settling Time



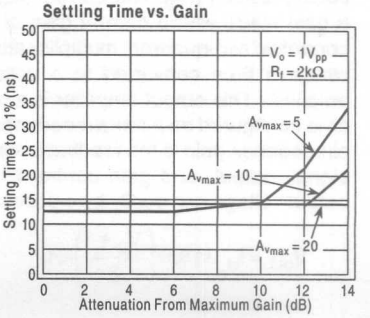
Long Term Settling Time



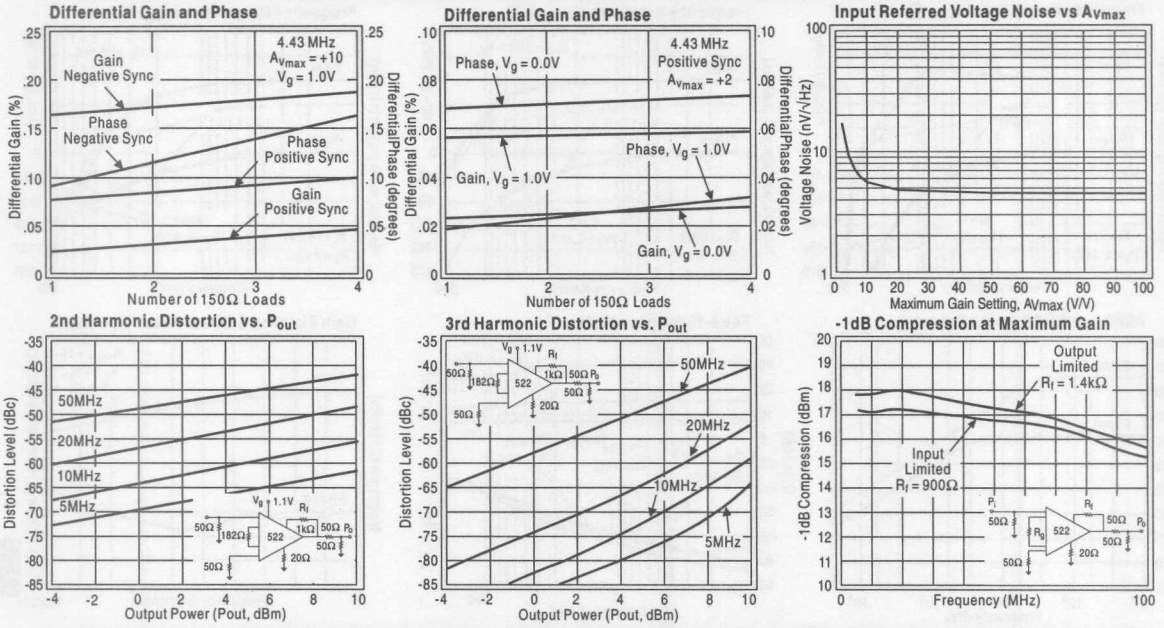
Settling Time vs. Capacitive Load



Settling Time vs. Gain



CLC522 Typical Performance (T_A=+25°C, V_{CC}=±5V, A_V=+10, V_g=1.1V, R_L=100Ω; unless noted)



Application Discussion

Theory of Operation

The CLC522 is a linear wideband variable-gain amplifier as illustrated in Fig 1. A voltage input signal may be applied differentially between the two inputs (+V_{in}, -V_{in}), or single-endedly by grounding one of the unused inputs.

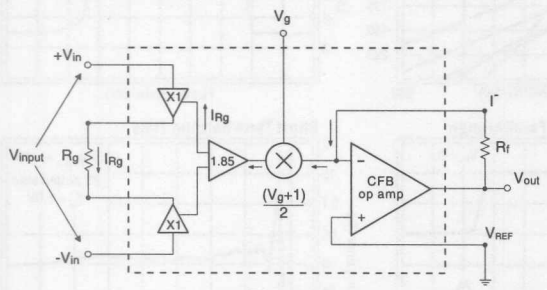


Fig. 1

The CLC522 input buffers convert the input voltage to a current (I_{Rg}) that is a function of the differential input voltage (V_{input} =+V_{in} - -V_{in}) and the value of the gain-setting resistor (R_g). This current (I_{Rg}) is then mirrored to a gain stage with a current gain of 1.85. The voltage-controlled two-quadrant multiplier attenuates this current which is then converted to a voltage via the output amplifier. This output amplifier is a current-feedback op amp configured as a transimpedance amplifier. It's transimpedance gain is the feedback resistor (R_f). The input signal, output, and gain control are all voltages. The output voltage can easily be calculated as seen in Eq. 1.

$$V_{out} = I_{R_g} * 1.85 * \left(\frac{V_g + 1}{2}\right) * R_f \qquad \text{Eq. 1}$$

since $I_{R_g} = \frac{V_{input}}{R_g}$

$$A_V = 1.85 * \frac{R_f}{R_g} * \left(\frac{V_g + 1}{2}\right) \qquad \text{Eq. 2}$$

The gain of the CLC522 is therefore a function of three external variables; R_g, R_f and V_g as expressed in Eq. 2. The gain-control voltage (V_g) has a ideal input range of -1V≤V_g≤+1V. At V_g=+1V, the gain of the CLC522 is at its maximum as expressed in Eq. 3.

$$A_{V_{max}} = 1.85 \frac{R_f}{R_g} \qquad \text{Eq. 3}$$

Notice also that Eq. 3 holds for both differential and single-ended operation.

Choosing R_f and R_g

R_g is calculated from Eq.4. $V_{input_{max}}$ is the maximum peak

$$R_g = \frac{V_{input_{max}}}{I_{R_{g_{max}}}} \qquad \text{Eq. 4}$$

input voltage (V_{pk}) determined by the application. $I_{Rg_{max}}$ is the maximum allowable current through R_g and is typically 1.8mA. Once $A_{V_{max}}$ is determined from the minimum input and desired output voltages, R_f is then determined using Eq. 5. These values of R_f and R_g are

$$R_f = \frac{1}{1.85} * R_g * A_{V_{max}} \qquad \text{Eq. 5}$$

the minimum possible values that meet the input voltage and maximum gain constraints. Scaling the resistor values will decrease bandwidth and improve stability.

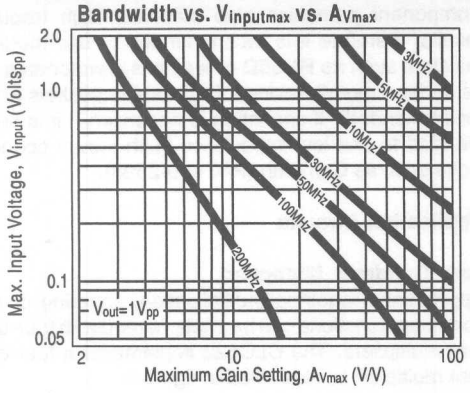


Fig. 2

Fig. 2 illustrates the resulting CLC522 bandwidths as a function of the maximum and minimum input voltages when V_{out} is held constant at $1V_{pp}$.

Adjusting Offsets

Treating the offsets introduced by the input and output stages of the CLC522 is easily accomplished with a two step process. The offset voltage of the output stage is treated by first applying -1.1Volts on V_g, which effectively

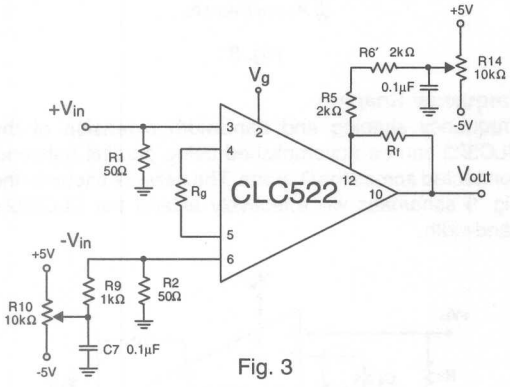


Fig. 3

isolates the input stage and multiplier core from the output stage. As illustrated in Fig. 3, the trim pot located at R14 on the CLC522 Evaluation Board should then be adjusted in order to null the offset voltage seen at the CLC522's output (pin 10). Once this is accomplished, the offset errors introduced by the input stage and multiplier core can then be treated. The second step requires the absence of an input signal and matched source impedances on the two input pins in order to cancel the bias current errors. This done then +1.1Volts should be applied to V_g and the trim pot located at R10 adjusted in order to null the offset voltage seen at the CLC522's output. If a more limited gain range is anticipated, the above adjustments should be made at these operating points.

Gain Errors

The CLC522's gain equation as theoretically expressed in Eq. 2 must include the device's error terms in order to yield the actual gain equation. Each of the gain error terms are specified in the Electrical Characteristics table and are defined below and illustrated in Fig. 4.

GACCU : error of $A_{V_{max}}$, expressed as ±dB.
GCNL : deviation from theoretical expressed as ±%.
$V_{g_{high}}$: voltage on V_g producing $A_{V_{max}}$.
$V_{g_{low}}$: voltage on V_g producing $A_{V_{min}} = 0V/V$.
$\Delta V_{g_{high}}, \Delta V_{g_{low}}$: error of $V_{g_{high}}, V_{g_{low}}$ expresed as ±mV.

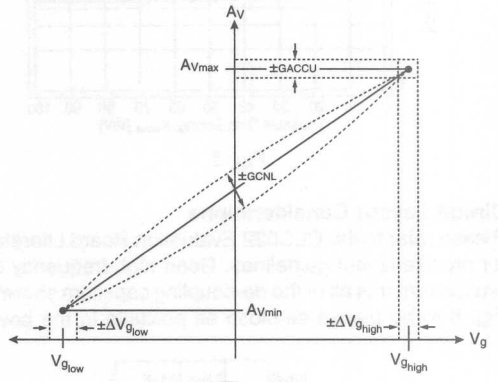


Fig. 4

Combining these error terms with Eq. 2 gives the "gain envelope" equation and is expressed in Eq. 7. From the Electrical Characteristics table, the nominal endpoint values of V_g are: $V_{g_{high}}$ =+990mV and $V_{g_{low}}$ = -975mV.

$$A_V = A_{V_{max}}\left(\frac{10^{\frac{\pm GACCU}{20}}\left(V_g - V_{g_{low}} \pm \Delta V_{g_{low}}\right)}{\left(V_{g_{high}} \pm \Delta V_{g_{high}} - V_{g_{low}} \pm \Delta V_{g_{low}}\right)} \pm \left(1 - V_g{}^2\right)GCNL\right) \qquad \text{Eq. 7}$$

Signal-Channel Nonlinearity

Signal-channel nonlinearity, SGNL, also known as integral endpoint linearity, measures the non-linearity of an amplifier's voltage transfer function. The CLC522's SGNL, as it is specified in the Electrical Characteristics table, is measured while the gain is set at its maximum (i.e. V_g=+1.1V). The Typical Performance Characteristics plot labled "SGNL & Gain vs V_g" illustrates the CLC522's SGNL as V_g is swept through its full range. As can be seen in this plot, when the gain as reduced from $A_{V_{max}}$, SGNL improves to < 0.02%(-74dB) at V_g=0 and then degrades somewhat at the lowest gains.

Noise

Fig. 5 describes the CLC522's input-refered spot noise density as a function of $A_{V_{max}}$. The plot includes all the noise contributing terms. At $A_{V_{max}}$ = 10V/V, the CLC522 has a typical input-referred spot noise density (e_{ni}) of 5.8nV/√Hz. The input RMS voltage noise can be determined from the following single-pole model:

$$V_{RMS} = e_{ni} * \sqrt{1.57 * (-3dB\ bandwidth)} \qquad \text{Eq. 8}$$

Further discussion and plots of noise and the noise model is provided in Application Note OA-23. Comlinear also provides SPICE models that model internal noise and other parameters for a typical part.

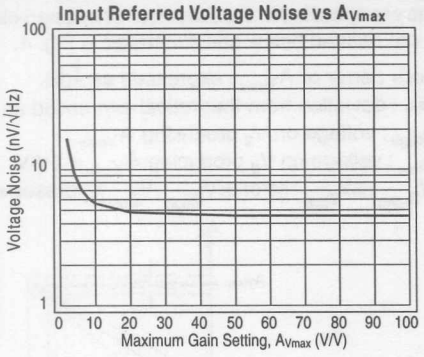


Fig. 5

Circuit Layout Considerations

Please refer to the CLC522 Evaluation Board Literature for precise layout guidelines. Good high-frequency operation requires all of the de-coupling capcitors shown in Fig. 6 to be placed as close as possible to the power

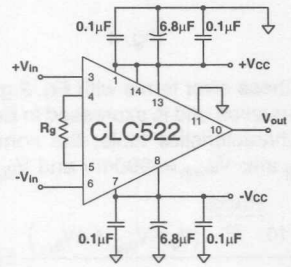


Fig. 6

supply pins in order to insure a proper high-frequency low-impedance bypass. Adequate ground plane and low-inductive power returns are also required of the layout. Minimizing the parasitic capacitances at pins 3, 4, 5, 6, 9,

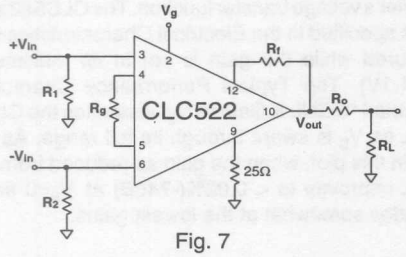


Fig. 7

10 and 12 as shown in Fig. 7 will assure best high frequency performance. Vref (pin 9) to ground should include a small resistor value of 25 ohms or greater to buffer the internal voltage follower. The parasitic inductance of component leads or traces to pins 4, 5 and 9 should also be kept to a minimum. Parasitic or load capacitance, C_L, on the output (pin 10) degrades phase margin and can lead to frequency response peaking or circuit oscillation. This should be treated with a small series resistor between output (pin 10) and C_L (see the plot "Settling Time vs. Capacitive Load" for a recommended series resistance).

Component parasitics also influence high frequency results, therefore it is recommended to use metal film resistors such as RN55D or leadless components such as surface mount devices. High profile sockets are not recommended. If socketing is necessary, it is recommended to use low impedance flush mount connector jacks such as Cambion (P/N 450-2598).

Application Circuits

Four-Quadrant Multiplier

Applications requiring multiplication, squaring or other non-linear functions can be implemented with four-quadrant multipliers. The CLC522 implements a four-quadrant multiplier as illustrated in figure 8.

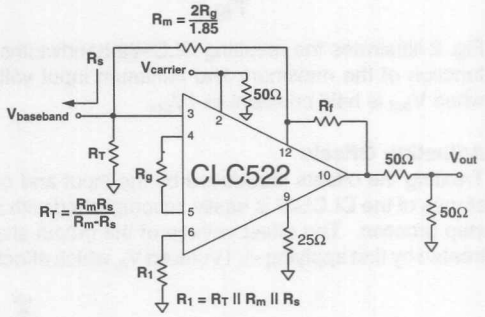


Fig. 8

Frequency Shaping

Frequency shaping and bandwidth extension of the CLC522 can be accomplished using parallel networks connected across the R_g ports. The network shown in the Fig. 9 schematic will effectively extend the CLC522's bandwidth.

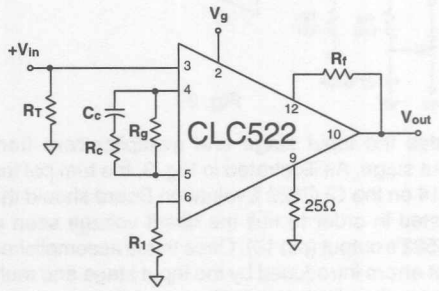


Fig. 9

2nd Order Tuneable Bandpass Filter

The CLC522 Variable-Gain Amplifier placed into feedback loops provide signal processing functions such as 2nd order tuneable bandpass filters. The center frequency of the 2nd order bandpass illustrated on the front page is adjusted through the use of the CLC522's gain-control voltage, V_g. The integrators implemented with two CLC420s, provide the coefficients for the transfer function.

Buffer Amplifier
Contents

Comlinear
A National Semiconductor Company

Low-Power, Wideband, Closed-Loop Buffer

CLC109

APPLICATIONS:

- Video switch buffers
- Test point drivers
- Low power active filters
- DC clamping buffer
- High-speed S & H circuits
- Inverting op amp input buffer

FEATURES:

- High small-signal bandwidth (270MHz)
- Low supply current (3.5mA @ ±5V)
- Low output impedance (2.8Ω)
- 350V/μs slew rate
- Single supply operation (0 to 3V supply min.)
- Evaluation boards and Spice models

DESCRIPTION

The CLC109 is a high-performance, closed-loop monolithic buffer intended for power sensitive applications. Requiring only 35mW of quiescent power (±5V supplies), the CLC109 offers a high bandwidth of 270MHz ($0.5V_{pp}$) and a slew rate of 350V/μs. Even with this minimal dissipation, the CLC109 can easily drive a demanding 100Ω load. The buffer specifications are for a 100Ω load.

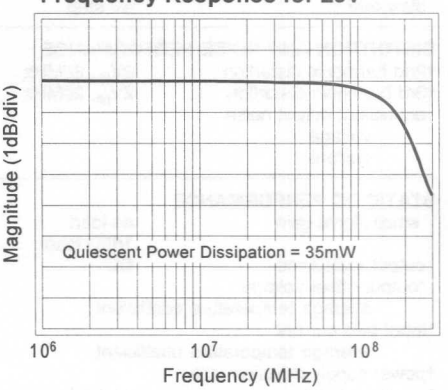
With its patented closed-loop topology, the CLC109 has significant performance advantages over conventional open-loop designs. Applications requiring low (2.8Ω) output impedance and nearly ideal unity gain (0.997) through very high frequencies will benefit from the CLC109's superior performance. Power sensitive applications will benefit from the CLC109's excellent performance on reduced or single supply voltages.

Constructed using an advanced, complementary bipolar process and Comlinear's proven high-performance architectures, the CLC109 is available in several versions to meet a variety of requirements.

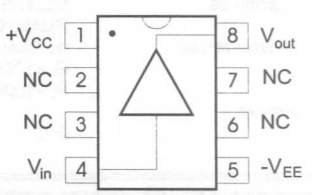
CLC109AJP	-40°C to +85°C	8-pin Plastic DIP
CLC109AJE	-40°C to +85°C	8-pin Plastic SOIC
CLC109AIB	-40°C to +85°C	8-pin hermetic CERDIP
CLC109A8B	-55°C to +125°C	8-pin hermetic CERDIP, MIL-STD-883, Level B
CLC109ALC	-55°C to +125°C	dice
CLC109AMC	-55°C to +125°C	dice qualified to Method 5008, MIL-STD-883, Level B

Contact factory for other packages and DESC SMD number.

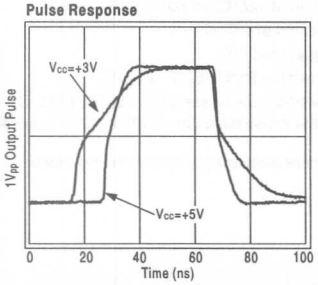
Frequency Response for ±5V



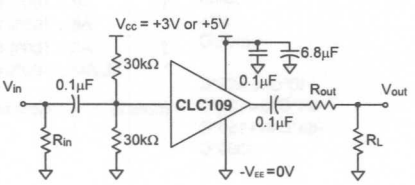
PINOUT
DIP & SOIC



Pulse Response

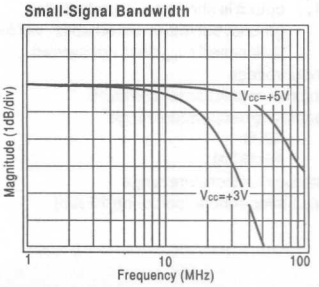


TYPICAL APPLICATION



Single-Supply Circuit

Small-Signal Bandwidth



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CLC109 Electrical Characteristics ($\pm V_{cc}$ = ± 5V, R_L = 100Ω unless specified)

PARAMETER	CONDITIONS	TYP	MIN AND MAX RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC109AJ/AI	+25°C	-40°C	+25°C	+85°C		
	CLC109A8/AM/AL	+25°C	-55°C	+25°C	+125°C		
FREQUENCY RESPONSE							
†small signal bandwidth	V_{out} < 0.5V_{pp}	270	200	200	150	MHz	SSBW
	V_{out} < 2.0V_{pp}	120	90	90	70	MHz	LSBW
gain flatness[1]	V_{out} < 0.5V_{pp}						
† flatness	DC-30MHz	0	±0.1	±0.1	±0.1	dB	GFL
† peaking	DC-200MHz	0	1.0	0.3	0.3	dB	GFPH
† rolloff	DC-60MHz	0.1	0.4	0.4	0.6	dB	GFRH
differential gain	4.43MHz, 150Ω load	0.7	1.5	1.0	1.0	%	DG
differential phase	4.43MHz, 150Ω load	0.03	0.05	0.05	0.1	°	DP
TIME DOMAIN RESPONSE							
rise and fall time	0.5V step	1.3	1.7	1.7	2.3	ns	TRS
	2.0V step	4.4	6	6	7	ns	TRL
settling time to ±0.05%	2.0V step	12	25	18	25	ns	TS
overshoot	0.5V step	3	15	10	10	%	OS1
slew rate	4V step	350	220	250	220	V/µsec	SR
DISTORTION AND NOISE PERFORMANCE							
†2nd harmonic distortion	$2V_{pp}$, 20MHz	-46	-36	-38	-38	dBc	HD2
†3rd harmonic distortion	$2V_{pp}$, 20MHz	-55	-50	-50	-45	dBc	HD3
equivalent output noise							
voltage		3.3	4.1	4.1	4.5	nV/√Hz	VN
current		1.3	3	2	2	pA/√Hz	ICN
STATIC DC PERFORMANCE							
small signal gain	no load	0.997	0.995	0.995	0.994	V/V	GA1
	100Ω load	0.96	0.94	0.95	0.95	V/V	GA2
output resistance	DC	2.8	5.0	4.0	4.0	Ω	RO
*output offset voltage		1	±8.2	±5	±6	mV	VIO
average temperature coefficient		±10	±40		±30	µV/°C	DVIO
*input bias current		±2	±8	±4	±4	µA	IBN
average temperature coefficient		±30	±50		±25	nA/°C	DIBN
†power supply rejection ratio		-56	-48	-48	-46	dB	PSRR
*supply current	no load	3.5	4	4	4	mA	ICC
MISCELLANEOUS PERFORMANCE							
integral endpoint linearity	±1V, full scale	0.5	1.0	0.7	0.6	%	ILIN
input resistance		1.5	0.3	1.0	2.0	MΩ	RIN
input capacitance	CERDIP	2.5	3.5	3.5	3.5	pF	CIN
	Plastic DIP	1.25	2.0	2.0	2.0	pF	CIN
output voltage range	no load	4.0	3.6	3.8	3.8	V	VO
	R_L=100Ω	+3.8,-2.5	+3.0,-1.2	+3.6,-2.0	+3.6,-2.5	V	VOL
	R_L=100Ω , 0°C		+3.0,-1.6			V	VOL
output current		+60,-30	+40,-12	+40,-20	+40,-30	mA	IO
	0°C		+40,-16			mA	IO

Absolute Maximum Ratings

V_{cc}	±7.0V
I_{out} output is short circuit protected to ground, but maximum reliability will be maintained if I_{out} does not exceed...	36mA
input voltage	±V_{cc}
maximum junction temperature	+175°C
operating temperature range	
AJ/AI	-40°C to +85°C
A8/AM/AL	-55°C to +125°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

Miscellaneous Ratings

Notes:

* AJ,AI : 100% tested at +25°C, sample +85°C.

† AJ : Sample tested at +25°C.

† AI : 100% tested at +25°C.

* A8 : 100% tested at +25°C, -55°C, +125°C

† A8 : 100% tested at +25°C, sample at -55°C, +125°C.

* AL,AM : 100% wafer probe tested at +25°C to +25°C specifications.

(note 1) : Gain flatness tests are performed from 0.1MHz

Single Supply Electrical Characteristics (V_{CC}=+3V or V_{CC}=+5V, $-V_{EE}$=0V, T_A=+25° C, R_L = 100Ω, unless noted)

PARAMETERS	CONDITIONS	V_{CC}=3V	V_{CC}=5V	UNITS
FREQUENCY DOMAIN RESPONSE				
-3dB bandwidth	V_{out} < 0.5V_{pp}	30	90	MHz
	V_{out} < 2.0V_{pp}		35	MHz
gain flatness	V_{out} < 0.5V_{pp}			
flatness	DC to 30MHz	3	0.3	dB
peaking	DC to 200MHz	0	0	dB
rolloff	DC to 60MHz		1.5	dB
TIME DOMAIN RESPONSE				
rise and fall time	0.5V step	13.9	4.7	ns
	2.0V step		13.5	ns
overshoot	0.5V step	0	0	%
slew rate	0.5V step	35	200	V/µs
DISTORTION AND NOISE RESPONSE				
2nd harmonic distortion	0.5V_{pp},20MHz	-32		dBc
	1.0V_{pp},20MHz		-37	dBc
3rd harmonic distortion	0.5V_{pp},20MHz	-29		dBc
	1.0V_{pp},20MHz		-43	dBc
STATIC DC PERFORMANCE				
small-signal gain	AC-coupled	0.89	0.94	V/V
supply current	R_L= ∞	0.75	1.6	mA
MISCELLANEOUS PERFORMANCE				
output voltage range	R_L= ∞	1.5	2.8	V_{pp}
	R_L=100Ω	1.1	2.6	V_{pp}

Operation

The CLC109 is a low-power, high-speed unity-gain buffer. It uses a closed-loop topology which allows for accuracy not usually found in high-speed buffers. A closed-loop design provides high accuracy and low output impedance through a wide bandwidth.

Single Supply Operation

Although the CLC109 is specified to operate from split ±5V power supplies, there is no internal ground reference that prevents operation from a single voltage power supply. For single supply operation the input signal should be biased at a DC value of ½V_{CC}. This can be accomplished by AC coupling and rebiasing as shown in the "Typical Application" illustrations on the front page.

The above electrical specifications provide typical performance specifications for the CLC109 at 25°C while operating from a single +3V or a single +5V power supply.

Printed Circuit Layout and Supply Bypassing

As with any high-frequency device, a good PCB layout is required for optimum performance. This is especially important for a device as fast as the CLC109.

To minimize capacitive feedthrough, pins 2, 3, 6, and 7 should be connected to the ground plane, as shown in Figure 1. Input and output traces should be laid out as transmission lines with the appropriate termination resistors very near the CLC109. On a 0.065 inch epoxy PCB material, a 50Ω transmission line (commonly called stripline) can be constructed by using a trace width of 0.1" over a complete ground plane.

Figure 1 shows recommended power supply bypassing.

Parasitic or load capacitance directly on the output of the CLC109 will introduce additional phase shift in the device.

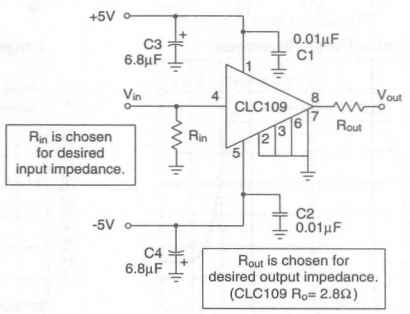


Figure 1: Recommended circuit & evaluation board schematic

This phase shift can decrease phase margin and increase frequency response peaking. A small series resistor inserted between pin 6 and the capacitance effectively decouples this effect. The graphs on the following page illustrate the required resistor value and the resulting performance vs. capacitance.

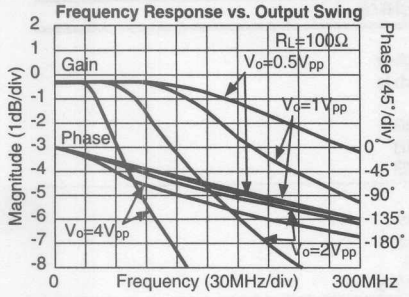
Precision buffed resistors (PRP8351 series from Precision Resistive Products), which have low parasitic reactances, were used to develop the data sheet specifications. Precision carbon composition resistors or standard spirally-trimmed RN55D metal film resistors will work, though they may cause a slight degradation of ac performance due to their reactive nature at high frequencies.

Evaluation Boards

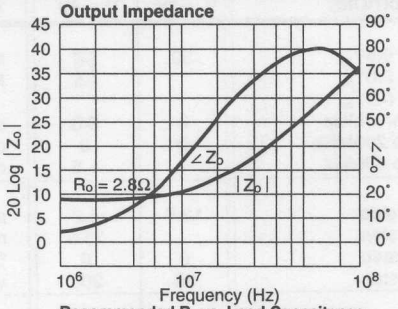
Evaluation boards are available from Comlinear as part #730012 (DIP) and #730045 (SOIC). This board was used in the characterization of the device and provides optimal performance. Designers are encouraged to copy these printed circuit board layouts for their applications.

Typical Performance Characteristics (T_A = +25°C, V_{cc} = ± 5V, R_L = 100Ω unless specified)

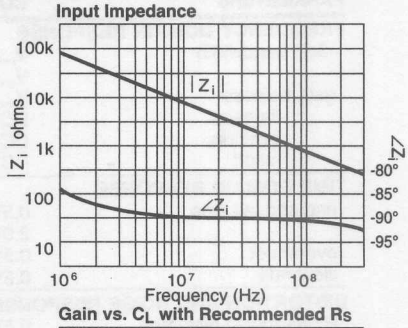
Frequency Response vs. Output Swing



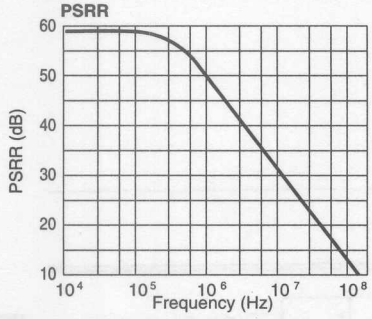
Output Impedance



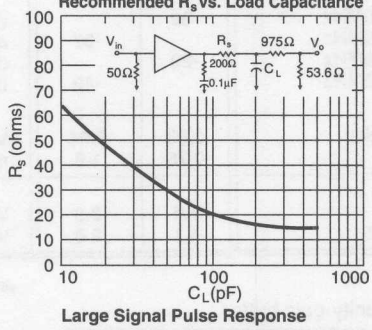
Input Impedance



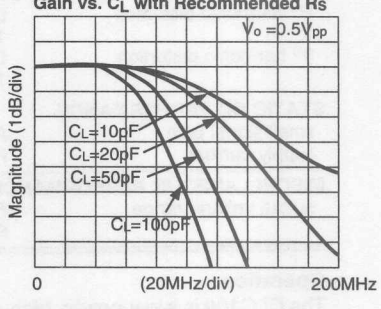
PSRR



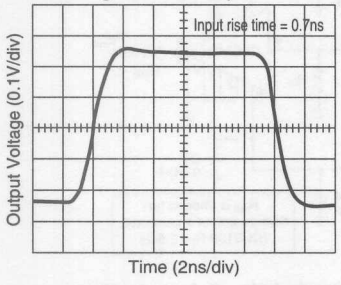
Recommended R_s vs. Load Capacitance



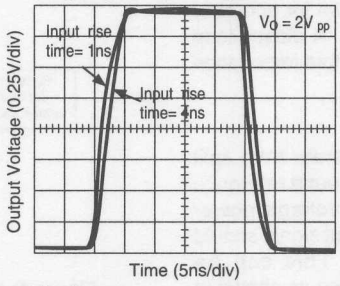
Gain vs. C_L with Recommended Rs



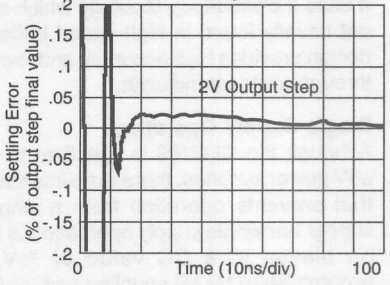
Small Signal Pulse Response



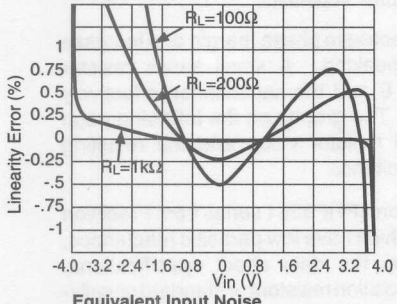
Large Signal Pulse Response



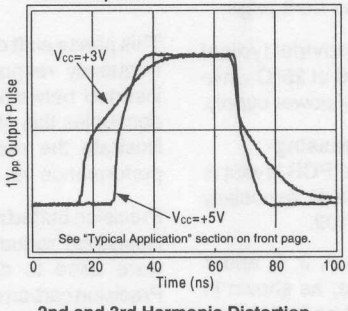
Short-Term Settling Time



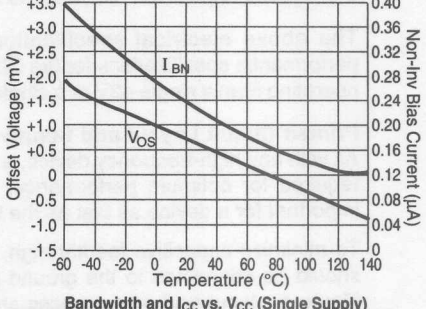
Integral Linearity Error



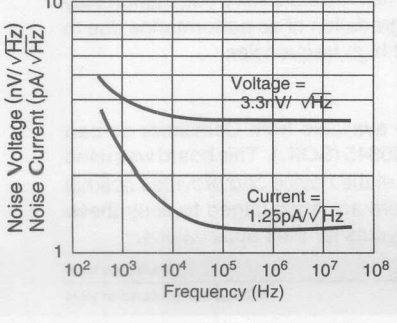
Pulse Response



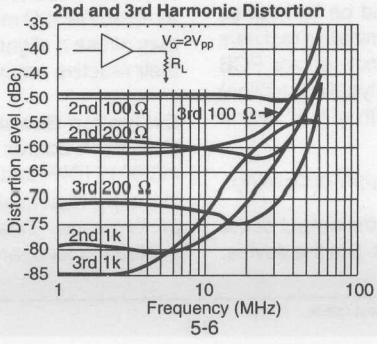
Typical D.C. Errors vs. Temperature



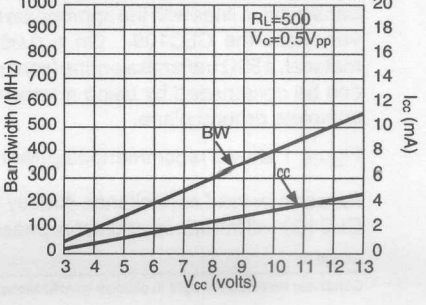
Equivalent Input Noise



2nd and 3rd Harmonic Distortion



Bandwidth and I_{CC} vs. V_{CC} (Single Supply)



Comlinear
A National Semiconductor Company

Ultra-High Slew Rate, Closed-Looped Buffer

CLC111

APPLICATIONS:

- Video switch buffers
- Test point drivers
- High frequency active filters
- Wideband DC clamping buffer
- High-speed peak detector circuits

FEATURES:

- Very wideband (800MHz)
- Ultra-high (3500V/µs) slew rate
- Very low output impedance (1.4Ω)
- Low (-62dBc) 2nd/3rd harmonics @ 20MHz
- 60mA output current (±5 supplies)
- Single supply operation (0 to 3V supply min.)
- Evaluation boards and Spice models

DESCRIPTION

The CLC111 is a high-performance, closed-loop, monolithic buffer designed for applications requiring very high-frequency signals. The CLC111's high performance includes an extremely fast 800MHz small signal bandwidth ($0.5V_{pp}$) and an ultra high (3500V/µs) slew rate while requiring only 10.5mA quiescent current. Signal fidelity is maintained with low harmonic distortion (-62dBc 2nd and 3rd harmonics at 20MHz). These performance characteristics are for a demanding 100Ω load.

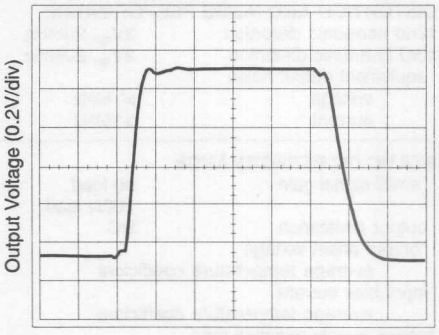
Featuring a patented closed-loop design, the CLC111 offers nearly ideal unity-gain (0.996) with very low (1.4Ω) output impedance. The CLC111 is ideally suited for buffering video signals with its 0.15%/0.04° differential gain and phase performance at 4.43MHz. Power sensitive applications will benefit from the CLC111's excellent performance on reduced or single supply voltages.

Constructed using an advanced, complementary bipolar process and Comlinear's proven high-performance architectures, the CLC111 is available in several versions to meet a variety of requirements.

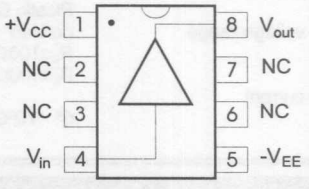
CLC111AJP	-40°C to +85°C	8-pin Plastic DIP
CLC111AJE	-40°C to +85°C	8-pin Plastic SOIC
CLC111AIB	-40°C to +85°C	8-pin hermetic CERDIP
CLC111A8B	-55°C to +125°C	8-pin hermetic CERDIP, MIL-STD-883, Level B
CLC111ALC	-55°C to +125°C	dice
CLC111AMC	-55°C to +125°C	dice qualified to Method 5008, MIL-STD-883, Level B

Contact factory for other packages and DESC SMD number.

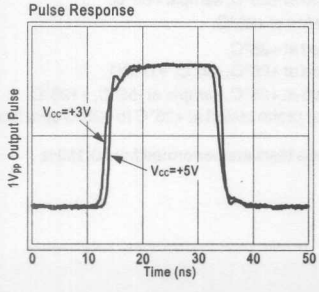
Pulse Response for ±5V

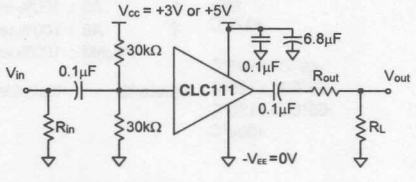


PINOUT
DIP & SOIC

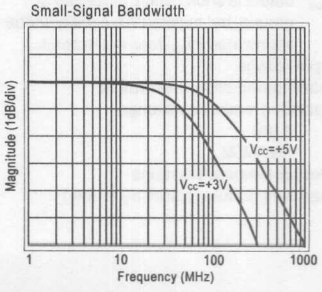


TYPICAL APPLICATION





Single-Supply Circuit



Comlinear Corporation • 4800 Wheaton Drive • Fort Collins, CO 80525 • (800) 776-0500 • FAX (970) 226-6761

5

CLC111 Electrical Characteristics ($\pm V_{cc} = \pm 5V$, $R_L = 100\Omega$ unless specified)

PARAMETER	CONDITIONS	TYP	MIN AND MAX RATINGS			UNITS	SYMBOL
Ambient Temperature	CLC109AJ/AI	+25°C	-40°C	+25°C	+85°C		
	CLC109A8/AM/AL	+25°C	-55°C	+25°C	+125°C		
FREQUENCY RESPONSE							
†small signal bandwidth	$V_{out} < 0.5V_{pp}$	800	400	400	300	MHz	SSBW
	$V_{out} < 4.0V_{pp}$	450	250	250	200	MHz	LSBW
gain flatness[1]	$V_{out} < 0.5V_{pp}$						
† flatness	DC-50MHz	0.02	±0.1	±0.1	±0.2	dB	GFL
† peaking	DC-200MHz	0.1	1.0	0.5	0.5	dB	GFPH
† rolloff	DC-200MHz	0.1	0.8	0.8	1.2	dB	GFRH
differential gain	4.43MHz, 150Ω load	0.15	0.4	0.25	0.25	%	DG
differential phase	4.43MHz, 150Ω load	0.04	0.08	0.08	0.08	°	DP
TIME DOMAIN RESPONSE							
rise and fall time	0.5V step	0.6	0.8	0.8	1.1	ns	TRS
	4.0V step	1.0	1.4	1.4	1.7	ns	TRL
settling time to ±0.1%	2.0V step	16	20	20	20	ns	TS
overshoot	4V step	0	8	5	5	%	OS1
slew rate	4V step	3500	2700	2700	2300	V/µsec	SR
DISTORTION AND NOISE PERFORMANCE							
†2nd harmonic distortion	$2V_{pp}$, 20MHz	-62	-47	-50	-50	dBc	HD2
†3rd harmonic distortion	$2V_{pp}$, 20MHz	-62	-55	-55	-52	dBc	HD3
equivalent output noise							
voltage	>1MHz	4.0	4.8	4.8	5.3	nV/√Hz	VN
current	>1MHz	1.6	4.0	3.0	3.0	pA/√Hz	ICN
STATIC DC PERFORMANCE							
small signal gain	no load	0.996	0.994	0.994	0.992	V/V	GA1
	100Ω load	0.98	0.96	0.97	0.97	V/V	GA2
output resistance	DC	1.4	3.0	2.0	2.0	Ω	RO
*output offset voltage		2	17	9	9	mV	VIO
average temperature coefficient		±30	±100		±50	µV/°C	DVIO
*input bias current		5	30	15	15	µA	IBN
average temperature coefficient		50	±187		±100	nA/°C	DIBN
†power supply rejection ratio		-52	-48	-48	-46	dB	PSRR
*supply current	no load	10.5	12	12	12	mA	ICC
MISCELLANEOUS PERFORMANCE							
integral endpoint linearity	±2V, full scale	0.2	1.0	0.5	0.5	%	ILIN
input resistance		1	0.3	0.7	1	MΩ	RIN
input capacitance	CERDIP	2.5	3.5	3.5	3.5	pF	CIN
	Plastic DIP	1.25	2.0	2.0	2.0	pF	CIN
output voltage range	no load	3.9	3.5	3.6	3.6	V	VO
	R_L=100Ω	3.5	+3.1,-2.5	3.2	3.2	V	VOL
	R_L=100Ω, 0°C		±3.1			V	VOL
output current		60	50,25	50	40	mA	IO
	0° - 70°C		50,35	50	50	mA	IO

Absolute Maximum Ratings

V_{cc}	±7.0V
I_{out} output is short circuit protected to ground, but maximum reliability will be maintained if I_{out} does not exceed...	96mA
input voltage	$\pm V_{cc}$
maximum junction temperature	+175°C
operating temperature range	
AJ/AI	-40°C to +85°C
A8/AM/AL	-55°C to +125°C
storage temperature range	-65°C to +150°C
lead temperature (soldering 10 sec)	+300°C

Miscellaneous Ratings

Notes:

* AJ,AI : 100% tested at +25°C, sample +85°C.

† AJ : Sample tested at +25°C.

† AI : 100% tested at +25°C.

* A8 : 100% tested at +25°C, -55°C, +125°C

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(note 1) : Gain flatness tests are performed from 0.1MHz

Single Supply Electrical Characteristics (V_{CC}=+3V or V_{CC}=+5V, $-V_{EE}$=0V, T_A=+25°C, R_L = 100Ω, unless noted)

PARAMETERS	CONDITIONS	V_{CC}=3V	V_{CC}=5V	UNITS
FREQUENCY DOMAIN RESPONSE				
-3dB bandwidth	V_{out} < 0.5V_{pp}	120	300	MHz
	V_{out} < 2.0V_{pp}		210	MHz
gain flatness	V_{out} < 0.5V_{pp}			
flatness	DC to 30MHz	0.5	0.1	dB
peaking	DC to 200MHz	0	0	dB
rolloff	DC to 60MHz	1.5	0.25	dB
TIME DOMAIN RESPONSE				
rise and fall time	0.5V step	3.9	1.2	ns
	2.0V step		1.5	ns
overshoot	1.0V step	3	3	%
slew rate	0.5V step	260	425	V/µs
DISTORTION AND NOISE RESPONSE				
2nd harmonic distortion	0.5V_{pp},20MHz	-46		dBc
	1.0V_{pp},20MHz		-55	dBc
3rd harmonic distortion	0.5V_{pp},20MHz	-44		dBc
	1.0V_{pp},20MHz		-64	dBc
STATIC DC PERFORMANCE				
small-signal gain	AC-coupled	0.96	0.97	V/V
supply current	R_L= ∞	2.0	4.5	mA
MISCELLANEOUS PERFORMANCE				
output voltage range	R_L= ∞	1.5	3.4	V_{pp}
	R_L=100Ω	1.1	2.6	V_{pp}

Operation

The CLC111 is a low-power, very high-speed unity-gain buffer. It uses a closed-loop topology which allows for accuracy not usually found in high-speed open-loop buffers. A slew enhanced front end allows for low quiescent power while not sacrificing ac performance.

Single Supply Operation

Although the CLC111 is specified to operate from split ±5V power supplies, there is no internal ground reference that prevents operation from a single voltage power supply. For single supply operation the input signal should be biased at a DC value of ½V_{CC}. This can be accomplished by AC coupling and rebiasing as shown in Figure 1.

The above electrical specifications provide typical performance specifications for the CLC111 at 25°C while operating from a single +3V or a single +5V power supply.

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As with any high-frequency device, a good PCB layout is required for optimum performance. This is especially important for a device as fast as the CLC111.

To minimize capacitive feedthrough, pins 2, 3, 6, and 7 should be connected to the ground plane, as shown in Figure 1. Input and output traces should be laid out as transmission lines with the appropriate termination resistors very near the CLC111. On a 0.065 inch epoxy PCB material, a 50Ω transmission line (commonly called stripline) can be constructed by using a trace width of 0.1" over a complete ground plane.

Figure 1 shows recommended power supply bypassing.

The ferrite beads are optional and are recommended only where additional isolation is needed from high-frequency (>400MHz) resonances in the power supply.

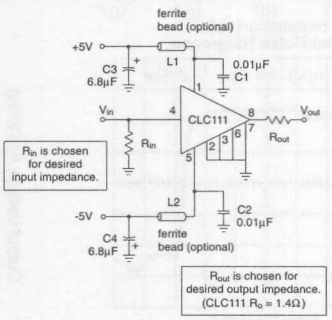

Figure 1: Recommended circuit & evaluation board schematic

Parasitic or load capacitance directly on the output of the CLC111 will introduce additional phase shift in the device. This phase shift can decrease phase margin and increase frequency response peaking. A small series resistor before the capacitance effectively decouples this effect. The graphs on the following page illustrate the required resistor value and the resulting performance vs. capacitance.

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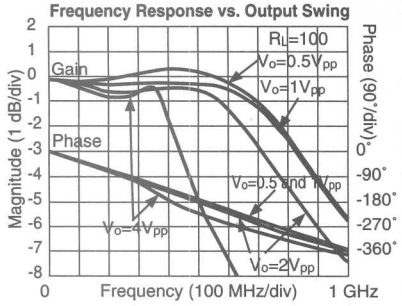
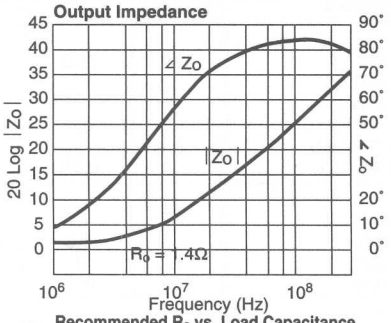
Typical Performance Characteristics (T_A = +25°C, V_{cc} = ± 5V, R_L = 100Ω unless specified)

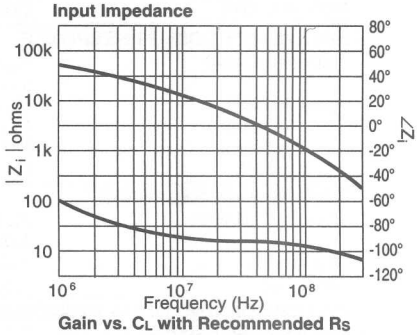
Frequency Response vs. Output Swing



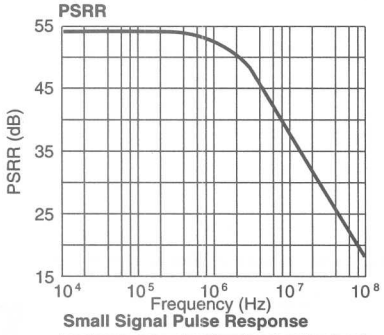
Output Impedance



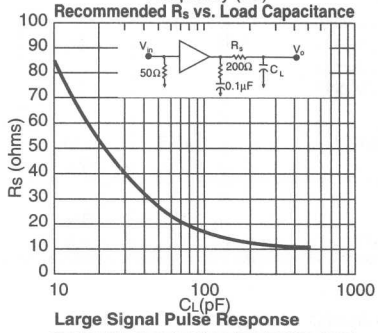
Input Impedance



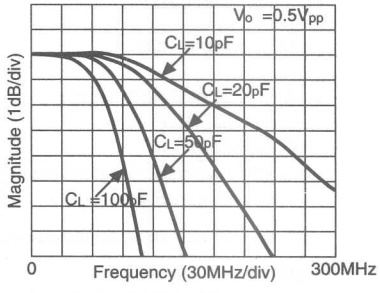
PSRR



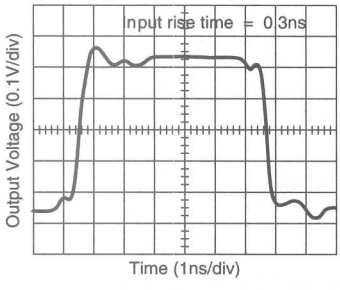
Recommended R_S vs. Load Capacitance



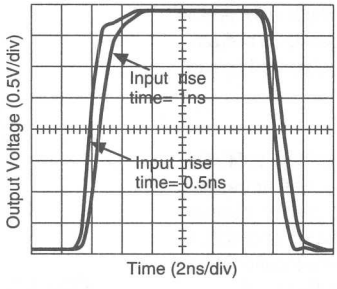
Gain vs. C_L with Recommended R_S



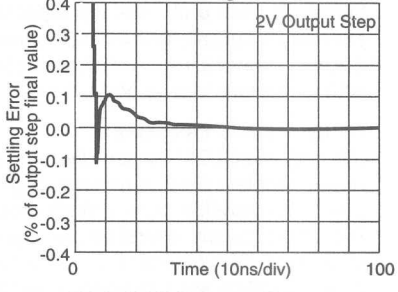
Small Signal Pulse Response



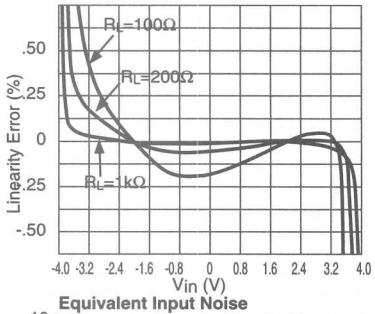
Large Signal Pulse Response



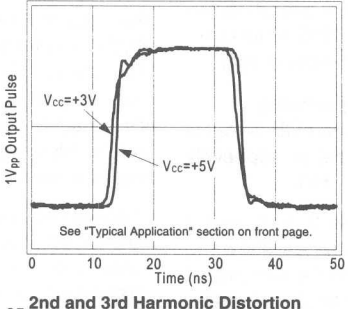
Short-Term Settling Time



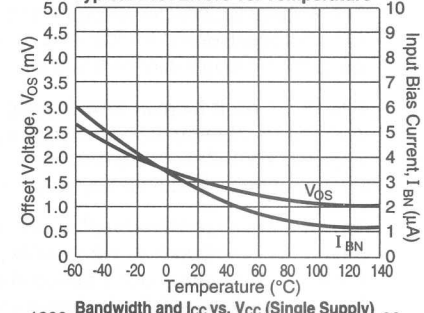
Integral Linearity Error



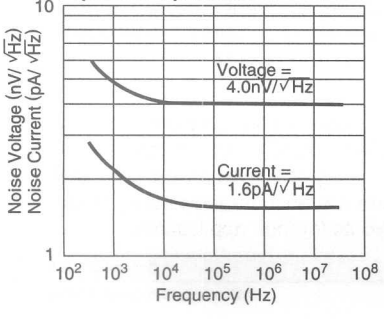
Pulse Response



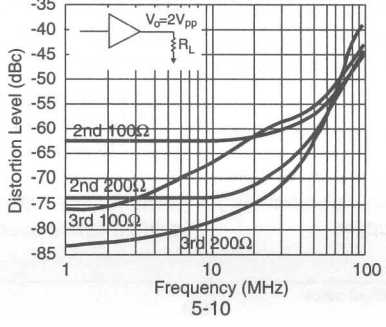
Typical D.C. Errors vs. Temperature



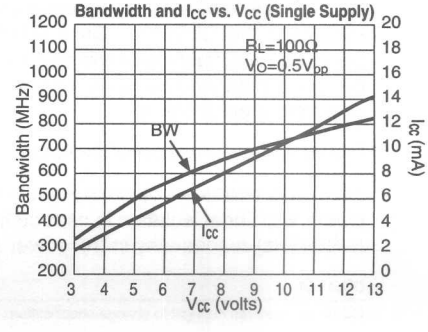
Equivalent Input Noise



2nd and 3rd Harmonic Distortion



Bandwidth and I_{CC} vs. V_{CC} (Single Supply)



Analog Multiplexers
Contents

6

Comlinear
A National Semiconductor Company

High-Speed 4:1 Analog Multiplexer

CLC533

APPLICATIONS:
- Infrared system multiplexing
- CCD sensor signals
- Radar I/Q switching
- High definition video HDTV
- Test and calibration

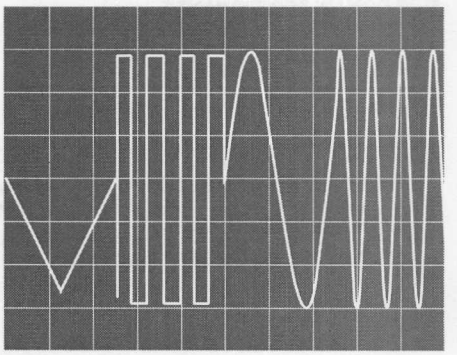
FEATURES:
- 12-bit settling (0.01%) – 17ns
- Low noise – 42μVrms
- Isolation – 80dB @ 10MHz
- 110MHz -3dB bandwidth (A_V = +2)
- Low distortion – 80dB @ 5MHz
- Adjustable bandwidth – 180MHz (max)

DESCRIPTION

The CLC533 is a high-speed 4:1 multiplexer employing active input and output stages. The CLC533 also employs a closed-loop design which dramatically improves accuracy over conventional analog multiplexer circuits. This monolithic device is constructed using an advanced high-performance bipolar process.

The CLC533 has been specifically designed to provide a 24ns settling time to 0.01%. This coupled with the adjustable bandwidth, makes the CLC533 an ideal choice for infrared and CCD imaging systems, with channel-to-channel isolation of 80dB @ 10MHz. Low distortion and spurious signal levels (-80dBc) make the CLC533 a very suitable choice for I/Q processors in radar receivers.

The CLC533 is offered over both the industrial and military temperature ranges. The industrial versions, CLC533AJP\AJE\AIB, are specified from -40°C to +85°C and are packaged in 16-pin plastic DIPs, SOIC's and CERDIP packages. The extended temperature versions, CLC533A8B/A8L-2A, are specified from -55°C to +125°C and are packaged in 16-pin CERDIP and 20-terminal LCC packages.



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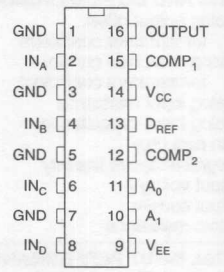
Ordering Information ...

CLC533AJP	-40°C to +85°C	16-pin plastic DIP
CLC533AJE	-40°C to +85°C	16-pin plastic SOIC
CLC533AIB	-40°C to +85°C	16-pin CERDIP
CLC533A8B	-55°C to +125°C	16-pin CERDIP, MIL-STD-883
CLC533A8L-2A	-55°C to +125°C	20-terminal LCC, MIL-STD-883

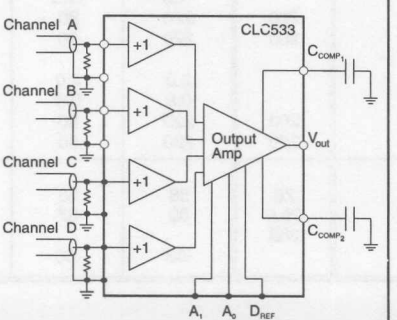
PINOUT
DIP & SOIC

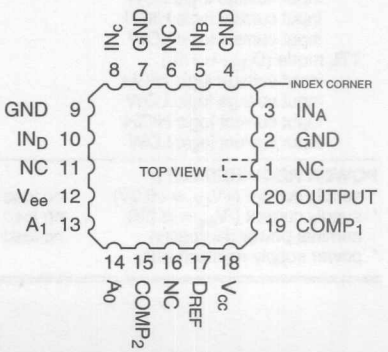


FUNCTIONAL DIAGRAM

A_1	A_0	OUT
0	0	A
0	1	B
1	0	C
1	1	D

ECL Mode - D_{REF} = open
TTL Mode - D_{REF} = +5V





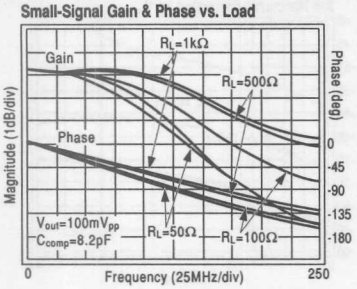
Comlinear Corporation • 4800 Wheaton Drive • Fort Collins, CO 80525 • (800) 776-0500 • FAX (970) 226-6761 • Internet: clc_apps@cc.com

CLC533 Electrical Characteristics ($+V_{cc}$ = +5.0V; $-V_{ee}$ = -5.2V; R_{in} = 50Ω; R_L = 500Ω; C_{COMP} = 8pf; ECL Mode, pin 13 = NC)

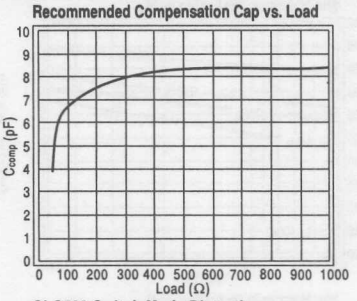
PARAMETERS	CONDITIONS	TYP	MIN & MAX RATINGS[2]			UNITS	SYMBOL
Ambient Temperature	CLC533A8B/A8L-2A	+25°C	-55°C	+25°C	+125°C		
Ambient Temperature	CLC533AJP/AJE/AIB	+25°C	-40°C	+25°C	+85°C		
FREQUENCY DOMAIN RESPONSE							
† -3dB bandwidth	$V_{OUT} < 0.1V_{pp}$	180	130	130	110	MHz	SSBW
-3dB bandwidth	$V_{OUT} = 2V_{pp}$	45	35	35	30	MHz	LSBW
† gain flatness	$V_{OUT} < 0.1V_{pp}$						
peaking	0.1MHz to 200MHz	0.2	0.5	0.5	0.5	dB	GFP
rolloff	0.1MHz to 100MHz	1.0	2.0	2.0	3.0	dB	GFR
linear phase deviation	dc to 100MHz	2.0				deg	LPD
crosstalk rejection - 1 channel	$2V_{pp}$, 10MHz	80	74	74	74	dB	CT10
	$2V_{pp}$, 20MHz	74	68	68	68	dB	CT20
	$2V_{pp}$, 30MHz	68	62	62	62	dB	CT30
crosstalk rejection - 3 channels	$2V_{pp}$, 10MHz	80	74	74	74	dB	3CT10
	$2V_{pp}$, 20MHz	74	68	68	68	dB	3CT20
	$2V_{pp}$, 30MHz	68	62	62	62	dB	3CT30
TIME DOMAIN PERFORMANCE							
rise and fall time	0.5V step	2.7	3.3	3.3	3.8	ns	TRS
	2V step	10	12.5	12.5	14.5	ns	TRL
settling time[2] 2V step	±0.01%	17	24	24	27	ns	TSP
	±0.1%	13	18	18	21	ns	TSS
overshoot	2.0V step	2	5	5	6	%	OS
slew rate		160	130	130	110	V/µs	SR
SWITCH PERFORMANCE							
channel to channel switching time	50% SELECT to 10%V_{OUT}	6	8	8	9	ns	SWT10
(2V step at output)	50% SELECT to 90%V_{OUT}	16	21	21	24	ns	SWT90
switching transient		30				mV	ST
DISTORTION AND NOISE PERFORMANCE							
† 2nd harmonic distortion	$2V_{pp}$, 5MHz	80	67	67	67	dBc	HD2
† 3rd harmonic distortion	$2V_{pp}$, 5MHz	86	67	67	67	dBc	HD3
equivalent input noise							
spot noise voltage	> 1MHz	4.2				nV/√Hz	SNF
integrated noise	1MHz to 100MHz	42	54		51	mVrms	INV
spot noise current		5				pA/√Hz	SNF
STATIC AND DC PERFORMANCE							
* analog output offset		1	12	3.5	4.5	mV	VOS
temperature coefficient		15	90		20	µV/°C	DVIO
* analog input bias current		50	280	120	120	µA	IBN
temperature coefficient		0.3	2.0		0.8	µA/°C	DIBN
analog input resistance		200	90	120	120	kΩ	RIN
analog input capacitance		2	3.0	2.5	2.5	pF	CIN
* gain accuracy	±2V	0.994	0.988	0.988	0.988	V/V	GA
integral endpoint linearity	±1V (full scale)	0.02	0.05	0.03	0.03	%FS	ILIN
output voltage	no load	±3.4	2.4	2.8	2.8	V	VO
output current		45	20	50	50	mA	IO
output resistance	DC	1.5	4.0	2.5	2.5	Ω	RO
DIGITAL INPUT PERFORMANCE							
ECL mode (D_{REF} floating)							
input voltage logic HIGH			-1.1	-1.1	-1.1	V	VIH1
input voltage logic LOW			-1.5	-1.5	-1.5	V	VIL1
input current logic HIGH		200	220	80	80	µA	IIH1
input current logic LOW		200	220	80	80	µA	IIL1
TTL mode (D_{REF} = +5V)							
input voltage logic HIGH			2.0	2.0	2.0	V	VIH2
input voltage logic LOW			0.8	0.8	0.8	V	VIL2
input current logic HIGH		200	220	80	80	µA	IIH2
input current logic LOW		200	220	80	80	µA	IIL2
POWER REQUIREMENTS							
* supply current ($+V_{CC}$ = +5.0V)	no load	28	38	36	36	mA	ICC
* supply current ($-V_{ee}$ = -5.2V)	no load	28.5	39	37	37	mA	IEE
nominal power dissipation	no load	288				mW	PD
* power supply rejection ratio			-53	-60	-60	dB	PSRR

CLC533 Typical Performance Characteristics (T_A = 25°C, $+V_{CC}$ = +5V, $-V_{EE}$ = -5.2V, R_L = 500Ω unless specified)

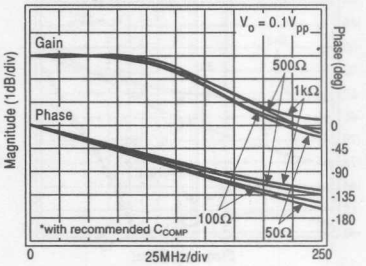
Small-Signal Gain & Phase vs. Load



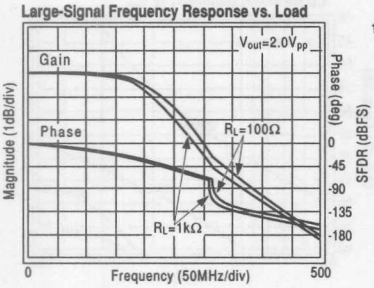
Recommended Compensation Cap vs. Load



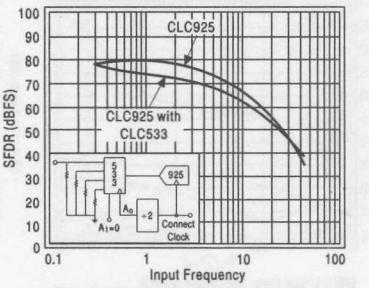
Small Signal Gain/Phase vs. Load*



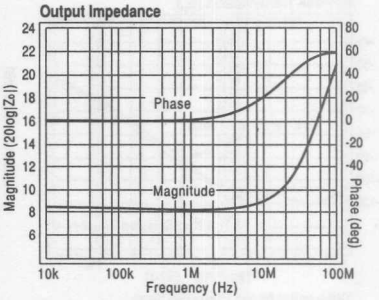
Large-Signal Frequency Response vs. Load



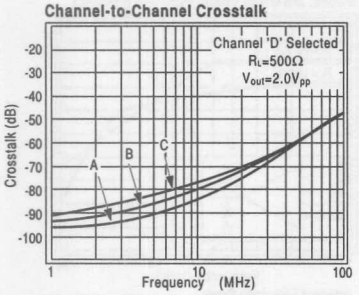
CLC533 Switch Mode Distortion



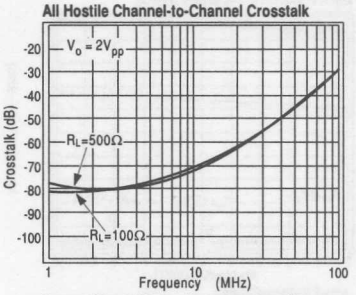
Output Impedance



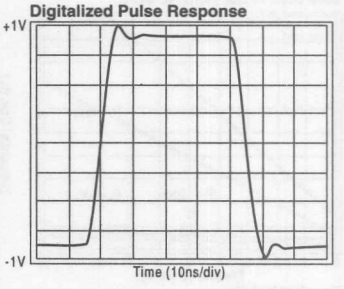
Channel-to-Channel Crosstalk



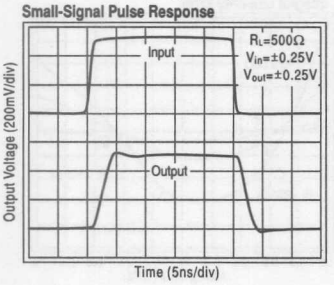
All Hostile Channel-to-Channel Crosstalk



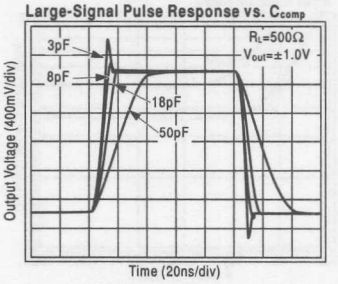
Digitalized Pulse Response



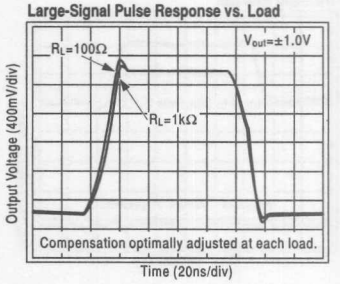
Small-Signal Pulse Response



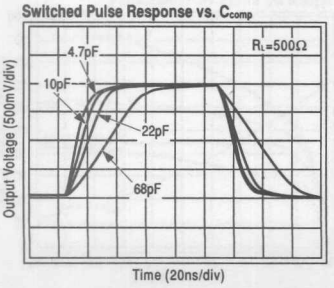
Large-Signal Pulse Response vs. C_{comp}



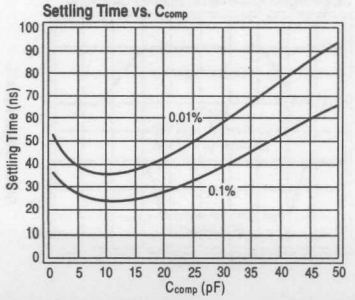
Large-Signal Pulse Response vs. Load



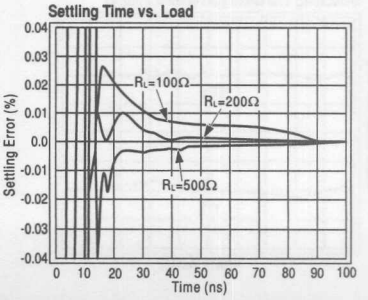
Switched Pulse Response vs. C_{comp}



Settling Time vs. C_{comp}



Settling Time vs. Load



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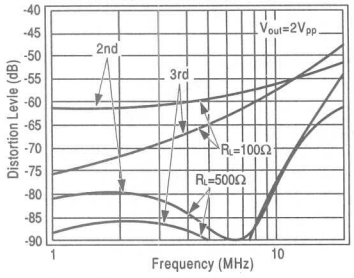
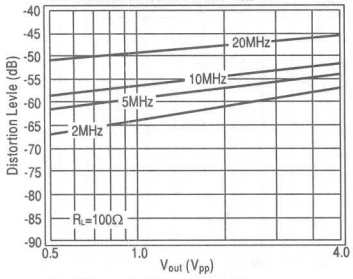
CLC533 Typical Performance Characteristics (T_A = 25°C, $+V_{CC}$ = +5V, $-V_{EE}$ = -5.2V, R_L = 500Ω unless specified)

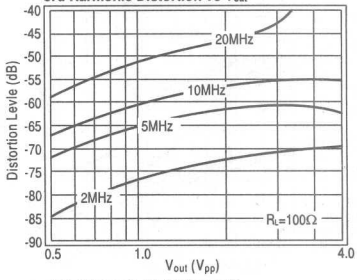
2nd & 3rd Harmonic Distortion



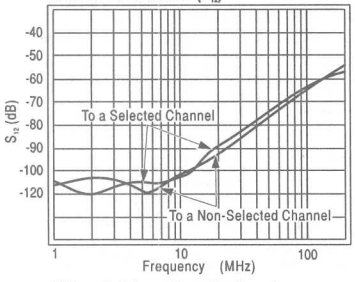
2nd Harmonic Distortion vs V_{out}



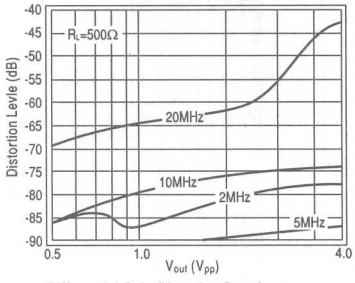
3rd Harmonic Distortion vs V_{out}



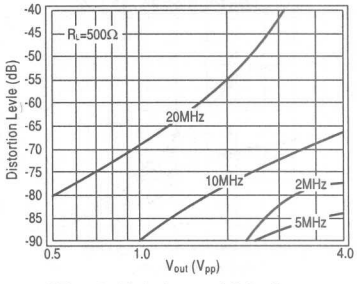
Reverse Transmission (S_{12})



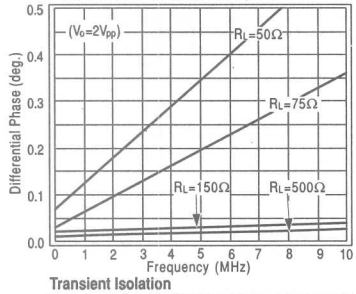
2nd Harmonic Distortion vs V_{out}



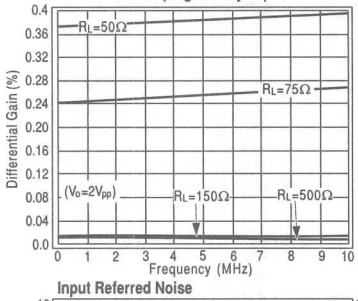
3rd Harmonic Distortion vs V_{out}



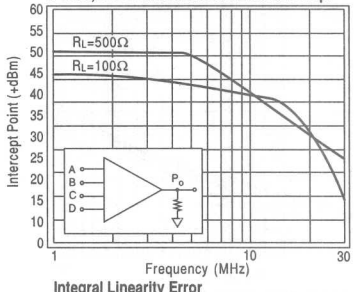
Differential Phase (Negative Sync.)



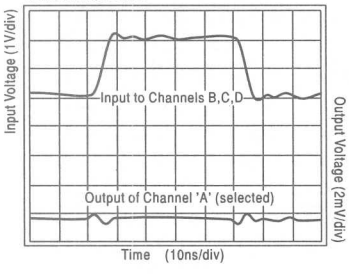
Differential Gain (Negative Sync.)



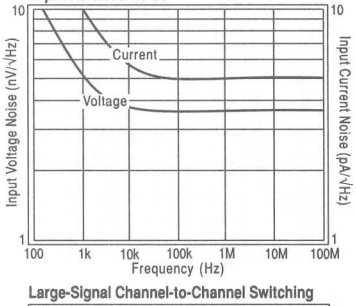
2-Tone, 3rd Order Intermodulation Intercept



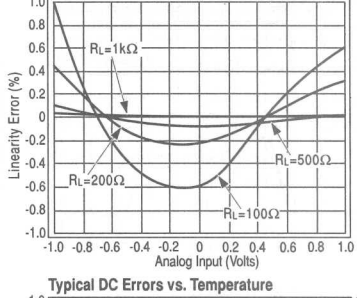
Transient Isolation



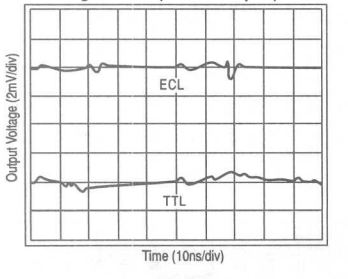
Input Referred Noise



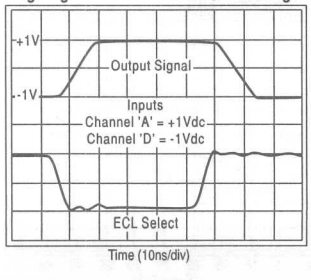
Integral Linearity Error



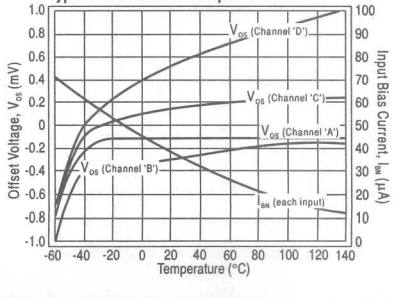
Switching Transient (Grounded Inputs)



Large-Signal Channel-to-Channel Switching



Typical DC Errors vs. Temperature



Recommended Operating Conditions

positive supply voltage ($+V_{cc}$)	+5.0V
negative supply voltage ($-V_{ee}$)	-5.2V
differential voltage between any two GND's	10mV
analog input voltage range	±2V
A_X input voltage range (TTL mode)	0V to +5.0V
A_X input voltage range (ECL mode)	0V to -2.0V
C_{COMP} range	5pF to 100pF

thermal data	θ_{jc}(°C/W)	θ_{ja}(°C/W)
16-pin plastic	50	60
16-pin Cerdip	20	65
16-pin SOIC	60	75
20-terminal LCC	20	35
16-pin side brazed	20	50

Absolute Maximum Ratings[3]

positive supply voltage ($+V_{cc}$)	-0.5V to +7.0V
negative supply voltage ($-V_{ee}$)	+0.5V to -7.0V
differential voltage between any two GND's	200mV
analog input voltage range	$-V_{ee}$ to $+V_{cc}$
digital input voltage range	$-V_{ee}$ to $+V_{cc}$
output short circuit duration (shorted to GND)	Infinite
junction temperature	+175°C
operating temperature range	
CLC533AJP/AJE/AIB	-40°C to +85°C
CLC533A8B/A8L-2A	-55°C to +125°C
storage temperature range	-65°C to +150°C
lead solder duration (+300°C)	10 sec

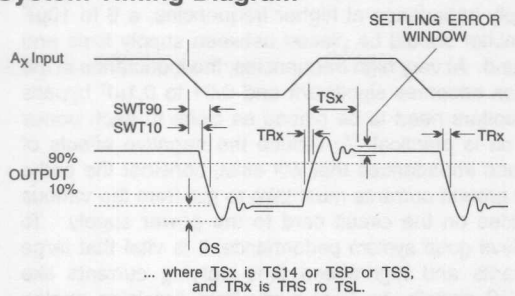
Note 1: Test levels are as follows:

* AI/AJ : 100% tested at +25°C, sample at +85°C.
† AJ : Sample tested at +25°C.
† AI : 100% tested at +25°C.
* A8 : 100% tested at +25°C, -55°C, +125°C.
† A8 : 100% tested at +25°C, sample at -55°C, +125°C.

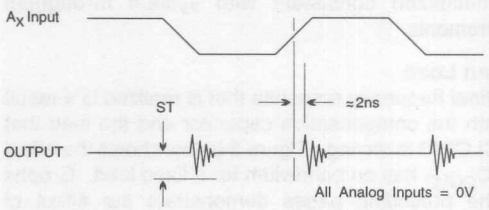
Note 2: Settling time measured from the 50% analog output transition.

Note 3: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

System Timing Diagram



Switching Transient Timing Diagram



6

APPLICATIONS INFORMATION

Operation

The CLC533 is a 4:1 analog multiplexer designed with a closed loop architecture to provide very low harmonic distortion and superior channel to channel isolation. This low distortion, coupled with very fast switching speed make the CLC533 an ideal multiplexer for data conversion applications. User selectable ECL or TTL select logic adds to the versatility of this device. External frequency response compensation allows the performance of the CLC533 to be optimized for each application.

Digital Interface and Channel Select

The CLC533 has two channel select pins which can be used to select any one of the four inputs. These digital inputs can be configured to meet TTL, ECL or CMOS logic levels with the D_{REF} pin. If D_{REF} is left open, then the A_0 and A_1 select inputs will respond to ECL 10K switching levels (Figure 1). For TTL or CMOS levels, D_{REF} should be tied to V_{cc} (Figure 2). There is an internal series resistor which makes it possible to connect D_{REF} directly to the power supply. Select pins according to the truth table shown on the front page. A more positive voltage is considered to be a logic '1'. Therefore with no connection to A_0 or A_1 the internal pull-up resistors will select the D input to be passed through to the output.

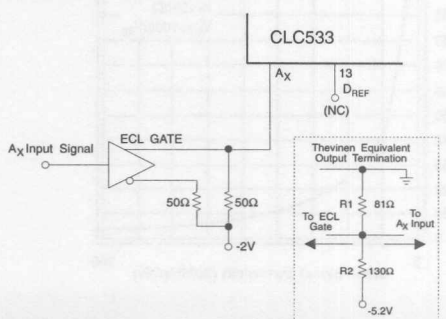


Figure 1: ECL Level Channel SELECT Configuration

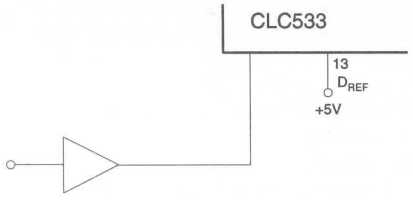


Figure 2: TTL/CMOS Level Channel SELECT Configuration

Compensation

The CLC533 is externally compensated, allowing the user to select the bandwidth that best suits the application. Decreasing bandwidth has two advantages: lower noise and lower switching transients. In a sampled system, noise at frequencies above 1/2 the sampling frequency will be aliased into the baseband and will corrupt the signal of interest. When the CLC533 is switched from one channel to another, the output slews rapidly until it arrives at the new signal. This high slew rate signal can capacitively couple into other nodes in the circuit and can have a detrimental effect on overall performance. Since coupling through stray capacitance and inductances decreases with decreasing dV/dt, the slew rate should be minimized consistent with system throughput requirements.

Output Load

The final frequency response that is realized is a result of both the compensation capacitor and the load that the CLC533 is driving. Figure 3 below shows the effect that C_{COMP} has on bandwidth for a fixed load. Graphs on the preceding pages demonstrate the effect of C_{COMP} on pulse response and settling time, and the optimum value of C_{COMP} to maximize bandwidth for various amounts of resistive loading. Because there are so many factors that go into determining the optimum value of C_{COMP} it is recommended that once a value is selected, the application circuit be built up and larger and smaller compensation capacitors be tried to determine the best value for that particular circuit.

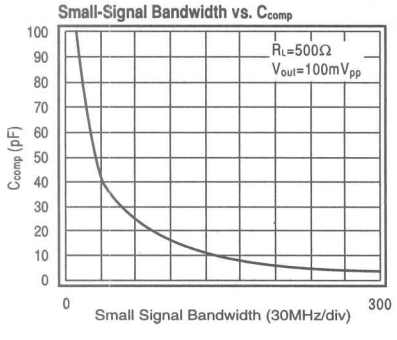


Figure 3

The output load that the CLC533 is driving has an effect on the harmonic distortion of the device as well as frequency response. Distortion is minimized with a 500Ω load. When driving components with a high input impedance, addition of a load resistor can improve the performance. If the load is capacitive in nature, it should be isolated from the CLC533 output via a series resistor. The recommended series resistor R_S, for various capacitive loads C_L, can be found by referring to the "Recommended Compensation Cap vs. Load" plot in the "Typical Performance" section.

Power Supplies and Grounding

In any circuit there are connections between components that are not desired. Some of the most common of these are the connections made through the power supply and grounding network. The goal in laying out the power and ground network for a mixed mode circuit is to minimize the impedance from the power pins to the supply, and minimize the impedance of the ground network.

To minimize impedance of the ground and power nets, use the heaviest possible traces and ground planes for minimizing the DC impedance. To further reduce the supply impedance at higher frequencies, a 6 to 10μF capacitor should be placed between supply lines and ground. At very high frequencies, the inductance in the traces becomes significant and 0.01 to 0.1μF bypass capacitors need to be placed as close to each power pin as is practical. To reduce the negative effects of ground impedances that will exist, consider the paths that ground currents must take to get from the various devices on the circuit card to the power supply. To achieve good system performance, it is vital that large currents and high-speed time varying currents like CMOS signals, be kept away from precision analog components. This can be achieved through layout of the power and ground nets. Using a ground plane split between analog and digital sections of the circuit forces all of the ground current from the digital circuits to go directly to the power connector without straying to the analog side of the card.

Optimizing for Channel-to-Channel Isolation

Although the CLC533 has excellent channel-to-channel isolation, if there is cross talk between the input signals before they reach the CLC533, the multiplexer will faithfully pass these corrupted signals through to its output and dutifully take the blame for poor isolation. The CLC533 evaluation board has successfully demonstrated in excess of 80dB of isolation and can be considered to be a model for the layout of boards requiring good isolation. The evaluation board has input signal traces shielded by a guard ring as shown in Figure 4. These guard rings help to prevent ground return currents from other channels finding their way into the selected channel. If there are input termination resistors, care must be taken that the

ground return currents between resistors cannot interfere with each other. Use of chip resistors allows for best isolation, and if the guard ring around the input trace is used for the termination resistor ground, then the ground currents for each input are forced to take paths away from one another.

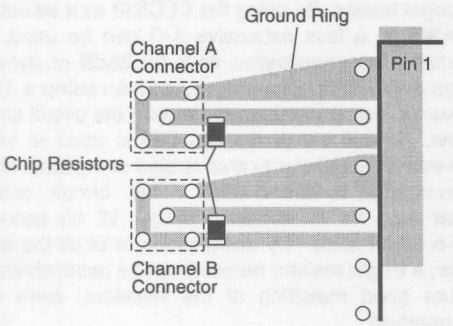


Figure 4: Analog Input Using Guard Ring

Use of the CLC533 with an Analog-to-Digital Converter

To get the most out of the combination of multiplexer and ADC, a clear understanding of both converter operation and multiplexer operation is required. Careful attention to the timing of the convert signal to the ADC and the channel select signal to the CLC533 is one key to optimizing performance.

To obtain the best performance from the combination, the output of the CLC533 must be a valid representation of the selected input at the time that the ADC samples it. The time at which the ADC samples the input is determined by the type of ADC that is being used. Subranging ADCs usually have a Track-and-Hold (T/H) at their input. For a successful combination of the multiplexer and the ADC, the multiplexer timing and the T/H timing must be compatible. When the ADC is given a convert command, the T/H transitions from Track mode to Hold mode. The delay between the convert command and this transition is usually specified as Aperture Delay or as Sampling Time Offset. To maximize the time that the multiplexer has to settle and the T/H has to acquire the signal, the multiplexer should begin its transition from one input to the other immediately after the T/H transition has taken place. However it is during this period of time that a subranging ADC is performing analog processing of the sampled signal, and high slew rate transitions on the input may feed through to the sample being converted. To minimize this interaction there are two strategies that can be taken: strategy one applies when the sample rate of the system is below the rated speed of the converter. Here the select timing is delayed so that the multiplexer transition takes place after the A/D has completed one conversion cycle and is waiting for the next convert command. As an example: a CLC935 (15Msps) A/D converter is being used at 10 MHz, the conversion takes place in the first 67ns after the convert command, the next 33ns are spent waiting for the next convert command and would be an ideal time to transition the multiplexer from one channel to the next. The second optimization strategy involves lowering the analog input slew rate so that it has fewer high frequency components that might feed through to the hold capacitor while the converter's T/H is in hold mode. This slew rate limitation can be done through the use of the external CLC533 compensation capacitors. Use of this method has the advantage of limiting some of the excess bandwidth that the CLC533 has compared to the ADC. This bandwidth limitation will reduce the amount of high frequency noise that is aliased back into the sampled band. Figure 5 shows recommended C_{COMP} values that can be used as a function of ADC Sample rate. Since the optimal values will change from one ADC to the next, this graph should be used as a starting point for C_{COMP} selection.

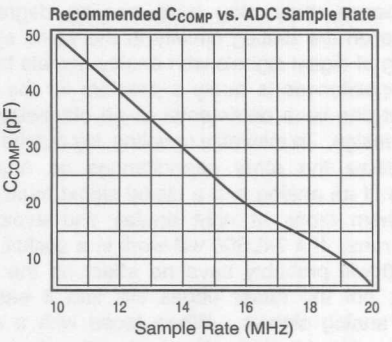


Figure 5

Flash ADCs are similar to subranging ADCs in that the sampling period is very brief. The primary difference is that the acquisition time of a flash converter is much shorter than that of a subranging A/D. With a flash ADC the transition of the mux output should be after the sampling instant (Aperture delay after the convert command). The periods of time during which the internal circuitry in a flash converter is sensitive to external disruptions are relatively brief. It is only during these points in time that the converter is susceptible to interference from the input. It may be found that a slight delay between the ADC clock and the CLC533 select lines will have a positive effect on overall performance.

Mixed Mode Circuit Design

In any mixed mode circuit care must be taken to keep the high slew-rate digital signals from interfering with the high precision analog signals. A successful design will take this into consideration from many angles and will account for it in digital timing, logic family selected, PCB layout, analog signal bandwidth and a myriad of other aspects. Below are a few tips that should be kept in mind when designing a circuit that involves both analog and digital circuitry.

6

Timing

If the analog signals going through the CLC533 are to be sampled, try to minimize the amount of digital logic switching concurrent with the sampling instant.

Power Supply Net

In an analog system the ideal situation would have each circuit element completely isolated from all others except for the intended connections. One of the most common ways for unwanted connections to be made is through the power supplies and ground. These are often shared by all of the circuits in the system. Refer to the section on power supplies and grounding for tips on how to avoid these pitfalls.

Logic Family Selection

When designing digital logic, there are often several logic families that will provide a solution to the problem at hand. Although they may perform equally in a digital sense, they may have varying degrees of influence on the analog circuits in the same system. Coupling of digital signals with analog signals through stray capacitances is rarely a problem for the digital logic but can be a detrimental to an otherwise good analog design. To minimize coupling, lay out the board to minimize the stray capacitances as much as possible: if an analog and a digital signal must cross, make them cross at right angles and avoid long parallel runs. If a 74LS00 will work in a socket, using a 74F00 will probably have no effect on the digital circuitry, but the faster edges will find it easier to corrupt analog signals. When faced with a choice between several logic families, select the slowest one possible to get the job done. Don't forget that the slew rates of digital logic depend not only on the rise and fall times, but on the output swing as well. ECL gates with a 1ns rise time have much slower slew rates than TTL gates with the same rise times. Do not attempt to slow logic edge rates through the addition of capacitance on the logic lines.

The negative effects that digital logic has on power supplies is not constant through different logic families. CMOS logic draws current only during transitions. The surge currents that it draws at these times can be quite significant and can be very disruptive to the power and ground networks. ECL tends to draw constant amounts of current and has a much smaller effect on the power net.

Gain Selection for an ADC

In many applications, such as RADAR, the dynamic range requirements may exceed the accuracy requirements. Since wide dynamic range ADCs are also typically highly accurate ADCs this often leads the designer into an ADC which is a technical overkill and a budget buster. By using the CLC533 as a selectable gain stage, a less expensive A/D can be used. For example, if an application calls for 85dB of dynamic range and 0.05% accuracy, rather than using a 16 bit converter, use a 12 bit converter with the circuit shown below. In this circuit the CLC533 is used to select between the input signal and version of the input signal attenuated by 6, 12 and 18dB. This circuit affords better than 14 bit dynamic range, 12 bit accuracy and a 12 bit price. By using resistors of all the same value, a single resistor network can be used which can assure good matching of the resistors, even over temperature.

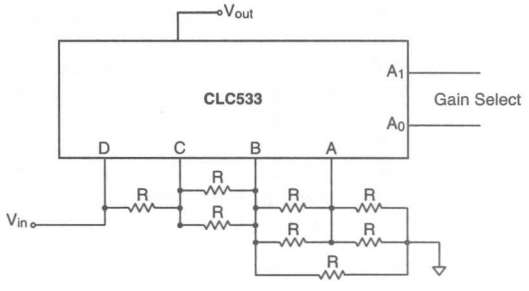


Figure 6

Evaluation Board

Evaluation boards are available for both the DIP versions (Part number 730035) and SOIC version (part number 730039) of the CLC533. These boards can be used for fast, trouble free evaluation and characterization of the CLC533. Additionally this board serves an example of a successful PCB layout that can be copied into applications circuits. A separate data sheet for the evaluation board can be obtained from Comlinear.

Applications Support

Comlinear maintains a staff of applications engineers who are available for design and applications assistance. To make use of this service call **(800) 776-0500 or (970) 225-7422.**

Analog-to-Digital Converters

Contents

Comlinear
A National Semiconductor Company

12-Bit A/D Converters
15 to 30.72MSPS

CLC935, 936, 937, & 938

APPLICATIONS:

- Electronic Imaging
- Digital Communications
- IF sampling
- Radar processing
- FLIR processing
- Instrumentation

FEATURES:

- Pin-Compatible Family
- Wide Dynamic Range
  - 82dB SFDR; F_{in} = 400kHz
  - 81dB IMD; F_{in} = 3.5MHz & 3.7MHz
  - 65dB SNR; F_{in} = 7MHz
- Fast Recovery Time
- 0.6 LSB Differential Linearity Error

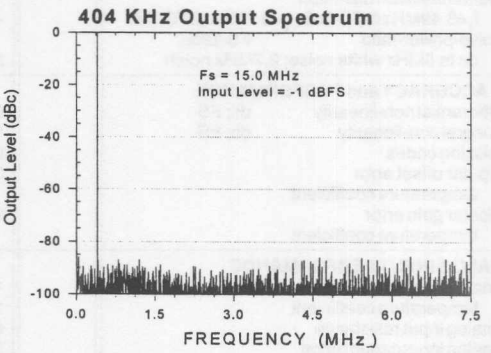
DESCRIPTION

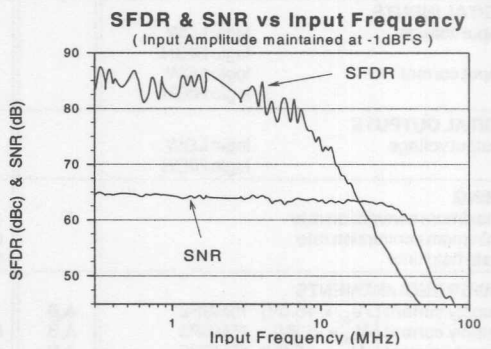
The CLC935, CLC936, CLC937, and CLC938 are a pin-compatible family of high-speed high-performance 12-bit Analog-to-Digital converters. All four converters are complete A/D subsystems, including 12-bit quantizer, track-and-hold, and references. This family of ECL compatible A/Ds have maximum sample rates of 15, 20, 25.6, and 30.72 MSPS, allowing the user to optimize performance over a wide range of sample rates without changes to PC boards or fixtures.

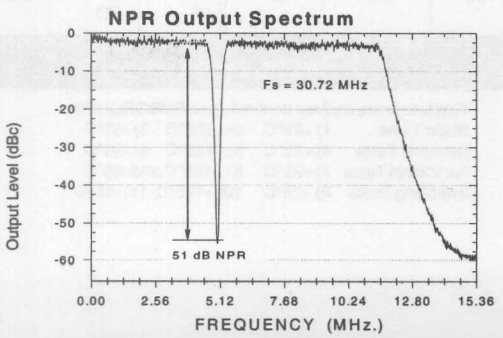
The CLC93X parts have excellent dynamic performance characteristics which are thoroughly tested to insure that system performance goals will be met. Sampling at 15MSPS with a 400kHz input signal, the CLC935 achieves a typical 82dBc SFDR and an SNR of 65.5dB. At the other end of the sample range, the CLC938, with a 140MHz track-and-hold bandwidth, maintains a 60dB SNR with a 50MHz input signal.

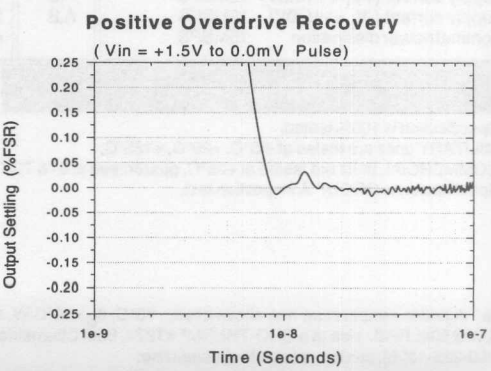
The CLC93X converter family incorporates a complete two-pass architecture which is constructed from high-speed IC's on a thin-film substrate. Critical DC parameters are laser trimmed to assure accurate part-to-part matching. A CONVERT clock, power, and an analog input signal are all that are required for CLC93X operation.

The CLC93X-XC parts are specified over the commercial temperature range, while the CLC93X-X8C parts are extended temperature range, high reliability versions. All of the parts are packaged in 40-pin, 1.1 inch wide, ceramic DIPs with side-brazed leads for easy access and inspection.









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CLC935B Electrical Characteristics ($+V_{CC}$ = +5.0V; $+V_1$ = +15.0V; $-V_2$ = -15.0V; $-V_{EE}$ = -5.2V; unless noted)

PARAMETER	CONDITIONS	NOTES	TYP	WORST CASE RATINGS			UNITS	SYMBOL	LEVEL
Case Temperature			+25	+25	0 to +70	-55 to +125	°C		
DYNAMIC CHARACTERISTICS									
small signal bandwidth	V_{IN} = 1/4 FS		150	100	100	100	MHz	SSBW	4,5,6
large signal bandwidth	V_{IN} = FS		130	80	80	80	MHz	LSBW	4,5,6
slew rate			450	300	300	300	V/µs	SR	4,5,6
overvoltage recovery time	V_{IN} = 2FS		14	25	25	25	ns	OR	4,5,6
effective aperture delay			-0.4	-1.5	-2.0	-2.0	ns	TA	4,5,6
aperture jitter			1.67	2.5	3.0	3.0	ps(RMS)	AJ	4,5,6
NOISE and DISTORTION (15MSPS)									
signal-to-noise ratio (not including harmonics)									
404kHz;	FS		65.6	63	63	61	dB	SNR1	4,5,6
4.984MHz;	FS	A,B	65.4	63	63	61	dB	SNR2	4,5,6
7.225MHz;	FS	A,B	65.2	63	63	61	dB	SNR3	4,5,6
in-band harmonics									
404kHz;	FS-1dB		-82.3	-74	-72	-70	dBc	IBH1	4,5,6
4.984MHz;	FS-1dB	A	-78.1	-70	-68	-64	dBc	IBH2	4,5,6
7.225MHz;	FS-1dB	A	-74.2	-68	-66	-62	dBc	IBH3	4,5,6
intermodulation distortion									
f_1=3.49MHz@FS-7dB; f_2=3.7MHz@FS-7dB			-81.2				dBc	IMD	
noise-power-ratio	FS-12dB								
dc to 5MHz white noise; 2.7MHz notch			51.0				dB	NPR	
DC ACCURACY and PERFORMANCE									
differential non-linearity	dc; FS		0.6	1.0	1.0	1.0	LSB	DNL	4,5,6
integral non-linearity	dc; FS		1.3	3.0	3.0	3.0	LSB	INL	4,5,6
missing codes			0	0	0	0	codes	MC	4,5,6
bipolar offset error			3.0	15	25	40	mV	VIO	4,5,6
temperature coefficient					250	250	µV/°C	DVIO	4,5,6
bipolar gain error			2.0	5.0	5.0	5.0	%FS	GE	4,5,6
temperature coefficient					0.05	0.05	%FS/°C	DGE	4,5,6
ANALOG INPUT PERFORMANCE									
analog input bias current			10	25	35	45	µA	IBN	4,5,6
temperature coefficient			100		250	250	nA/°C	DIBN	4,5,6
analog input resistance			80	25	25	25	kΩ	RIN	4,5,6
analog input capacitance			3.5	5.5	5.5	5.5	pF	CIN	4,5,6
DIGITAL INPUTS									
input voltage	logic LOW			-1.5	-1.5	-1.5	V	VIL	1,2,3
	logic HIGH			-1.1	-1.1	-1.1	V	VIH	1,2,3
input current	logic LOW			1.0	1.0	1.0	mA	IIL	1,2,3
	logic HIGH			1.0	1.0	1.0	mA	IIH	1,2,3
DIGITAL OUTPUTS									
output voltage	logic LOW			-1.5	-1.5	-1.5	V	VOL	1,2,3
	logic HIGH			-1.1	-1.1	-1.1	V	VOH	1,2,3
TIMING									
maximum conversion rate		A	15	15	15	15	MSPS	CR	9,10,11
minimum conversion rate			0	0	0	0	MSPS	CRM	9,10,11
data hold time			6.0	4.0	3.0	3.0	ns	THLD	9,10,11
POWER REQUIREMENTS									
supply current ($+V_{CC}$ = +5.0V)	15MSPS	A,B	146	175	175	175	mA	ICC	1,2,3
supply current ($-V_{EE}$ = -5.2V)	15MSPS	A,B	647	750	750	750	mA	IEE	1,2,3
supply current ($+V_1$ = +15.0V)	15MSPS	A,B	16	20	20	20	mA	I1	1,2,3
supply current ($-V_2$ = -15.0V)	15MSPS	A,B	28	35	35	35	mA	I2	1,2,3
nominal power dissipation	15MSPS		4.75				W	PD	

Test Notes

A) Specification is 100% tested.
MILITARY units are tested at -55°C, +25°C, +125°C;
COMMERCIAL units are tested at +25°C, guaranteed at 0° & 70°C.
B) Specification is GROUP A inspection test.

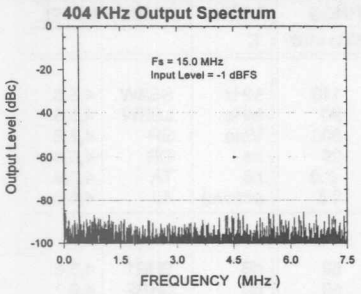
Test Level

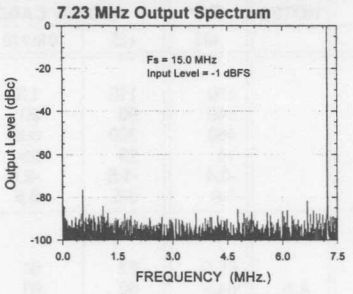
Test levels are derived from mil spec SUBGROUPS.

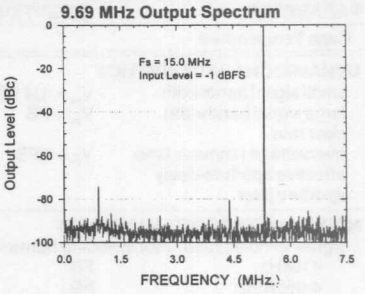
Static Tests	1) +25°C	2) +125°C	3) -55°C
Dynamic Tests	4) +25°C	5) +125°C	6) -55°C
Functional Tests	7) +25°C	8) +125°C and -55°C	
Switching Tests	9) +25°C	10) +125°C	11) -55°C

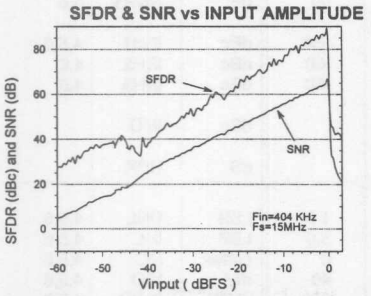
Note: Junction temperature rise above case ≈ 16°C; θ_{CA}=16°C/W; θ_{CA}= 7°C/W@500LFPM. Use of a CHO-THERM® #T274, from Chemetrics (1-800-225-1936), can lower case-to-ambient rise.

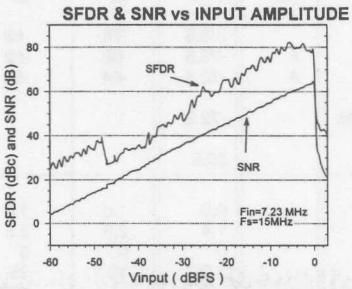
CLC935B Typical Performance Characteristics (Tc = 35°C; 15 MSPS)

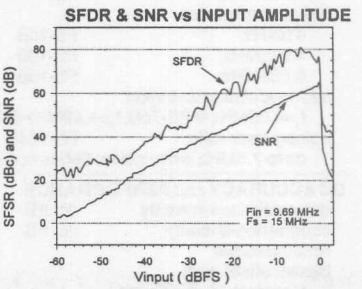


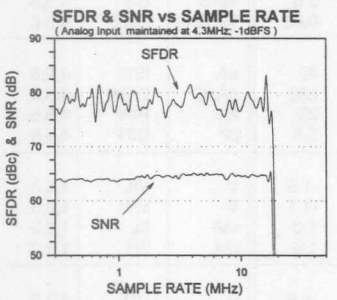


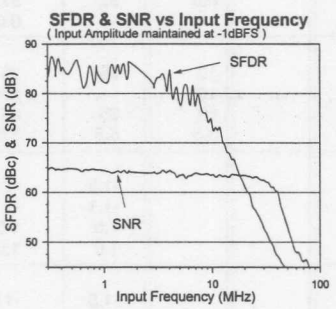


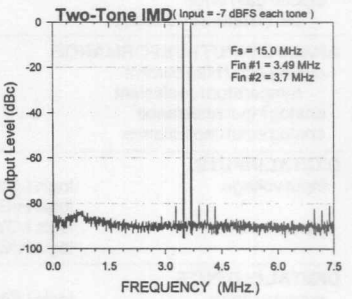


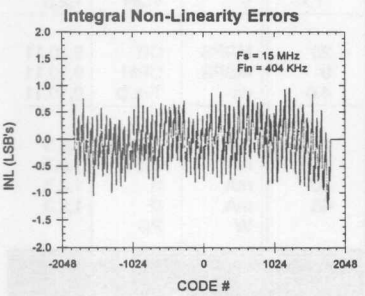


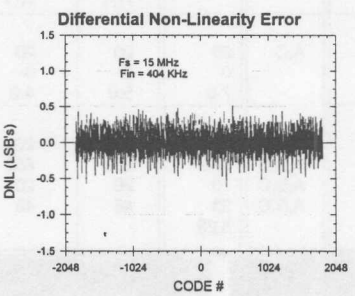


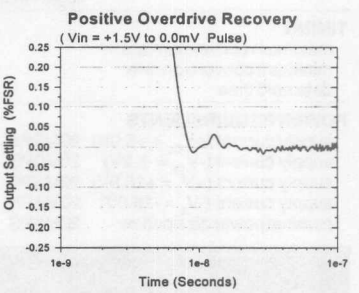


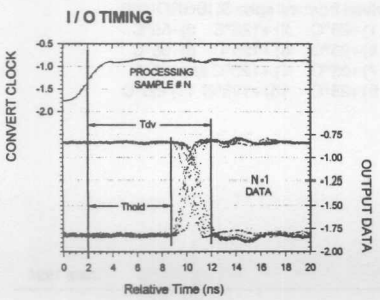


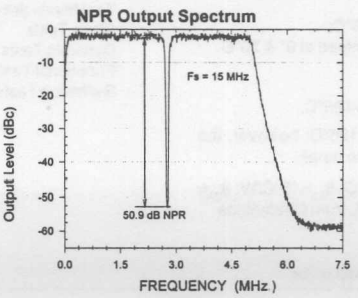


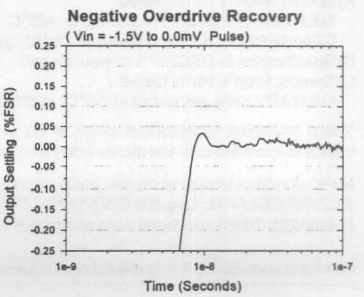












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CLC936C Electrical Characteristics ($+V_{CC}$ = +5.0V; $+V_1$ = +15.0V; $-V_2$ = -15.0V; $-V_{EE}$ = -5.2V; unless noted)

PARAMETER	CONDITIONS	NOTES	TYP	WORST CASE RATINGS			UNITS	SYMBOL	LEVEL
Case Temperature			+25	+25	0 to +70	-55 to +100*	°C		
DYNAMIC CHARACTERISTICS									
small signal bandwidth	V_{IN} = 1/4 FS		160	110	110	110	MHz	SSBW	4,5,6
large signal bandwidth	V_{IN} = FS		140	90	90	90	MHz	LSBW	4,5,6
slew rate			450	300	300	300	V/µs	SR	4,5,6
overvoltage recovery time	V_{IN} = 2FS		14	25	25	25	ns	OR	4,5,6
effective aperture delay			-0.4	-1.5	-2.0	-2.0	ns	TA	4,5,6
aperture jitter			1.8	3.5	3.5	3.5	ps(RMS)	AJ	4,5,6
NOISE and DISTORTION (20MSPS)									
signal-to-noise ratio (not including harmonics)									
410kHz;	FS		65.0	62	61	59	dB	SNR1	4,5,6
4.985MHz;	FS	A,B	64.6	62	61	59	dB	SNR2	4,6
9.663MHz;	FS	A,B	64.3	62	61	59	dB	SNR3	4,6
in-band harmonics									
410kHz;	FS-1dB		-75.6	-70	-68	-64	dBc	IBH1	4,5,6
4.985MHz;	FS-1dB	A	-73.8	-66	-62	-60	dBc	IBH2	4,6
9.663MHz;	FS-1dB	A	-72.4	-64	-60	-60	dBc	IBH3	4,6
intermodulation distortion									
f_1=4.30MHz@FS-7dB; f_2=4.49MHz@FS-7dB			-72.2				dBc	IMD	
noise-power-ratio	FS-12dB								
dc to 7.5MHz white noise; 5MHz notch			50.6				dB	NPR	
DC ACCURACY and PERFORMANCE									
differential non-linearity	dc; FS		0.6	1.0	1.0	1.0	LSB	DNL	4,5,6
integral non-linearity	dc; FS		1.4	2.5	3.5	5.0	LSB	INL	4,5,6
missing codes			0	0	0	0	codes	MC	4,5,6
bipolar offset error			3.0	15	25	40	mV	VIO	4,5,6
temperature coefficient					250	250	µV/°C	DVIO	4,5,6
bipolar gain error			0.6	5.0	5.0	5.0	%FS	GE	4,5,6
temperature coefficient					0.05	0.05	%FS/°C	DGE	4,5,6
ANALOG INPUT PERFORMANCE									
analog input bias current			10	25	35	45	µA	IBN	4,5,6
temperature coefficient			100		250	250	nA/°C	DIBN	4,5,6
analog input resistance			80	25	25	25	kΩ	RIN	4,5,6
analog input capacitance			3.5	5.5	5.5	5.5	pF	CIN	4,5,6
DIGITAL INPUTS									
input voltage	logic LOW			-1.5	-1.5	-1.5	V	VIL	1,2,3
	logic HIGH			-1.1	-1.1	-1.1	V	VIH	1,2,3
input current	logic LOW			1.0	1.0	1.0	mA	IIL	1,2,3
	logic HIGH			1.0	1.0	1.0	mA	IIH	1,2,3
DIGITAL OUTPUTS									
output voltage	logic LOW			-1.5	-1.5	-1.5	V	VOL	1,2,3
	logic HIGH			-1.1	-1.1	-1.1	V	VOH	1,2,3
TIMING									
maximum conversion rate		A,C	20	20	20	20	MSPS	CR	9,10,11
minimum conversion rate			0	0	0	0	MSPS	CRM	9,10,11
data hold time			7.0	5.0	4.0	4.0	ns	THLD	9,10,11
POWER REQUIREMENTS									
supply current ($+V_{CC}$ = +5.0V)	20MSPS	A,B,C	158	200	200	200	mA	ICC	1,2,3
supply current ($-V_{EE}$ = -5.2V)	20MSPS	A,B,C	735	850	850	850	mA	IEE	1,2,3
supply current ($+V_1$ = +15.0V)	20MSPS	A,B,C	10	20	20	20	mA	I1	1,2,3
supply current ($-V_2$ = -15.0V)	20MSPS	A,B,C	35	45	45	45	mA	I2	1,2,3
nominal power dissipation	20MSPS		5.28				W	PD	

Test Notes

A) Specification is 100% tested.
MILITARY units are tested at -55°C, +25°C, +100°C;
COMMERCIAL units are tested at +25°C, guaranteed at 0° & 70°C.
B) Specification is GROUP A inspection test.
C) Specification is 100% tested.
MILITARY units are tested at -55°C, +25°C and +125°C.

*Note: operating temperature range is -55°C to +125°C; however, the device is specified over the above listed temperature range.

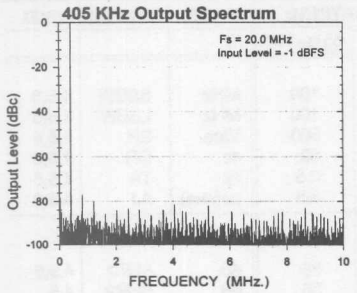
Note: Junction temperature rise above case ≈ 16°C; θ_{CA}=16°C/W; θ_{CA}= 7°C/W@500LFPM. Use of a CHO-THERM® #T274, from Chemetrics (1-800-225-1936), can lower case-to-ambient rise.

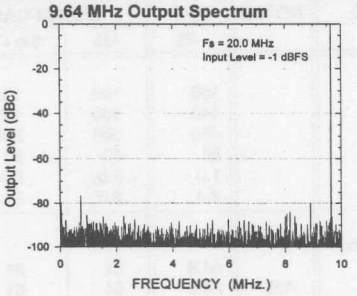
Test Level

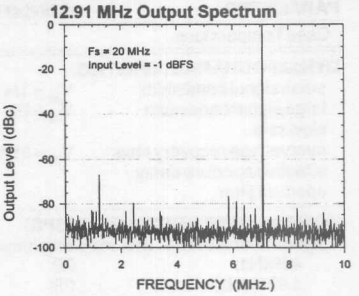
Test levels are derived from mil spec SUBGROUPS.

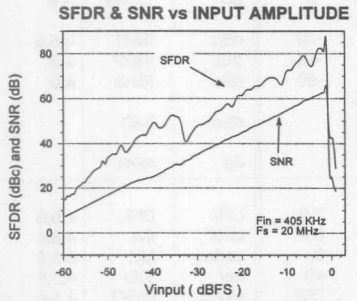
Static Tests	1) +25°C	2) +125°C	3) -55°C
Dynamic Tests	4) +25°C	5) +125°C	6) -55°C
Functional Tests	7) +25°C	8) +125°C and -55°C	
Switching Tests	9) +25°C	10) +125°C	11) -55°C

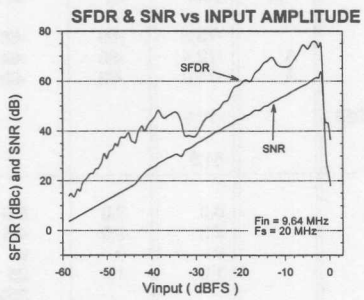
CLC936C Typical Performance Characteristics (Tc = 35°C; 20 MSPS)

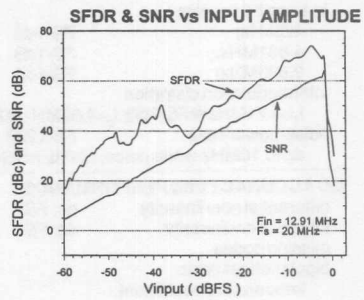


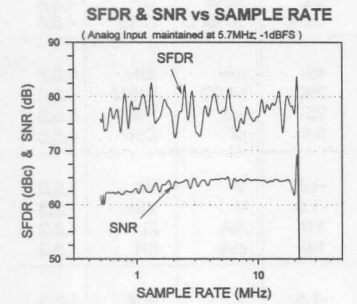


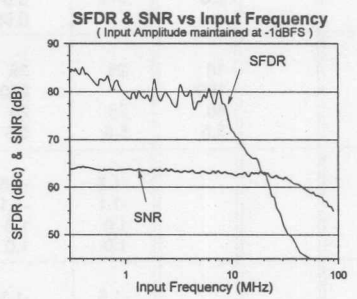


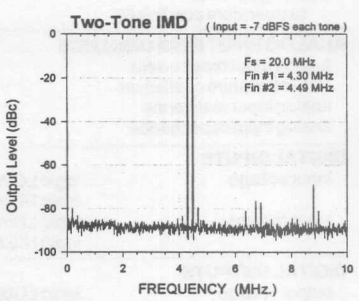


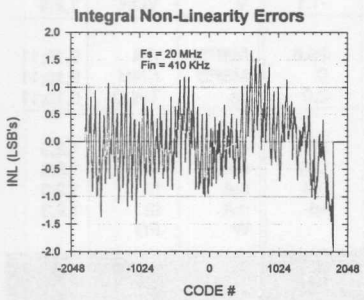


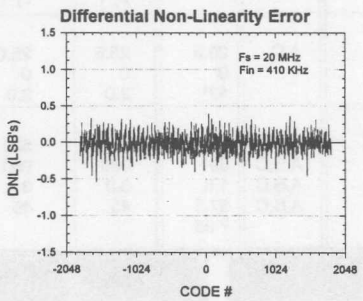


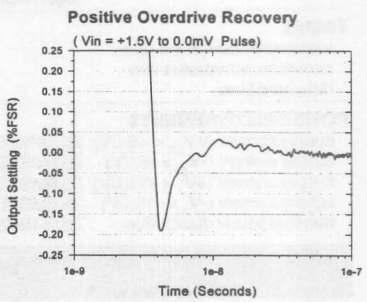


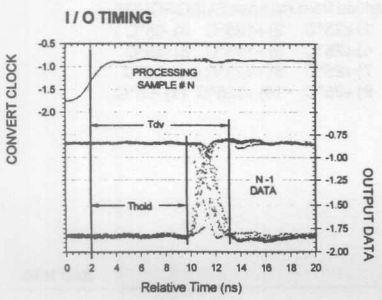


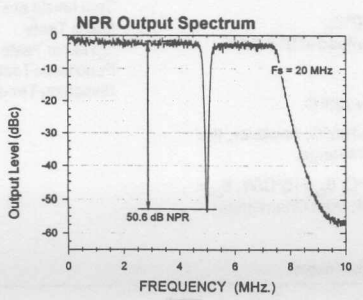


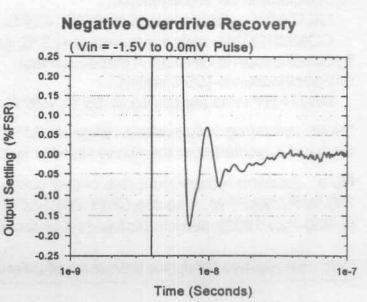












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CLC937B Electrical Characteristics ($+V_{CC}$ = +5.0V; $+V_1$ = +15.0V; $-V_2$ = -15.0V; $-V_{EE}$ = -5.2V; unless noted)

PARAMETER	CONDITIONS	NOTES	TYP	WORST CASE RATINGS			UNITS	SYMBOL	LEVEL
Case Temperature			+25	+25	0 to +70	-55 to +100*	°C		
DYNAMIC CHARACTERISTICS									
small signal bandwidth	V_{IN} = 1/4 FS		160	100	100	100	MHz	SSBW	4,5,6
large signal bandwidth	V_{IN} = FS		140	100	100	100	MHz	LSBW	4,5,6
slew rate			450	300	300	300	V/µs	SR	4,5,6
overvoltage recovery time	V_{IN} = 2FS		56	80	80	80	ns	OR	4,5,6
effective aperture delay			1.0	2.5	2.5	2.5	ns	TA	4,5,6
aperture jitter			2.4	3.5	3.5	3.5	ps(RMS)	AJ	4,5,6
NOISE and DISTORTION (25.6MSPS)									
signal-to-noise ratio (not including harmonics)									
425kHz;	FS		64.8	61	61	59	dB	SNR1	4,5,6
4.831MHz;	FS	A,B	64.2	61	61	58	dB	SNR2	4,6
9.893MHz;	FS	A,B	64.0	61	61	57	dB	SNR3	4,6
in-band harmonics									
425kHz;	FS-1dB		-73.3	-68	-66	-63	dBc	IBH1	4,5,6
4.831MHz;	FS-1dB	A	-72.4	-65	-64	-60	dBc	IBH2	4,6
9.893MHz;	FS-1dB	A	-71.0	-62	-62	-60	dBc	IBH3	4,6
intermodulation distortion									
f_1=4.71MHz@FS-7dB; f_2=4.89MHz@FS-7dB			-71.0				dBc	IMD	
noise-power-ratio	FS-12dB								
dc to 10MHz white noise; 5MHz notch			51.0				dB	NPR	
DC ACCURACY and PERFORMANCE									
differential non-linearity	dc; FS		0.8	2.0	2.0	2.0	LSB	DNL	4,5,6
integral non-linearity	dc; FS		2.0	3.5	4.5	6.0	LSB	INL	4,5,6
missing codes			0	0	0	0	codes	MC	4,5,6
bipolar offset error			1.3	15	25	40	mV	VIO	4,5,6
temperature coefficient					250	250	µV/°C	DVIO	4,5,6
bipolar gain error			2.0	5.0	5.0	5.0	%FS	GE	4,5,6
temperature coefficient					0.05	0.05	%FS/°C	DGE	4,5,6
ANALOG INPUT PERFORMANCE									
analog input bias current			10	25	35	45	µA	IBN	4,5,6
temperature coefficient			100		250	250	nA/°C	DIBN	4,5,6
analog input resistance			80	25	25	25	kΩ	RIN	4,5,6
analog input capacitance			3.5	5.5	5.5	5.5	pF	CIN	4,5,6
DIGITAL INPUTS									
input voltage	logic LOW			-1.5	-1.5	-1.5	V	VIL	1,2,3
	logic HIGH			-1.1	-1.1	-1.1	V	VIH	1,2,3
input current	logic LOW			1.0	1.0	1.0	mA	IIL	1,2,3
	logic HIGH			1.0	1.0	1.0	mA	IIH	1,2,3
DIGITAL OUTPUTS									
output voltage	logic LOW			-1.5	-1.5	-1.5	V	VOL	1,2,3
	logic HIGH			-1.1	-1.1	-1.1	V	VOH	1,2,3
TIMING									
maximum conversion rate		A,C	25.6	25.6	25.6	25.6	MSPS	CR	9,10,11
minimum conversion rate			0	0	0	0	MSPS	CRM	9,10,11
data hold time			4.0	2.0	2.0	2.0	ns	THLD	9,10,11
POWER REQUIREMENTS									
supply current ($+V_{CC}$ = +5.0V)	25.6MSPS	A,B,C	420	500	500	500	mA	ICC	1,2,3
supply current ($-V_{EE}$ = -5.2V)	25.6MSPS	A,B,C	897	980	980	980	mA	IEE	1,2,3
supply current ($+V_1$ = +15.0V)	25.6MSPS	A,B,C	1.5	3.0	3.0	3.0	mA	I1	1,2,3
supply current ($-V_2$ = -15.0V)	25.6MSPS	A,B,C	37.5	45	45	45	mA	I2	1,2,3
nominal power dissipation	25.6MSPS		7.35				W	PD	

Test Notes

A) Specification is 100% tested.
MILITARY units are tested at -55°C, +25°C, +100°C;
COMMERCIAL units are tested at +25°C, guaranteed at 0° & 70°C.
B) Specification is GROUP A inspection test.
C) Specification is 100% tested.
MILITARY units are tested at -55°C, +25°C and +125°C.

*Note: operating temperature range is -55°C to +125°C; however, the device is specified over the above listed temperature range.

Note: Junction temperature rise above case ≈ 16°C; θ_{CA}=16°C/W; θ_{CA}= 7°C/W@500LFPM. Use of a CHO-THERM® #T274, from Chemetrics (1-800-225-1936), can lower case-to-ambient rise.

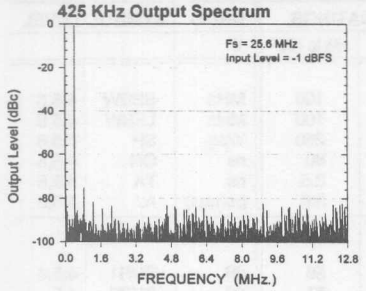
Test Level

Test levels are derived from mil spec SUBGROUPS.

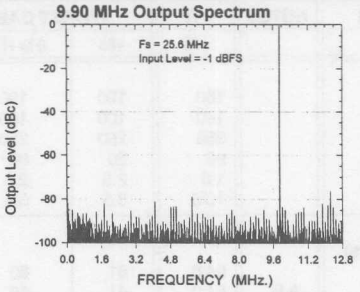
Static Tests	1) +25°C	2) +125°C	3) -55°C
Dynamic Tests	4) +25°C	5) +125°C	6) -55°C
Functional Tests	7) +25°C	8) +125°C and -55°C	
Switching Tests	9) +25°C	10) +125°C	11) -55°C

Typical Performance Characteristics (Tc = 35°C; 25.6 MSPS)

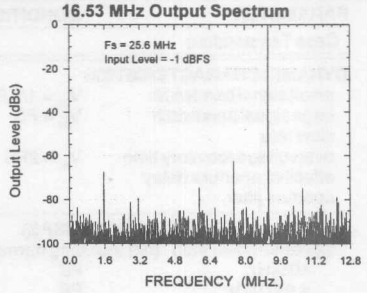
425 KHz Output Spectrum



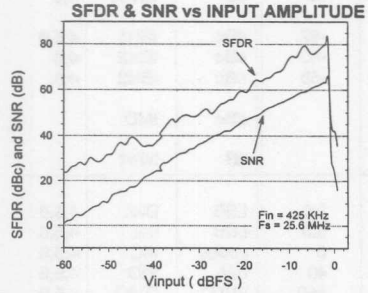
9.90 MHz Output Spectrum



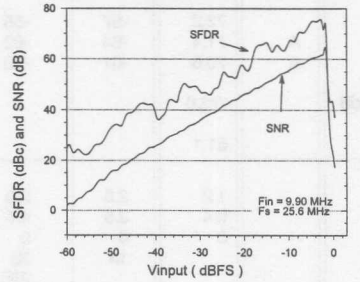
16.53 MHz Output Spectrum



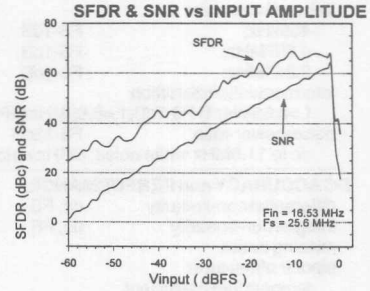
SFDR & SNR vs INPUT AMPLITUDE



SFDR & SNR vs INPUT AMPLITUDE

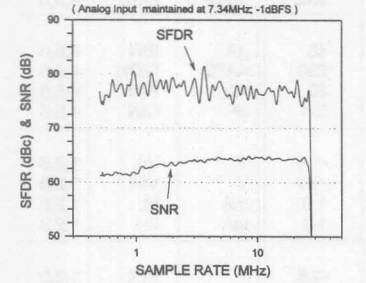


SFDR & SNR vs INPUT AMPLITUDE



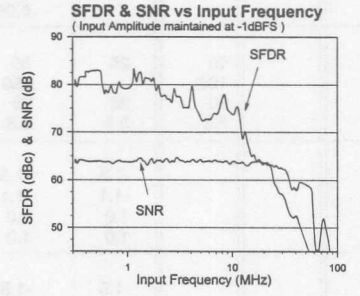
SFDR & SNR vs SAMPLE RATE

(Analog Input maintained at 7.34MHz -1dBFS)



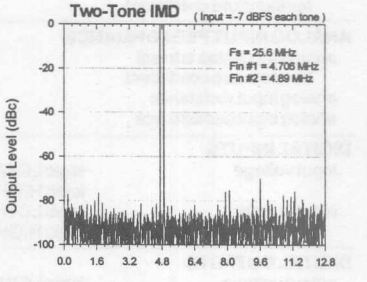
SFDR & SNR vs Input Frequency

(Input Amplitude maintained at -1dBFS)

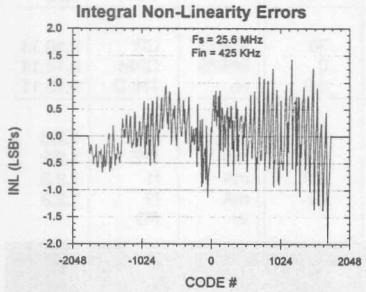


Two-Tone IMD

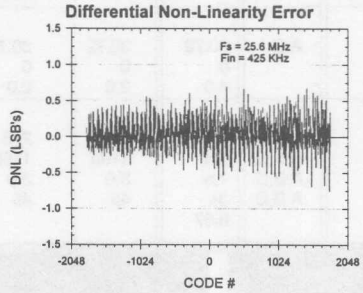
(Input = -7 dBFS each tone)



Integral Non-Linearity Errors

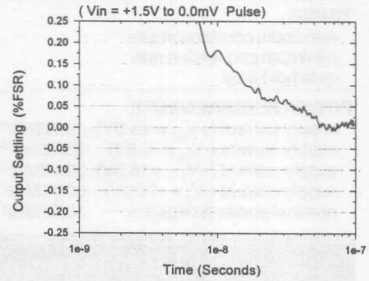


Differential Non-Linearity Error

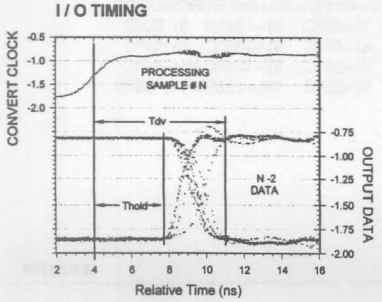


Positive Overdrive Recovery

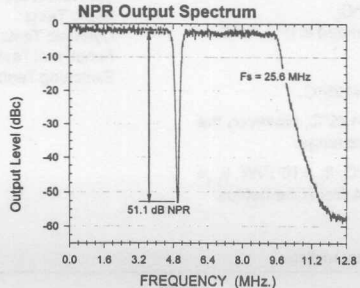
(Vin = +1.5V to 0.0mV Pulse)



I / O TIMING

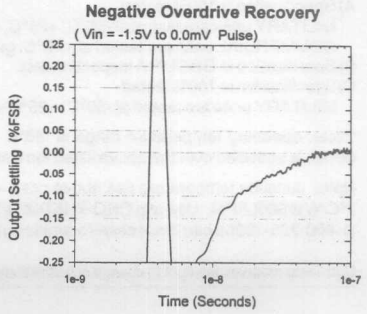


NPR Output Spectrum



Negative Overdrive Recovery

(Vin = -1.5V to 0.0mV Pulse)



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CLC938C Electrical Characteristics ($+V_{CC}$ = +5.0V; $+V_1$ = +15.0V; $-V_2$ = -15.0V; $-V_{EE}$ = -5.2V; unless noted)

PARAMETER	CONDITIONS	NOTES	TYP	WORST CASE RATINGS			UNITS	SYMBOL	LEVEL
Case Temperature			+25	+25	0 to +70	-55 to +85*	°C		
DYNAMIC CHARACTERISTICS									
small signal bandwidth	V_{IN} = 1/4 FS		160	100	100	100	MHz	SSBW	4,5,6
large signal bandwidth	V_{IN} = FS		140	100	100	100	MHz	LSBW	4,5,6
slew rate			350	250	250	250	V/µs	SR	4,5,6
overvoltage recovery time	V_{IN} = 2FS		56	80	80	80	ns	OR	4,5,6
effective aperture delay			1.0	2.5	2.5	2.5	ns	TA	4,5,6
aperture jitter			1.78	3.5	3.5	3.5	ps(RMS)	AJ	4,5,6
NOISE and DISTORTION (30.72MSPS)									
signal-to-noise ratio (not including harmonics)									
405kHz;	FS		64.6	61	60	58	dB	SNR1	4,5,6
4.897MHz;	FS	A,B	64.0	61	60	57	dB	SNR2	4,6
9.367MHz;	FS	A,B	63.7	61	60	56	dB	SNR3	4,6
in-band harmonics									
405kHz;	FS-1dB		72.2	-67	-65	-62	dBc	IBH1	4,5,6
4.897MHz;	FS-1dB	A	71.4	-64	-62	-60	dBc	IBH2	4,6
9.367MHz;	FS-1dB	A	70.6	-61	-60	-59	dBc	IBH3	4,6
intermodulation distortion									
f_1=6.65MHz@FS-7dB; f_2=6.85MHz@FS-7dB			-72.0				dBc	IMD	
noise-power-ratio	FS-12dB								
dc to 11.5MHz white noise; 5MHz notch			51.1				dB	NPR	
DC ACCURACY and PERFORMANCE									
differential non-linearity	dc; FS		1.2	2.0	2.0	2.0	LSB	DNL	4,5,6
integral non-linearity	dc; FS		2.4	3.5	4.5	6.0	LSB	INL	4,5,6
missing codes			0	0	0	0	codes	MC	4,5,6
bipolar offset error				15	25	40	mV	VIO	4,5,6
temperature coefficient					250	250	µV/°C	DVIO	4,5,6
bipolar gain error				5.0	5.0	5.0	%FS	GE	4,5,6
temperature coefficient					0.05	0.05	%FS/°C	DGE	4,5,6
ANALOG INPUT PERFORMANCE									
analog input bias current			10	25	35	45	µA	IBN	4,5,6
temperature coefficient			100		250	250	nA/°C	DIBN	4,5,6
analog input resistance			80	25	25	25	kΩ	RIN	4,5,6
analog input capacitance			3.5	5.5	5.5	5.5	pF	CIN	4,5,6
DIGITAL INPUTS									
input voltage	logic LOW			-1.5	-1.5	-1.5	V	VIL	1,2,3
	logic HIGH			-1.1	-1.1	-1.1	V	VIH	1,2,3
input current	logic LOW			1.0	1.0	1.0	mA	IIL	1,2,3
	logic HIGH			1.0	1.0	1.0	mA	IIH	1,2,3
DIGITAL OUTPUTS									
output voltage	logic LOW			-1.5	-1.5	-1.5	V	VOL	1,2,3
	logic HIGH			-1.1	-1.1	-1.1	V	VOH	1,2,3
TIMING									
maximum conversion rate		A,C	30.72	30.72	30.72	30	MSPS	CR	9,10,11
minimum conversion rate			0	0	0	0	MSPS	CRM	9,10,11
data hold time			4.0	2.0	2.0	2.0	ns	THLD	9,10,11
POWER REQUIREMENTS									
supply current ($+V_{CC}$ = +5.0V)	30.72MSPS	A,B,C	216	275	275	275	mA	ICC	1,2,3
supply current ($-V_{EE}$ = -5.2V)	30.72MSPS	A,B,C	910	1100	1100	1100	mA	IEE	1,2,3
supply current ($+V_1$ = +15.0V)	30.72MSPS	A,B,C	1.5	3.0	3.0	3.0	mA	I1	1,2,3
supply current ($-V_2$ = -15.0V)	30.72MSPS	A,B,C	34	45	45	45	mA	I2	1,2,3
nominal power dissipation	30.72MSPS		6.57				W	PD	

Test Notes

A) Specification is 100% tested.
MILITARY units are tested at -55°C, +25°C, +85°C;
COMMERCIAL units are tested at +25°C, guaranteed at 0° & 70°C.
B) Specification is GROUP A inspection test.
C) Specification is 100% tested.
MILITARY units are tested at -55°C, +25°C and +125°C.

*Note: operating temperature range is -55°C to +125°C; however, the device is specified over the above listed temperature range.

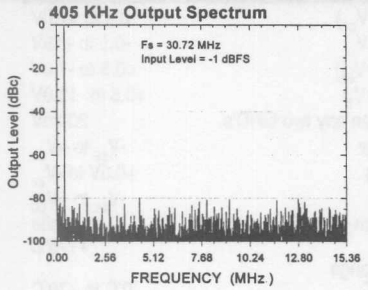
Note: Junction temperature rise above case ≈ 16°C; θ_{CA}=16°C/W; θ_{CA}= 7°C/W@500LFPM. Use of a CHO-THERM® #T274, from Chemetrics (1-800-225-1936), can lower case-to-ambient rise.

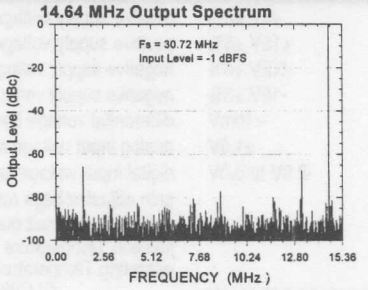
Test Level

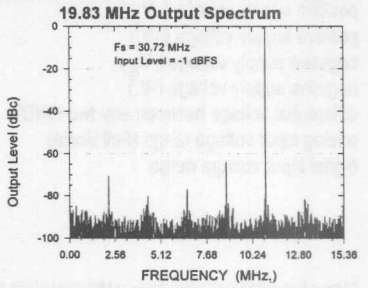
Test levels are derived from mil spec SUBGROUPS.

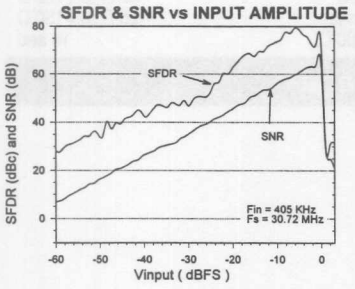
Static Tests	1) +25°C	2) +125°C	3) -55°C
Dynamic Tests	4) +25°C	5) +125°C	6) -55°C
Functional Tests	7) +25°C	8) +125°C and -55°C	
Switching Tests	9) +25°C	10) +125°C	11) -55°C

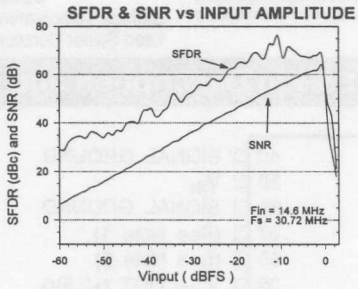
CLC938C Typical Performance Characteristics (Tc = 35°C; 30.72 MSPS)

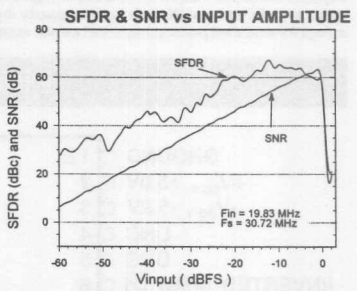


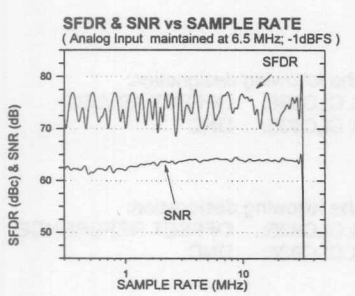


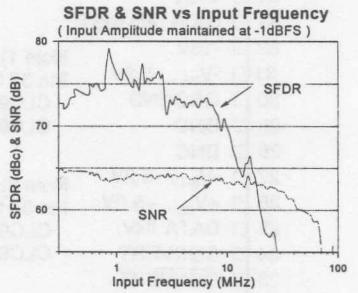


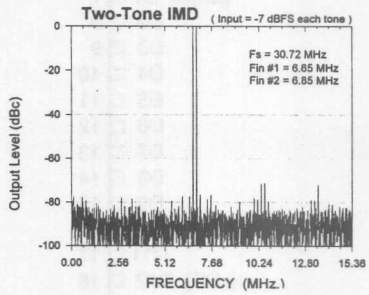


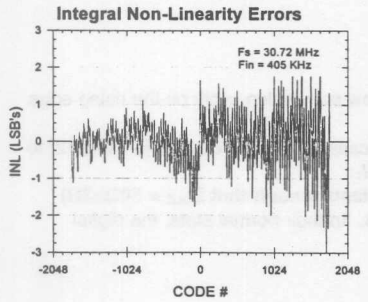


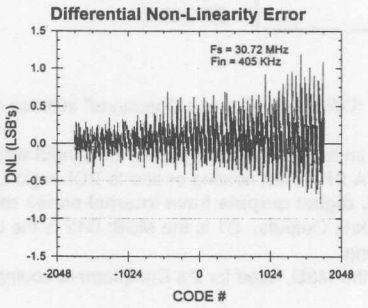


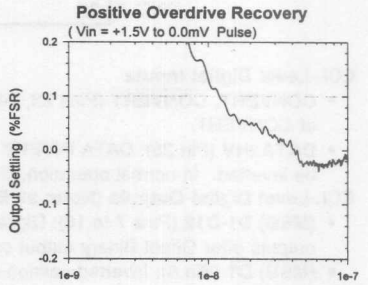


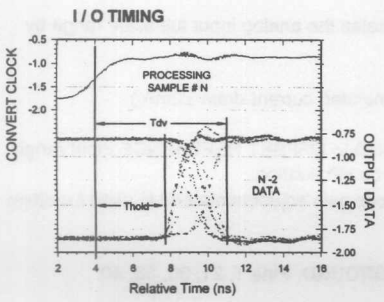


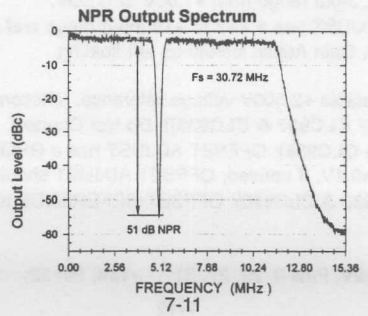


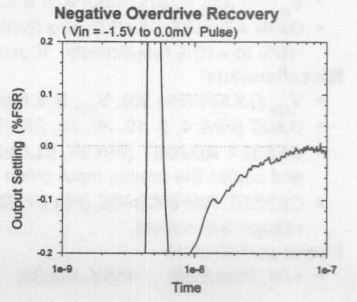












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Recommended Operating Conditions

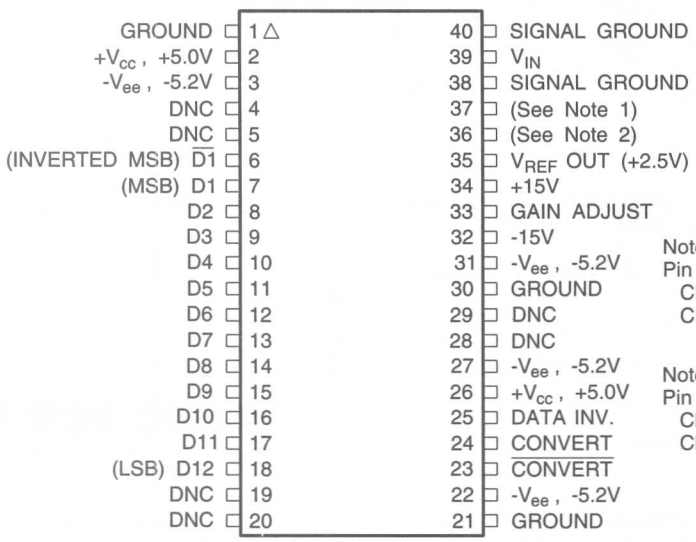
positive supply voltage ($+V_{CC}$)	+5V ±5%
positive supply voltage ($+V_1$)	+15V ±5%
negative supply voltage ($-V_{EE}$)	-5.2V ±5%
negative supply voltage ($-V_1$)	-15V ±5%
differential voltage between any two GND's	<10mV
analog input voltage range (Full Scale)	±1.0V
digital input voltage range	-2.0V to 0.0V

* Note: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

Absolute Maximum Ratings*

positive supply voltage ($+V_{CC}$)	-0.5 to +7.0V
positive supply voltage ($+V_1$)	-0.5 to +18V
negative supply voltage ($-V_{EE}$)	+0.5 to -7.0V
negative supply voltage ($-V_1$)	+0.5 to -18.0V
differential voltage between any two GND's	200mV
analog input voltage range	$-V_{EE}$ to $+V_{CC}$
digital input voltage range	+0.5V to $-V_{EE}$
gain adjust voltage range	$-V_{EE}$ to $+V_{CC}$
output short circuit duration (one pin to ground)	Infinite
junction Temperature	+175°C
operating Temperature Range	
CLC93XXC	0°C to +70°C
CLC93XX8C	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Solder Duration (+300°C)	10 sec

Pinout & Pin Description and Usage



Note 1)
Pin 37 has the following designation:
CLC935 & CLC936: OFFSET ADJUST
CLC937 & CLC938: DNC

Note 2)
Pin 38 has the following designation:
CLC935 & CLC936: OFFSET REFERENCE
CLC937 & CLC938: DNC

ECL-Level Digital Inputs

- **CONVERT, $\overline{\text{CONVERT}}$** (Pins 23, 24) : "Differential Convert Command" initiates a new conversion cycle on the rising edge of CONVERT.
- **DATA INV** (Pin 25): DATA INVERT is an active HIGH (grounded) ECL input which causes the data outputs [D1 to D12] to be inverted. In normal operation, DATA INV is left floating or tied to ECL logic LOW.

ECL-Level Digital Outputs (Note: all ECL digital outputs have internal series resistances such that Z_{out} = 50Ω±3Ω)

- **(MSB) D1-D12** (Pins 7 to 18): Digital Data Outputs. D1 is the MSB; D12 is the LSB. In their normal state, the digital outputs offer Offset Binary output coding.
- **$\overline{\text{(MSB) D1}}$** (Pin 6): Inverted version of the MSB, used for 2's Complement coding.

Analog Input

- **V_{IN}** (Pin 39): Analog input with a 2.0V_{PP} input range from +1.00V to -1.00V.
- **GAIN ADJUST** (Pin 33): The GAIN ADJUST has a +4V to +1V input range and scales the analog input full-scale range by -10% to +10% respectively. If unused, Gain Adjust should be left floating.

Miscellaneous

- **V_{REF} (+2.5V)** (Pin 35): V_{REF} is a highly stable +2.500V voltage reference. (Recommended current drain ≤2mA.)
- **D.N.C** (Pins 4, 5, 19, 20, 28, 29, **[36,37 CLC937 & CLC938]**): Do Not Connect.
- **OFFSET ADJUST (Pin 36, CLC935 & CLC936)**: OFFSET ADJUST has a GROUND to OFFSET REFERENCE input range and scales the analog input offset by ±0.1V. If unused, OFFSET ADJUST should be left floating.
- **OFFSET REFERENCE (Pin 37, CLC935 & CLC936)**: OFFSET REFERENCE tracks gain adjustments and is used for offset voltage adjustment.

Power and Ground

- **+5V**, Pins 2,26; **+15V**, Pin 34; **-5.2V**, Pins 3, 22, 27, 31; **-15V**, Pin 32; **GROUND**, Pins 1, 21, 30, 38, 40.

Discussion of CLC93X Plots and Specifications

Some of the preceeding performance plots require more explanation than is feasible in the caption. This section goes into more detail as to how these plots were generated, and how they might be utilized. Additional information can be found in the application note AD-01 ... Designing with High-Performance A/D converters"

Spectral Plots
Three frequency spectrum plots are shown for each of the CLC93X ADCs. Low and High "Nyquist - band" (<Fs/2) single tone input frequencies were selected along with a "super - Nyquist" (>Fs/2) tone. FFT analysis were performed using 4K point (4096), rectangular windowed data. Valid ADC input frequencies were chosen to land within the center of a prime numbered FFT frequency bin.

SFDR and SNR vs Input level Plots
Fixed frequency input amplitude sweeps were run and the 4K point FFT analysis summary plotted for the three Spectral Plot input frequencies. Signal to Noise Ratio (SNR) is the power ratio between the fundamental and the spectral noise (the first 10 harmonics are excluded from the noise power calculation). As the signal level is reduced from full scale, the noise power remains relatively constant. This results in a backward declining straight line shown as SNR vs Input Amplitude. In some converters the 'noise' is not independent of the input signal level and hence the line's slope may vary.

The Spur-Free Dynamic Range (SFDR) performance is less uniform. SFDR is the magnitude ratio of the fundamental to the next largest spectral line. ADC differential & integral linearity, along with sample to sample step magnitude, create a unique spectral response for each ADC and operating condition. Because sub-ranging ADCs are susceptible to conversion errors at their "coarse-quantization" thresholds (see Principle of Operation), spectral variations become less predictable at these operating points. Special care has been taken in the design of these converters to minimize the characteristic SFDR performance dip in the -20 to -40 dBFS input amplitude ranges.

SNR and SFDR vs Conversion Rate
The CLC93X converters have asyncronous timing schemes which are triggered by the rising edge of the CONVERT clock. The conversion sequence timing is fixed for each ADC; the faster the converter, the shorter the conversion sequence. When the conversion cycle is complete, the T/H amplifier resumes its "track" mode of operation. Because of this timing scheme, ADC performance is relatively independent of sample rate. Increased dynamic performance at slower rates can be achieved by choosing the appropriate converter within the 93X family.

SNR, and SFDR vs Input Frequency
These plots show the variation in converter performance relative to analog input frequency. Input frequencies to about 65MHz (the Large Signal Bandwidth) are included, and can be useful for under-sampled applications. Beyond the Large Signal Bandwidth, performance for large signals degrades quickly. The small-signal-bandwidth (measured with analog inputs below 500mV_{PP}) performance does not degrade until around 135MHz.

Two Tone Linearity Spectrum
In a linear system, the input signal can be viewed mathematically as a superposition of sinusoids (Fourier Transform). The system output can be predicted by the superpositioning of the individual effects on each of the sinusoid inputs. For example, if a linear network is presented with a single tone signal F_1 and the result is an attenuation by a factor A_1, and it is then presented with another frequency F_2 attenuated by A_2 through the system, then the expected output for an input of F_1+F_2 would be $A_1F_1 + A_2F_2$. If the network is not linear, the output will contain frequency components in addition to those present at the input. The most common products likely to be present in the output are at $MF_1 \pm NF_2$, where M and N are integers, and F_1 and F_2 are the two input frequencies.

In the *Two-Tone IMD* plots, two sinusoids are passively filtered and summed to comprise the ADC input. The Vin peak to peak magnitude is set so that the ADC is operating at -1dBFS and the test tone frequencies are shown on the various plots.

Differential & Integral Linearity plots
Differential Non-Linearity (DNL) is computed by collecting a large data series and calculating the difference between its code density and the code density of an ideal sine-wave. The ADC is sampled at its rated maximum conversion rate with a low frequency (approx 400KHz), -1dBFS sine-wave input. The Integral Non-Linearity (INL) is computed by fitting the summed DNL data to a straight line. Deviations of either DNL or INL are usually specified in fractional Quantization levels (LSBs). DNL describes the code to code uniformity.

Digital I/O Timing plot
The digital outputs make their transition and become valid T_{DV}ns after the rising edge of the CONVERT signal. The actual time to this transition varies slightly from output bit to output bit. The amount of this variation is small and well within the timing needs of most systems. In the I/O Timing plot, the transition of the 6 most significant output bits are shown with reference to the CONVERT clock.

Noise Power Ratio (NPR) plots
NPR testing simulates multichannel communication applications. The ADC input is comprised of broadband random noise (Nyquist band limited) with a deep, narrow band of noise notched out. The NPR is simply the depth of the notch in the FFT spectrum. The non-coherent nature of the input signal requires that the data be windowed in order to minimize spectral "leakage" into adjacent FFT filter bins. A four term window function similar to Blackman-Harris was used on 4K point data sets and 10 FFT results were averaged. The input power is varied until a peak NPR figure is found. Distortion products from outside the notched band fall into the FFT notch and degrade NPR. Thus, channel to channel isolation can be determined.

Overdrive Recovery plots
These plots indicate ADC time domain settling from a 50% overdrive condition. A very fast, +1.5V or -1.5V to 0.00V pulse, with a period slightly shorter (100ps) than that of the CONVERT clock, is used as the input source. The ADC is therefore "slipped" through the input waveform and the output data is plotted after being smoothed using a 5 point sliding average. The slip rate (period difference between clock and input) and data point number are used to generate the time axis. For the sake of plot resolution, only fine settling is shown.

Understanding A/D Dynamic Specifications

Analog-to-Digital converters are specified in many ways. As a component achieves higher performance, its specifications and their definitions can become more critical. Fortunately, the vast number of converter applications can generally be placed into one of two classes. These are processed data and non-processed data applications. The distinction seems quite simple but the split implies a completely different approach in specifying A/D converters for a given application.

The processed data area includes the frequency domain applications which employ Fourier processing (FFT). Also in this category are the highly averaged applications, usually concerned with low noise. In each case, the converter's data is averaged or convolved mathematically. This processing reduces the apparent noise level in the output data. For FFTs, the noise is simply spread over a large number of frequency bins. For simple averaging approaches, the Gaussian distribution of noise is greatly reduced, appearing to increase the converter's resolution. Processed applications include radar, network and spectrum analyzers, communications receivers, etc.

The non-processed applications tend to take the converter's data in its original form with very little processing. This means that the noise reduction benefits of the processed applications are not seen. The non-processed area is composed primarily of time domain applications like imaging, DSO's, ultrasound, etc.

The processed vs. non-processed issue has several implications in terms of converter specifications. For the non-processed (time domain) systems the dominant converter specifications deal with noise (SNR) and converter accuracy (DNL). The converter's quantization noise and input stage noise dominate converter accuracy . The harmonic distortion (primarily INL) of the converter is generally of little interest given that most time domain applications present data for visual analysis and tend to focus on "local" accuracy rather than over the full input range. "Local" accuracy is best described through the standard noise measurements, such as SNR and DNL.

In the frequency domain application areas, the noise of the converter is processed to the point where, for almost all systems, it is no longer of issue. This is manifested as a reduction in the apparent noise floor. The actual RMS noise is not reduced, but is spread over more and more frequency bins as processing levels are increased. Unfortunately, the harmonic distortion performance of the converter is not affected by increased processing. This makes the harmonic performance, or more specifically the spurious performance, the dominant error source for frequency domain applications. SFDR becomes the dominant specification for determining converter performance in the frequency domain.

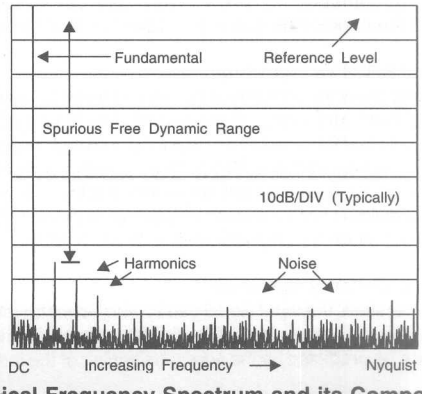
Signal-to-Noise Ratio (SNR) is the ratio of the power contained in the fundamental signal compared to the power contained in the entire noise floor. That is to say all individual noise components are added together to arrive at an integrated noise power. For SNR, harmonic power is excluded from the noise measurement. SNR is particularly important in time domain applications like digital image processing and infrared imaging, where conversion accuracy can be heavily degraded by integrated noise.

Signal-to-Noise-and-Distortion (SINAD) is the ratio of the fundamental signal power to the power at all other frequencies. This includes all noise as well as all harmonics. SINAD is a worst case specification for A/D converters, combining variables from both frequency and time domains. The value of SINAD in high-performance converter applications is not clear since it does not accurately predict the best converter for a given application. Because data converter applications tend to fall into either noise-sensitive time-domain applications or distortion-sensitive frequency-domain applications, SINAD is not specified for the CLC93X data converters.

Total Harmonic Distortion (THD) is the combined power of a specified number of harmonics, compared to the power of the fundamental signal. Harmonics are located at predictable frequencies, spaced at integer multiples of the fundamental signal. For example, a 1MHz fundamental would generate harmonics at 2MHz, 3MHz, 4MHz, ... and so on. In practice, only the first five harmonics contribute significantly to THD, although more may be included in the measurement. THD does not tend to apply well in frequency domain applications which are by their nature very SFDR oriented. In time domain applications, THD is indicative of full-scale input range distortion, however the high-performance time domain applications are generally most interested in local distortion performance. Local distortion and accuracy is dominated by DNL. The use of THD for applications requiring local performance is not likely to yield accurate or repeatable results and therefore THD does not appear in the CLC93X specifications.

Spurious-Free-Dynamic-Range (SFDR) is the "clean" dynamic range of the converter, free from harmonic and spurious signals. SFDR is ratio of the power of the fundamental compared to the power of the next largest component in the frequency spectrum. The SFDR specification is especially important to frequency domain applications which perform Fourier transforms to analyze the converter's output data. Processed applications like radar and network analyzers are typical areas where SFDR offers a direct prediction of converter's performance at both the system and component levels. SFDR is the single best specification for selecting a converter to be used in a frequency domain application.

In-Band Harmonics (IBH) is the ratio of the power of the fundamental compared to the power of the single largest harmonic. This specification is very similar to SFDR, but since it only considers a fairly limited number of harmonics, it is potentially an incomplete gauge of converter performance. SFDR is more stringent and should be used whenever possible in lieu of IBH.



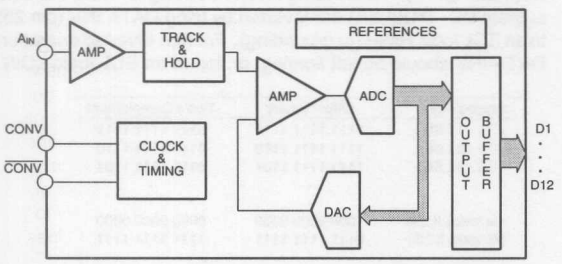
Typical Frequency Spectrum and its Components

Applications Information

In high-speed data acquisition systems, overall performance is often determined by the A/D converter. Accordingly, special attention should be given to the data converter, its operation, and its environment. To assist in this process, information on these critical items has been included in this data sheet. Additional information on using high-performance A/D converters can also be found in Comlinear Corporation application note AD-01.

Principle of Operation

Each of the CLC93X family is a complete two step, subranging A/D converter, with input buffering, internal track-and-hold, quantizer, and all necessary voltage references. The block diagram for the CLC93X data converters is shown below.

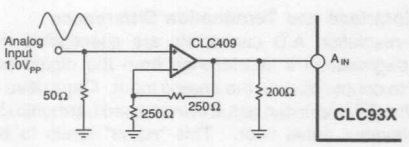


CLC93X Functional Block Diagram

The conversion cycle is initiated on the rising edge of the CONVERT signal. The analog input is sampled by the track-and-hold amplifier and is then digitized with an 8-bit digitizer. The 6 MSBs of this conversion are the "coarse-quantization", which drive a 14-bit accurate DAC to match the input level. The DAC output is then subtracted from the original analog input to generate an error signal, which is then digitized. The two digitized results are combined to form the 12-Bit accurate output. Error correction and ECL output buffering are also provided by each of the CLC93X converters.

Analog Input Driving Circuits

The high dynamic range of the CLC93X family places high demands on any analog processing circuitry that precedes the data converter. This is particularly true in the area of harmonic distortion where the A/Ds' performance often exceeds -80dBc. Fortunately, the each employs an internal buffer for the analog input, and external buffering circuits are usually not required. Both the CLC207 and the CLC409 amplifiers can be configured for better than -80dBc harmonic distortion (note that the CLC207 does support 12-bit settling performance necessary for "time domain" applications). This makes them ideal choices for any analog signal conditioning or buffering that may be required.



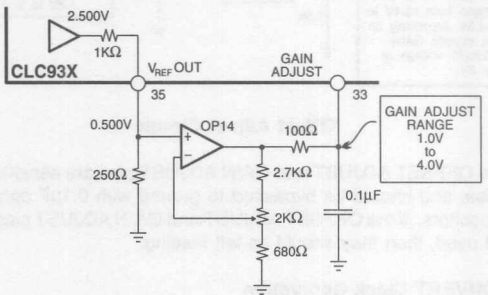
Analog Input Buffering

Gain Adjust

Each of the CLC93X data converter's input range can be adjusted ±10% from its nominal ±1V range. The input range is controlled by adjusting the gain of the internal input buffer. This gain is controlled by the applied voltage at the GAIN ADJUST (pin33). The relationship between applied voltage at pin 33 and the analog input range is:

$$\text{analog input range} = \pm [2V + (0.129)(V_{\text{GAIN ADJUST}} - 2.5V)]$$

GAIN ADJUST pin(33) Voltage	Analog Input Range
1.0V	$1.8V_{PP}$
2.5V or open	$2.0V_{PP}$
4.0V	$2.2V_{PP}$

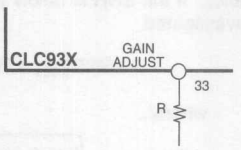


Analog Input Range Adjust Circuit

A resistor from GAIN ADJUST to ground provides a second method of adjusting the analog input range. This technique will decrease the data converter's gain and increase the analog input range.

$$R = \frac{774 - 4{,}800\,\Delta}{\Delta}$$

Where Δ is the gain change factor,i.e 0.01 equals 1% change.



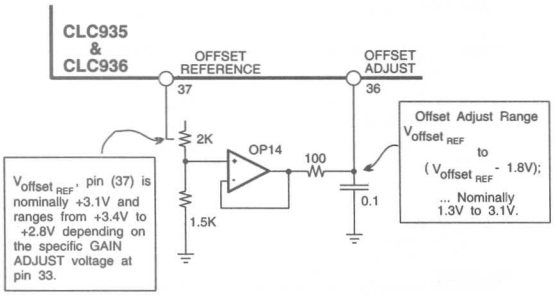
Alternate Input Range Adjust Circuit

Offset Adjust (CLC935 & CLC936)

Typically the center of the ±1V analog input range is laser trimmed to 0V during construction. By applying a voltage at the OFFSET ADJUST (pin 36), the analog input offset can be adjusted approximately ±100mV around ground. The applied voltage at pin 36 can range from GROUND to $V_{\text{OFFSET REFERENCE}}$. If the OFFSET REFERENCE (pin 37) voltage is used to generate the applied OFFSET ADJUST voltage, adjustments in the analog input range *offset* will track any adjustments made to the analog input range *gain*. Analog input range gain and offset adjustments are tightly coupled when the OFFSET REFERENCE is used to generate the OFFSET ADJUST applied voltage. Self-calibration techniques for adjusting offset and gain should use OFFSET REFERENCE in adjusting the offset.

Analog input offset and gain adjustments can be made independent of each other if the V_{REF} OUT (pin 35) is used to generate the applied OFFSET ADJUST voltage instead of the OFFSET REFERENCE voltage. If the V_{REF} OUT approach is adopted, the CLC935/CLC936 offset and gain will be independent of each other, but will likely need an iterative adjustment approach where both offset and gain are successively adjusted until the desired result is obtained.

Offset Adjust Range pin (36)	Analog Input Offset
$V_{OFFSET\ REFERENCE}$	+100mV
open	0mV
GROUND	-100mV



Offset Adjust Circuit

The OFFSET ADJUST and GAIN ADJUST pins are sensitive to noise; and should be bypassed to ground with 0.1µF ceramic capacitors. If the OFFSET ADJUST and GAIN ADJUST pins are not used, then they should be left floating.

CONVERT Clock Generation

All high-speed high-resolution A/D converters are sensitive to the CONVERT clock quality. With a full scale 7MHz analog input signal, the slew rate at the 0V crossing is 90LSB/ns. An error (jitter) of as little as 5ps in the clock edge will yield a 0.5LSB error at the A/D output. This is as great or greater than any other error source likely to be present. This type of clock error or clock jitter is most easily seen in the form of poor SNR (signal-to-noise ratio). If the SNR is below expectations, clock jitter should be investigated.

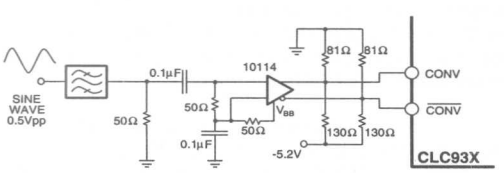
$$SNR_{MAX} = 20\log\left[\frac{1}{2\pi f_{in}\,jitter_{RMS}}\right]$$

where...

$$jitter_{RMS} = \sqrt{(clock\ jitter_{RMS})^2 + (analog\ jitter_{RMS})^2}$$

It should also be noted that jitter in the analog input source will have the same detrimental effect on SNR. Analog input signal jitter is usually only a problem in evaluation setups, and does not generally present a problem in full systems.

Low-jitter crystal controlled oscillators make the best CONVERT clock sources. If the CONVERT clock is generated from another type of source, by gating, dividing or other method, it should be registered by the original clock as the last step. This should keep jitter terms from compounding.



Sine to ECL Conversion Circuit

For variable frequency CONVERT clocks, low-phase-noise frequency synthesizers like the Fluke 6080A or the HP8662 are good choices. Sinusoidal sources of this type will require a sine-to-ECL conversion circuit, such as the one above. This circuit operates consistently with low level inputs (0dBm), but is sensitive to noise (jitter) from the synthesizer. Maintaining a larger input level (>+6dBm), greatly reduces this jitter contribution.

Output Coding

Each of The CLC93X data converters is capable of producing four possible digital output formats: offset binary, two's complement, and their inverted versions. In offset binary the outputs count from 000h to FFFh, as the input varies from -FS (full-scale) to +FS. For two's complement output coding, the MSB in the offset binary format is inverted. On the CLC93X converters, this is achieved by using the $\overline{D1\ (MSB)}$ (pin 6) output rather than the D1(MSB) (pin 7). When using inverted coding formats, the data outputs D2 - D12(LSB) are inverted by tying DATA INV (pin 25) to an ECL logic HIGH (or grounding). For non-inverted operation DATA INV should be left floating, or tied to an ECL logic LOW.

Analog Input	Offset Binary	Two's Complement
+FS - 1 LSB	1111 1111 1111	0111 1111 1111
+FS - 2 LSBs	1111 1111 1110	0111 1111 1110
+FS - 3 LSBs	1111 1111 1101	0111 1111 1101
-	-	-
-	-	-
mid-scale + ½ LSB	1000 0000 0000	0000 0000 0000
mid-scale - ½ LSB	0111 1111 1111	1111 1111 1111
-	-	-
-	-	-
-FS + 2 LSBs	0000 0000 0010	1000 0000 0010
-FS + 1 LSB	0000 0000 0001	1000 0000 0001
-FS	0000 0000 0000	1000 0000 0000

Output Data and "Data Ready"

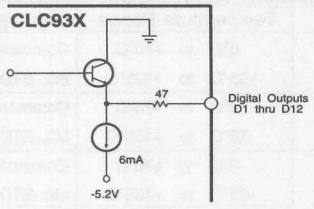
The CLC935 and CLC936 have data latency of one clock cycle whereas the CLC937 and CLC938 have a two clock cycle data latency. This means that a sample taken on the rising edge of CONVERT (t_N) will appear at the output on the t_{N+1} clock cycle of the CLC935 & CLC936 and t_{N+2} clock cycle of the CLC937 & CLC938. The internally latched data from the previous conversion (t_{N-1} CLC935/CLC936; t_{N-2} CLC937/CLC938) is latched to the digital outputs on the rising edge of CONVERT. The previous output data is guaranteed to be valid for at least t_{HLD} after the rising edge of CONVERT and the new output data will be stable t_{DV} after the rising edge of CONVERT (see timing diagram).

Since the output data is synchronous with the rising edge of the CONVERT, its falling edge should be used to generate the output latch clock, or DATA READY signal, if the system so requires. This will limit the bulk of the digital switching noise to a period well away from the sensitive analog processing inside the data converter. The use of the rising edge of CONVERT for Data Ready, and buffer clocking signals, is not recommended. Separate drivers for CONVERT and output latch strobing should be used to minimize corruption and jitter in the CONVERT signal.

Digital Interface and Termination Differences

All high-resolution A/D converters are susceptible to performance degradation if interference from the digital outputs is allowed to couple back to the analog input. Capacitive coupling back to the A/D input can result in increased harmonic distortion, or an elevated noise floor. This "noise" tends to be highly correlated to the input signal, and is difficult to remove through standard DSP noise reduction techniques. To minimize this effect, each of the CLC93X data converters employs ECL "compatible" outputs rather than larger swing TTL compatible outputs. Additional measures to reduce output-to-input coupling have resulted in some slight differences when interfacing to the data converter outputs as compared with true ECL.

Significant system power and digital noise reduction for each of the CLC93X data converters results from the use of on chip ECL pull-down sources for each of the twelve bit lines as illustrated in the figure below. As shown, series termination resistors are included on each data bit in order to drive external 50Ω transmission lines (i.e. PCB traces with Zo = 50Ω).

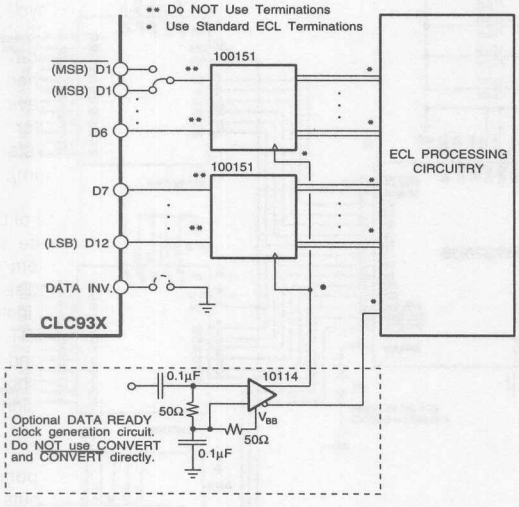


Internal ECL Termination Circuit

The CLC93X data converter outputs are 10KH ECL logic compatible with internal constant-current pull-downs, and are designed to be connected directly to 10KH level inputs with no external termination. The power dissipation in each termination is the 6mA standing current, multiplied by the 5.2V supply, or 31mW per output. For a 12-bit data converter, this represents 375mW. When compared to external (50Ω/-2V) Thevenin terminations, the power savings is 1.2W.

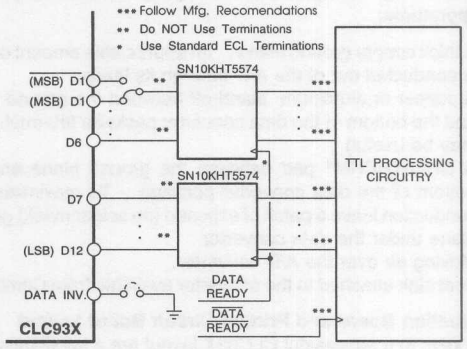
Output Latching and Level Translation

Parasitic capacitances and inductances should be minimized, when interfacing to the CLC93X outputs. Output latches (10176) or buffers should be placed as close as practical to the output pins. If these output latches drive a significant trace load on the same board as the data converter, differential output latches (100151) and trace routing should be used.



Recommended Output Buffering Circuits

In many systems, DSP and other forms of processing will employ TTL or CMOS circuitry. The output logic levels of the CLC93X data converters will need to be translated to match those of the processing circuitry. Several options and translators exist to perform this task. Special care must be used if "10125" type circuits are used since these devices are not particularly suited to a high-resolution, low-noise, analog environment. Other options include TI's 105574 Latched Translator.



ECL to TTL/CMOS Level Translator Options

Power supplies, Grounding, and Bypassing

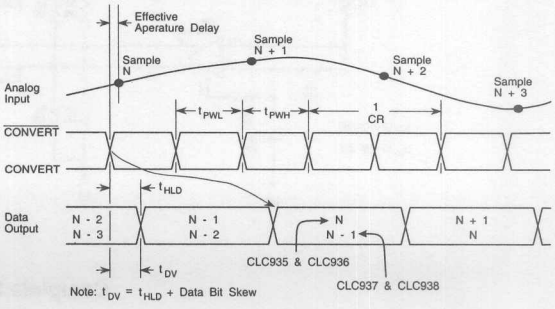
To obtain the best possible performance from any high-speed device, the design engineer must pay close attention to power supplies, grounding and bypassing. This applies not only to the A/D data converter itself but throughout the system as well.

The recommended supply decoupling scheme is as follows: One 0.01µF to 0.033µF chip capacitor at every supply pin, with a +6.8µF to +10µF tantalum for each of the four main supply feeds (within a few inches of the ADC). Note that supply feeds with excessive digital switching noise may require separate filtering using ferrite beads, additional capacitance, or split supplies. Proper bypassing of all other integrated circuits, especially logic circuits, should minimize power supply and ground transients.

All of the CLC93X data converter grounds are internally connected. A single low-impedance ground plane is recommended. Split analog and digital grounds are not recommended. The SIGNAL GND is used internally for the track-and-hold and buffering amplifiers, while the other GROUND pins are essentially power supply returns.

The SIGNAL GND pins (pins 39 & 40) are very sensitive nodes, and should have a solid, low-impedance, ground connection. The path that the input signal and its return currents follow must be isolated from other circuitry. Single-point grounding at the data converter should minimize common impedance paths which would allow other signals to directly couple into the analog input, affecting accuracy.

CLC93X Timing Diagram



Thermal Considerations

The following strategies can be applied to minimize junction temperatures:

a) A thick copper ground plane ... an appreciable amount of heat is conducted out of the A/D through its leads.
b) A copper or aluminum stand-off between the ground plane and the bottom of the data converter package (thermal paste may be useful).
c) A CHO-THERM® pad between the ground plane and the bottom of the data converter package . To maximize heat conduction leave a patch of exposed (no solder mask) ground plane under the data converter.
d) Moving air over the A/D converter.
e) Heat sink attached to the converter available from Comlinear.

Evaluation Board and Printed Circuit Board Layout

The keys to a successful CLC93X layout are a substantial low-impedance ground plane, short connections (in and out of the data converter), and proper power supply decoupling. The use of a socket for the CLC93X data converter is specifically not recommended in the final system design.

The CONVERT clock line traces should be equal length. If they are not equal, the edges may not arrive at the A/D at the same time, which may allow the clock signals to more easily couple into the analog input.

Evaluation boards are available for the CLC93X family (assembled - "E93XPCASM"). The boards can be used to quickly evaluate the performance of the CLC93X data converters. Use of the evaluation board as a model is highly recommended.

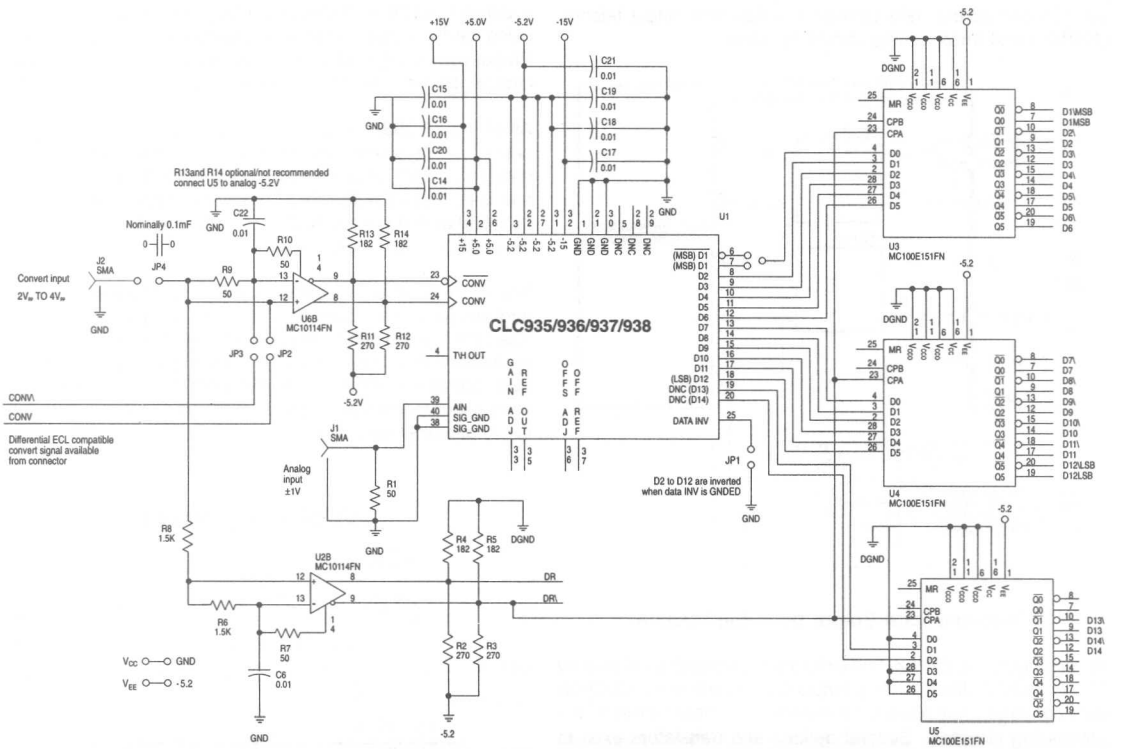
Applications Support

Comlinear Corporation maintains a staff of applications engineers who are available for design and applications assistance. Also, evaluation systems are available, please call (303) 226-0500.

Ordering Information

Model	Temperature Range	Description
CLC935BC	0°C to +70°C	Commercial Version
CLC935B8C	-55°C to +125°C	MIL-STD-883, class B
CLC936CC	0°C to +70°C	Commercial Version
CLC936C8C*	-55°C to +100°C	MIL-STD-883, class B
CLC937BC	0°C to +70°C	Commercial Version
CLC937B8C*	-55°C to +100°C	MIL-STD-883, class B
CLC938CC	0°C to +70°C	Commercial Version
CLC938C8C*	-55°C to +85°C	MIL-STD-883, class B

*Note: operating temperature range is -55°C to +125°C; however, the devices are specified over the above listed temperature ranges.



Complete System Circuit

Comlinear
A National Semiconductor Company

Low-Power, 12-Bit 1.0/1.5 MSPS A/D Converters

Advance Data CLC945/CLC946

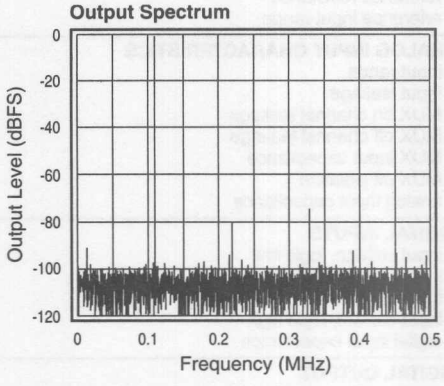
APPLICATIONS:
- Digital cameras
- Optical scanners
- DSP front ends
- Mobile telecommunications
- Data acquisition
- Instrumentation
- Medical imaging

FEATURES:
- Low-power
- SNR of 72dB
- THD of -82dB
- Single +5V power supply
- Internal sample & hold
- Internal 2:1 analog multiplexer
- Low power standby mode

DESCRIPTION

Featuring an internal 2:1 multiplexer, internal sample and hold amplifier and a complete A/D converter, the CLC945 and CLC946 make data acquisition system design easy. The CLC945 is capable of a maximum conversion rate of 1Mega Sample-per-Second (MSPS) whereas the CLC946 is able to convert signals at rates up to 1.5MSPS. The low power of these parts (75mW for the CLC945 and 200mW for the CLC946) is a feature that will help to extend the battery life in battery powered applications. In addition there is a mode in which the devices may be powered down to dissipate only 250µW with a simple digital power down signal. Further enhancing the suitability of these devices for battery powered applications is the fact that they require only one power supply.

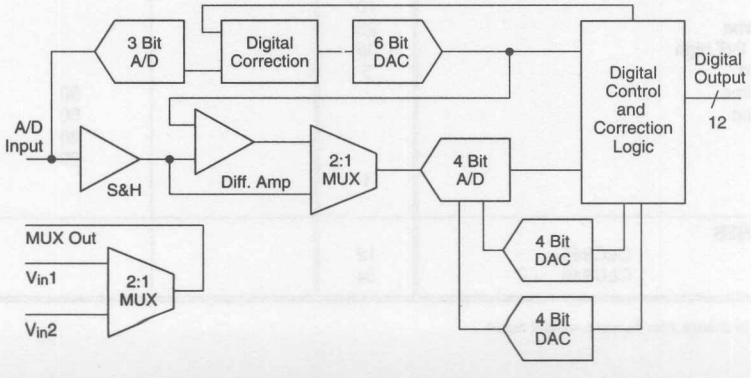
The CLC945 and CLC946 are fabricated in a fine line CMOS technology. The CLC945AJQ, CLC945BJQ and CLC946AJQ are specified over the industrial temperature range of -40°C to +85°C and are packaged in the 44-pin PLCC plastic chip carrier.



Applications Support

Comlinear maintains a staff of applications engineers who are available for design and applications assistance. To make use of this service call **(800) 776-0500 or (970) 225-7422**.

BLOCK DIAGRAM



CLC945/CLC946 Electrical Characteristics (V_{CC} = + 5V, V_{REF+} = 4.096V, F_{IN} = 100KHz, F_S = 1MSPS, V_{REF-} = 0V)

PARAMETERS	CONDITIONS	TYP	GUARANTEED MIN/MAX		UNITS	NOTES
Ambient Temperature	CLC945/CLC946	+25°C	+25°C	-40 to 85°C		
DYNAMIC CHARACTERISTICS						
overvoltage recovery time					ns	
effective aperture delay		20			ns	
DISTORTION AND NOISE RESPONSE						
SINAD	CLC945/CLC946	71/70			dB	
intermodulation distortion		80			dB	
total harmonic distortion	CLC945/CLC946	82/80			dB	
DC ACCURACY AND PERFORMANCE						
differential non-linearity		0.4			LSB	
integral non-linearity	CLC945	0.4			LSB	
	CLC946	0.4			LSB	
missing codes		0			Codes	
gain error	CLC945	0.2			LSB	
	CLC946	0.3			LSB	
power supply sensitivity	CLC945/CLC946			0.75/1.0	LSB	
VOLTAGE REFERENCE CHARACTERISTICS						
reference resistance		750			Ω	
reference input range		0-V_{CC}				
ANALOG INPUT CHARACTERISTICS						
input range		GND-V_{CC}				
input leakage		0.1			µA	
MUX on channel leakage		0.1			µA	
MUX off channel leakage		0.1			µA	
MUX input capacitance		7			pF	
MUX off isolation		92			dB	
analog input capacitance		25			pF	
DIGITAL INPUTS						
input voltage, logic low				0.8	V	
input voltage, logic high				2.0	V	
input current, logic low		0.1		1.0	µA	
input current, logic high		0.1			µA	
digital input capacitance		4			pF	
DIGITAL OUTPUT						
output voltage, logic low				0.4	V	
output voltage, logic high	I_{out} = -100µA			4.25	V	
output voltage, logic low	I_{out} = - 360µA			2.4	µA	
TRI-STATE® output leakage current		0.1			µA	
TRI-STATE® output capacitance		5			pF	
TIMING						
maximum conversion rate	CLC945/CLC946	1.0/1.5			MSPS	
conversion time	CLC945/CLC946	740/580			ns	
S/H pulse width maximum	CLC945/CLC946	550/400			ns	
S/H pulse width minimum		5			ns	
S/H to EOC low	CLC945/CLC946	95/90			ns	
access time		10			ns	
TRI-STATE® control time		25			ns	
delay from RD low to INT high		35			ns	
EOC high to data valid		5			ns	
MUX address setup time				50	ns	
MUX address hold time				50	ns	
CS setup time				20	ns	
CS hold time				20	ns	
wakeup time		1			µs	
data hold time						
POWER REQUIREMENTS						
supply current	CLC945	12			mA	
	CLC946	34			mA	

Comlinear reserves the right to change specifications without notice.

Comlinear
A National Semiconductor Company

Very Low Power, 12-Bit, 20MSPS Monolithic A/D Converter

CLC949

APPLICATIONS:
- CCD imaging
- IR imaging
- FLIR processing
- Medical imaging
- High definition video
- Instrumentation
- Radar processing
- Digital communications

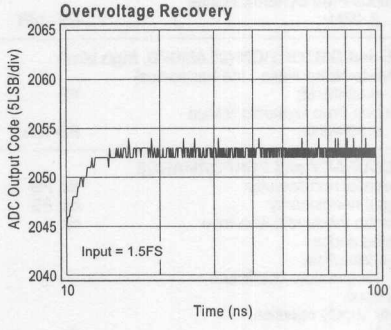
FEATURES:
- Very low/programmable power
  - 0.07W @ 5MSPS
  - 0.22W @ 20MSPS
  - 0.40W @ 30MSPS
- Single supply operation (+5V)
- 0.5 LSB differential linearity error
- Wide dynamic range
  - 72dBc spurious-free dynamic range
  - 68dB signal-to-noise ratio
- No missing codes

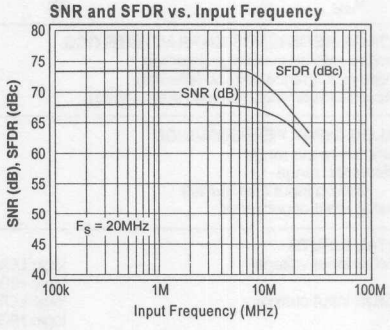
DESCRIPTION

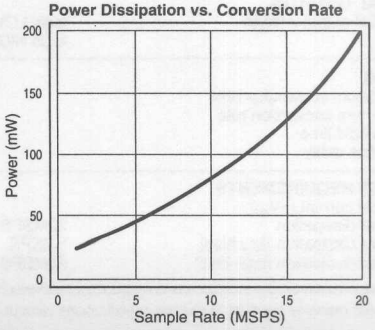
The CLC949 is a 12-bit analog-to-digital converter subsystem including 12-bit quantizer, sample-and-hold amplifier, and internal reference. The CLC949 has been optimized for low power operation with high dynamic range and is packaged in a 44-pin PLCC. The CLC949 has a unique feature which allows the user to adjust internal bias levels in the converter which results in a trade-off between power dissipation and maximum conversion rate. With bias set for 220mW power dissipation the converter operates at 20MSPS. Under these conditions, dynamic performance with a 9.9MHz analog input is typically 68dB SNR and 72dBc SFDR. When bias is set for only 65mW power dissipation the converter maintains excellent performance at 5MSPS. With a 2.4MHz analog input signal the SNR is 70dB and SFDR is 78dBc. This excellent dynamic performance in the frequency domain without high power requirements make the part a strong performer for communications and radar applications. The low input noise of the CLC949, its 0.5LSB differential linearity error specification, fast settling, and low power dissipation also lead to excellent performance in imaging systems. All parts are thoroughly tested to insure that guaranteed specifications are met.

The CLC949 incorporates an input sample-and-hold amplifier followed by a quantizer which uses a pipelined architecture to minimize comparator count and the associated power dissipation penalty. An on-board voltage reference is provided. Analog input signals, conversion clock, and a single supply are all that are required for CLC949 operation.

The CLC949 is fabricated in a 0.9µm CMOS technology. The **CLC949ACQ** is specified over the commercial temperature range of 0°C to +70°C and is packaged in a 44-pin PLCC.







Power Requirements

	Typ	Units
V_{cc} = +5V, 5MSPS, Low Bias	65	mW
V_{cc} = +5V, 20MSPS, Med Bias	220	mW
V_{cc} = +5V, 30MSPS, High Bias	400	mW

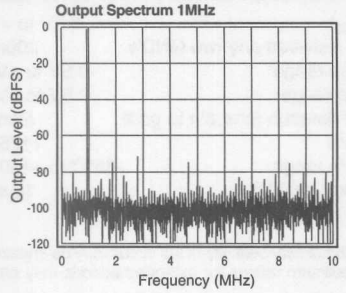
CLC949 Electrical Characteristics ($+V_{DD}$ = +5V, Medium Bias (200µA): unless specified)

PARAMETERS	CONDITIONS	TYP	WORST CASE RATINGS		UNITS	SYMBOL
Case Temperature			+25°C	0 to 70°C		
DYNAMIC CHARACTERISTICS						
overvoltage recovery V_{IN} = 1.5FS		15	25	25	ns	OR
effective aperture delay		3.0	6.2	6.2	ns	TA
aperture jitter		7.0	15	15	ps(rms)	AJ
slew rate		400			V/µS	SR
settling time		12			ns	ST
NOISE and DISTORTION (20MSPS)						
Signal-to-Noise Ratio (no harmonics)						
4.985MHz;	FS	68	66	66	dB	SNR2
9.663MHz;	FS	68	66	66	dB	SNR3
Spurious-Free Dynamic Range						
4.985MHz;	FS -1dB	72			dBc	SFDR2
9.663MHz;	FS -1dB	72	63	58	dBc	SFDR3
Intermodulation Distortion						
f_1 = 5.58MHz @ FS -7dB; f_2 = 5.70MHz @ FS -7dB		-70			dBc	IMD
3dB bandwidth (full power)		100			MHz	BW
NOISE and DISTORTION (5MSPS, low bias)						
Signal-to-Noise Ratio (no harmonics)						
2.4MHz;	FS	70	68	68	dB	SNR1
Spurious-Free Dynamic Range						
2.4MHz;	FS -1dB	78	66	66	dBc	SFDR1
NOISE and DISTORTION (25.6MSPS, high bias)						
Signal-to-Noise Ratio (no harmonics)						
9.894MHz;	FS	67	63	63	dB	SNR4
Spurious-Free Dynamic Range						
9.894MHz;	FS-1dB	67	59	53	dBc	SFDR4
DC ACCURACY and PERFORMANCE						
differential non-linearity	dc; FS	0.5	1.0	1.0	LSB	DNL
integral non-linearity	dc; FS	1.2	3.5	3.5	LSB	INL
common mode rejection ratio	dc	60			dB	CMRR
missing codes		0	0	0	codes	MC
mid-scale offset		5.0	25	25	mV	VIO
temperature coefficient		15			µV/°C	DVIO
gain error		1.0	5.0	5.0	%FS	GE
power supply rejection						
V_{dda}	dc	55			dB	PSRA
V_{ddd}	dc	50			dB	PSRD
VOLTAGE REFERENCE CHARACTERISTICS						
positive reference voltage (internal)		3.25	3.24-3.26	3.24-3.26	V	VREFP
negative reference voltage (internal)		1.25	1.24-1.26	1.24-1.26	V	VREFN
differential reference voltage (Vrefp - Vrefn)		2.0	1.98-2.02	1.98-2.02	V	VDIFF
ANALOG INPUT PERFORMANCE						
common mode range		2 - 3			V	VCM
differential range		± 2			V	VDM
analog input bias current		± 0.1	± 1.0	± 1.0	µA	IBN
analog input capacitance		5.0	10	10	pF	CIN
DIGITAL INPUTS						
CMOS input voltage	logic LOW		1	1	V	VIL
	logic HIGH		4.0	4.0	V	VIH
CMOS input current	logic LOW	±0.1	±1.0	±1.0	µA	IIL
	logic HIGH	±0.1	±1.0	±1.0	µA	IIH
DIGITAL OUTPUTS						
CMOS output voltage	logic LOW	0.25	0.5	0.5	V	VOL
	logic HIGH	4.8	4.5	4.5	V	VOH
TIMING						
maximum conversion rate		30	30	30	MSPS	CR
minimum conversion rate		10	10	10	KSPS	CRM
data hold time		7.0	4.5	4.5	ns	THLD
pipeline delay		6.5	6.5	6.5	clocks	
POWER REQUIREMENTS						
supply current ($+V_{dd}$)		44	60	60	mA	IDD
power dissipation	20MSPS	220	300	300	mW	PDM
power dissipation (low bias)	5MSPS	65			mW	PDL
power dissipation (high bias)	30MSPS	400			mW	PDH

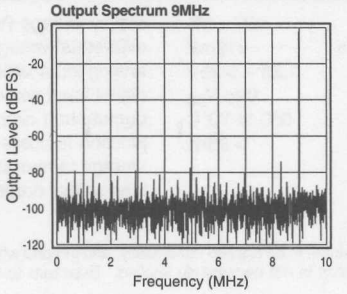
Comlinear reserves the right to change specifications without notice.

CLC949 Typical Performance Characteristics ($+V_{DD}$ = + 5V, Med Bias, F_S = 20MSPS: unless specified)

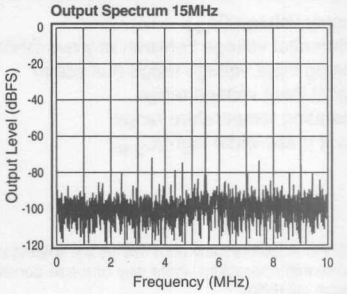
Output Spectrum 1MHz



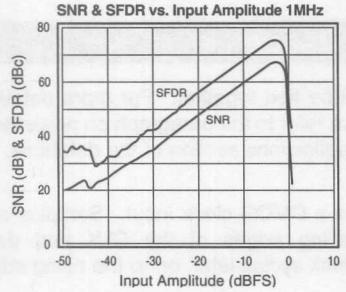
Output Spectrum 9MHz



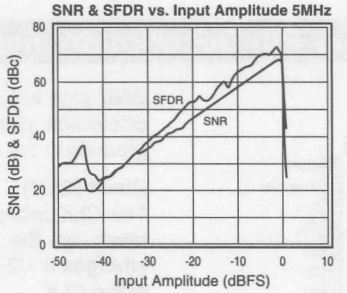
Output Spectrum 15MHz



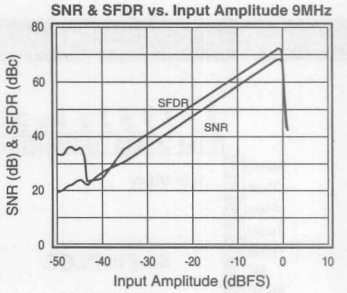
SNR & SFDR vs. Input Amplitude 1MHz



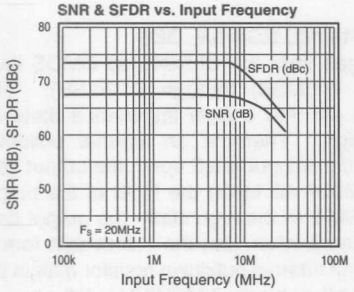
SNR & SFDR vs. Input Amplitude 5MHz



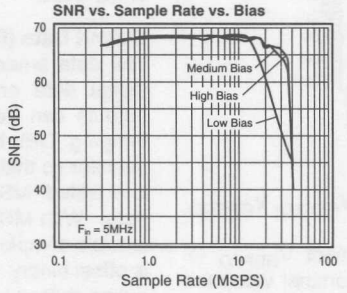
SNR & SFDR vs. Input Amplitude 9MHz



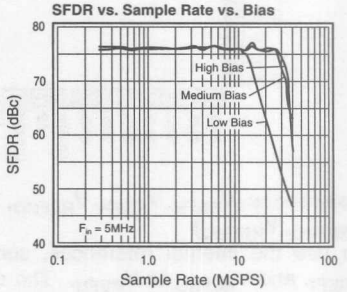
SNR & SFDR vs. Input Frequency



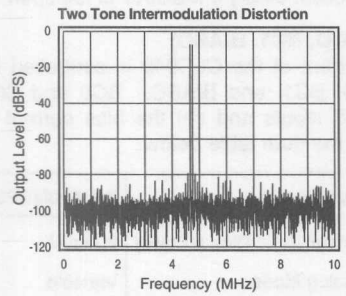
SNR vs. Sample Rate vs. Bias



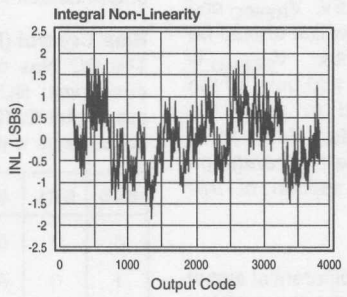
SFDR vs. Sample Rate vs. Bias



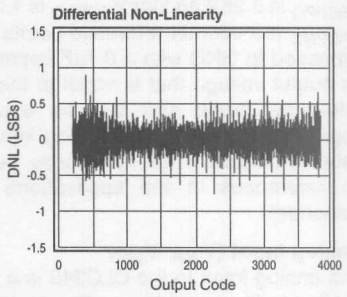
Two Tone Intermodulation Distortion



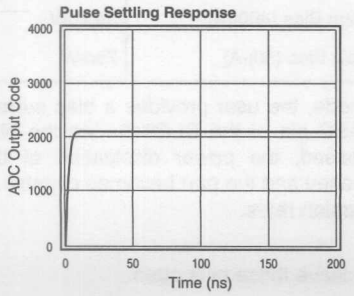
Integral Non-Linearity



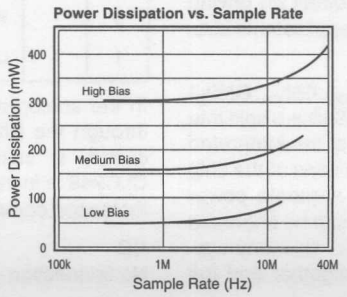
Differential Non-Linearity



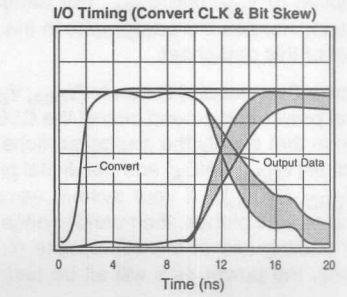
Pulse Settling Response



Power Dissipation vs. Sample Rate



I/O Timing (Convert CLK & Bit Skew)



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Recommended Operating Conditions

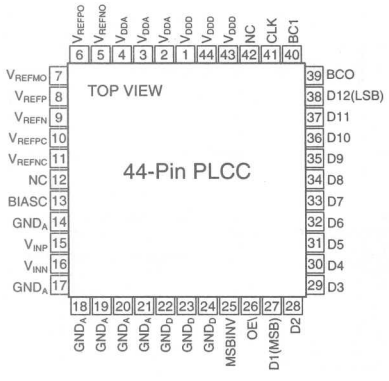
supply voltage (V_{DD})	+5V ±5%
differential voltage between any two GND's	<10mV
analog input voltage range (full scale)	1.25 – 3.25V
digital input voltage range	0 to V_{DD}
operating temperature range	0°C to 70°C
clock pulse-width high (C_{pwh})	> 25ns

Absolute Maximum Ratings*

supply voltage (V_{DD})	-0.5V to +7V
differential voltage between any two GND's	200mV
analog input voltage range	-0.5V to +V_{DD}
digital input voltage range	-0.5V to +V_{DD}
output short circuit duration (one pin to gnd)	infinite
junction temperature	+175°C
storage temperature range	-65°C to +150°C
lead solder duration (+300°C)	10 sec

***NOTE:** Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

Pinout & Pin Description and Usage



References (V_{REFN}, V_{REFP}, V_{REFNO}, V_{REFPO}, V_{REFNC}, V_{REFPC}, V_{REFMO})

To use the internal references, connect V_{REFPO} to V_{REFP} and V_{REFNO} to V_{REFN}. The nominal value for V_{REFPO} is 3.25V and for V_{REFNO} is 1.25V. V_{REFPC} and V_{REFNC} are internal reference points which should be bypassed to GND with a 0.1µF capacitor. V_{REFMO} is an output voltage that is equal to the mid point of the reference range and can be used to apply the appropriate offset to the analog inputs. For a more detailed discussion on references, see the paragraph on references in the applications section of this datasheet.

Analog Input (V_{INP}, V_{INN})

The analog input to the CLC949 is a differential signal applied to V_{INP} and V_{INN}. For more detail on driving the inputs, see the paragraphs in the applications section of this datasheet.

Power Supplies and Grounds (V_{DDA}, V_{DDD}, GND_A, GND_D)

The power and ground pins of the CLC949 are split into those that supply the analog portions of the integrated circuit (V_{DDA}, GND_A) and the digital portions of the chip (V_{DDD}, GND_D). If your system uses separate power and ground planes, then performance can be improved by making use of the appropriate pins. In many systems, the power pins will all be tied together and the GND pins will all be tied together. For more detailed discussion, please refer to the paragraph on power and grounds in the applications section of the databook.

Clock (CLK)

The CLK accepts a CMOS clock input. Samples are taken on the falling edges of the CLK and data emerges 6 1/2 clock cycles later, on to the rising edge of the CLK.

Output Data (D1-D12, MSBINV, OE\)

The data emerges from the CLC949 as CMOS level digital data on D1(MSB) through D12(LSB). The outputs can be put into a high impedance state by bringing OE\ high. There is an internal pulldown resistor so that if this input is left open, the output data is enabled. MSBINV will invert the MSB of the output data. With MSBINV in the high state, the output data is two's complement, when low, the output data format is offset binary. An internal pulldown resistor makes the output default to offset binary if MSBINV is left open.

Bias Control (BCO, BC1, BIASC)

The DC bias current of the CLC949 is controlled by three pins: BCO, BC1, and BIASC. BC0 and BC1 are digital CMOS inputs and set the bias current in accordance with the truth table below:

BC0	BC1	Bias Current	PD@10MSPS
0	0	Default: Med Bias (200µA)	200mW
1	0	Analog Mode	Variable
0	1	High Bias (400µA)	350mW
1	1	Low Bias (50µA)	75mW

In the analog mode, the user provides a bias current through the BIASC pin of the CLC949. As the bias current is increased, the power dissipation of the CLC949 is increased and the part becomes capable of increased conversion rates.

NC

No connection - leave these pins open.

CLC949 OPERATION

Application

In a high speed data acquisition system, the overall performance is often determined by the A/D converter and its surrounding circuitry. You should pay special attention to the data converter and its support circuitry if you want to obtain the best possible performance. The information on these pages is intended to help you design the circuitry surrounding the CLC949 in such a way as to achieve superior results. Additional information is available in the form of Comlinear applications notes. Especially useful are AD-01 and AD-02.

Circuit Description

The CLC949 ADC consists of an input Sample-and-Hold Amplifier (SHA) followed by a pipelined quantizer. Internal reference sources and output data latches complete the major functions required of an A/D converter. Digital error correction in the quantizer helps to provide accurate conversions of high speed dynamic signals. The speed of the analog circuitry is determined in part by the internal bias currents applied. The CLC949 allows you to make this important tradeoff between power and performance through settings on two digital control pins and for fine adjustments through the use of an external resistor.

Timing and CLK Generation

The falling edge of the CLK pulse causes the input sample-and-hold amplifier to transition into the hold mode. The sample is taken approximately 3ns after this falling edge. The digitized data is presented to the output latches 6 1/2 clock cycles later and is held until after the next rising edge of CLK. This timing is shown in the timing diagram, Figure 1.

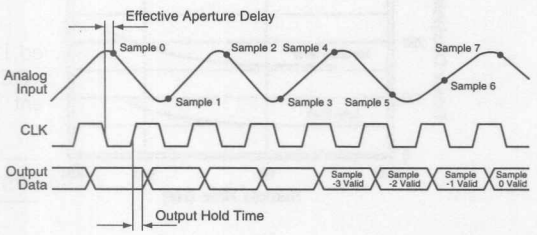


Figure 1: Timing Diagram

The CLC949 is designed to operate with a CMOS clock signal. To obtain the lowest possible noise when digitizing a high frequency input, more care must be taken in the generation of this clock than is usually accorded to CMOS Clocks. To minimize aperture jitter induced errors, the CLK needs to have as low a jitter as possible and as fast an edge rate as possible. To obtain a very low jitter clock from a sinusoidal source, the circuit shown in Figure 2 is recommended.

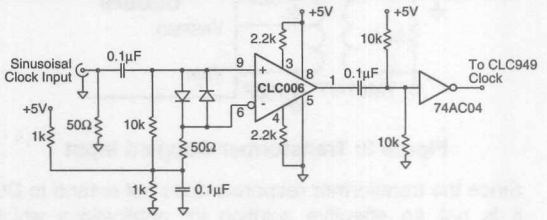


Figure 2: Clock Generation

Here the CLC006 cable driver is used as a comparator to generate a high speed clock. The CLC006 has less than 2ps of jitter and has rise and fall times less than 1ns. The CLC006 output is then buffered by a 74AC04 which maintains fast edge rates and provides CMOS levels for the CLC949. If there is excessive jitter in the CLK, then the digitized signal will exhibit an excessive amount of noise, especially for high frequency inputs. For a more detailed description of this phenomenon, please read the Comlinear Application Note AD-03.

In addition to the circuitry generating the clock, the layout of the clock distribution network can affect the overall performance of the converter. To obtain the best possible performance, a clock driver with very low output impedance and fast edge rates such as the 74AC04, should be placed as close as possible to the CLC949 clock input pin. Additional length in the circuit trace for the clock will cause an increase in the jitter seen by the converter. On the CLC949 evaluation board, the E949PCASM, there is less than 1/16th of an inch between the 74AC04 that is driving the clock input and the input to the CLC949. If the system has several CLC949s, and jitter is liable to generate problems, then use a separate clock driver for each CLC949. Each driver should be placed as close to the converter that it is driving as is practicable.

Driving the Differential Input

The CLC949 has a differential input with a common mode voltage of 2.25V. Since not all applications have a signal preconditioned in this manner there is often a need to do a single-ended-to-differential conversion and to add offset. In systems which do not need to be DC coupled, the best method for doing this is with an RF transformer such as the Minicircuits TMO1-1T. This is an RF transformer with a center tapped secondary which will operate over a frequency range of 50kHz to 200MHz. You can offset the input and split the phases simply by connecting the center tap to the mid scale reference output (V_{REFMO}) as shown in Figure 3.

This set up can be realized on the CLC949 evaluation board by enabling option 1. See E949PCASM datasheet for details. A transformer coupled input will allow the CLC949 to exhibit the best possible distortion performance for high frequency input signals.

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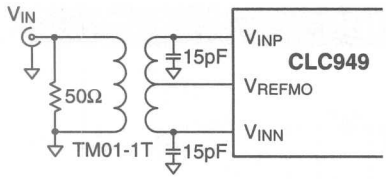


Figure 3: Transformer Coupled Input

Since the transformer response does not extend to DC it is not an effective solution for applications which require DC coupled inputs.

To drive the input of the CLC949, and retain DC information, an amplifier configuration is required. Comlinear suggests the use of the circuit shown in Figure 4. This circuit is used on the E949PCASM.

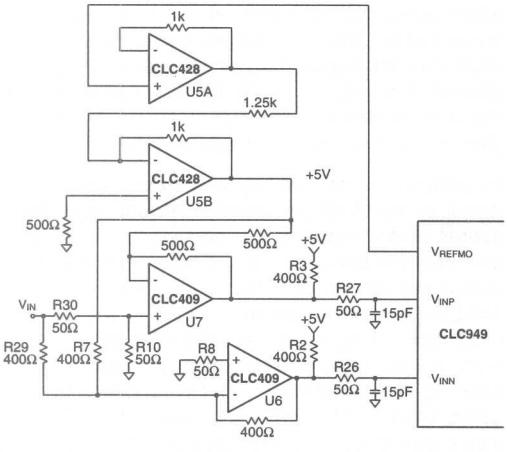


Figure 4: Amplifier Coupled Input

In this circuit U7 buffers the analog input with a gain of +1, and U6 buffers the input with a gain of -1. The circuit has been designed so that U6 and U7 have the same loop gain, thereby offering the best possible match of their AC characteristics. U5 is used to generate the required offset voltages which are summed into the input signal via U6 and U7. The CLC409 was selected for U6 and U7 due to its current feedback topology which allows for very low distortion even at high frequencies, and its excellent phase linearity. Phase match between U6 and U7 is critical for good pulse response. To generate the D.C. offsets, the CLC428 dual Op-amp was selected. The CLC428 is a voltage-feedback op amp with very good DC characteristics, and the large bandwidth makes the output impedance low over a wide range of frequencies, allowing good AC performance.

Regardless of how the input is driven, a small capacitor (15pF) should be added from the V_{INP} and V_{INN} terminals to GND. This will help to reduce the current transients that are generated by the CLC949 inputs during sampling.

Reference Generation

The CLC949 has internally generated reference voltages. To use these references, you must externally connect the reference inputs by shorting V_{REFPO} to V_{REFP} and V_{REFNO} to V_{REFN}. During the conversion cycle, the impedance on these four pins varies dynamically. To maintain stable biases on these pins you must bypass them with 0.1µF to GND. If you want to provide an external reference, then you have to be careful to provide low output impedance drivers to the V_{REFP} and V_{REFN} pins. Bypass capacitors on all reference pins are recommended for best performance.

Bias Control

One of the unique features of the CLC949 is that it allows you to set the internal bias current of the device. When designing an A/D converter a tradeoff is made between the amount of power dissipated and the performance. The CLC949 allows you to make this tradeoff yourself. The bias current is controlled by the pins BC0 and BC1. These two pins are digital input pins from which one of three discrete bias points may be selected (see truth table on page 4 of this datasheet) or an external bias may be provided through the analog bias control pin BIASC. If BC0 and BC1 are left open, they will drift low and provide the default bias condition which results in 220mW of dissipation at 20MHz sampling rate. The actual power dissipated by the device is a function of both the bias condition and the sample rate. The relationship between power and speed is shown for the three discrete bias points in Figure 5.

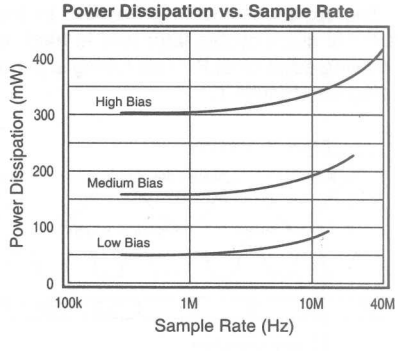


Figure 5: Power Dissipation vs. Sample Rate

As the bias is turned up, the ability of the CLC949 to handle high frequency inputs and the power dissipation of the CLC949 increases. To use the BIASC pin, attach a resistor from the pin to V_{DDA}. The current drawn by this resistor is mirrored in the device to set the internal bias currents. A smaller value resistor will result in higher bias currents and higher performance. Beyond a certain point, additional improvement is not seen, although power continues to increase. For this reason, it is recommended that bias setting resistors of less than 10K not be used. To generate the graph in

Figure 6 a CLC949 was set to sample a signal 1dB below full scale with a frequency of 1/2 the sample rate. The bias current was then turned up until the SNR was better than 65dB and the SFDR exceeded 72dB. The axis on the left shows the power that was dissipated by the device as a function of speed, whereas the other curve uses the axis on the right to show the resistor value required to obtain this bias.

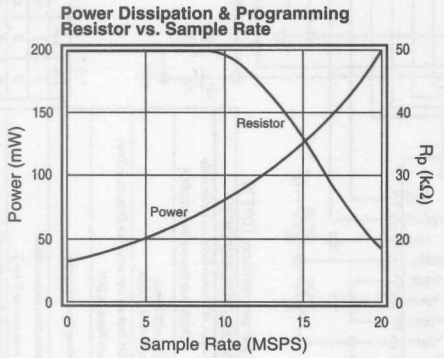


Figure 6: Power Dissipation & Programming Resistor vs. Sample Rate

Dynamic Power Down

In systems where you do not use the A/D converter continually, and low power consumption is a key requirement, the power to the CLC949 can be turned down while it is not being used. This is done through the use of the BIASC pin, and a programming resistor to the power supply. When the potential on this resistor is brought low, the part goes into a sleep mode which saves power. This can be accomplished by connecting the bias setting resistor to a CMOS gate as shown in Figure 7. In sleep mode the CLC949 will draw approximately 8mA, or 40mW on a 5V supply.

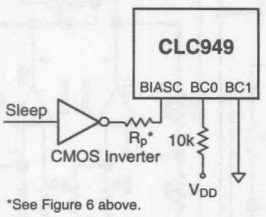


Figure 7: Dynamic Power Savings

PCB Layout

The keys to a successful CLC949 layout are a substantial low-impedance ground plane, short connections in and out of the data converter, and proper power supply decoupling. The use of a socket for the final design is not recommended but if one must be used during debug or prototyping, then Comlinear recommends the McKenzie #PLCC-44P-T-SMT socket which has low parasitic impedances. The traces from the clock source to the CLC949 should be as short as possible, if forced to put the clock driver more than a couple of centimeters away from the CLC949, then add a buffer for the clock right next to the CLC949.

There is an evaluation board available for the CLC949 (E949PCASM) This board can be used to quickly evaluate the performance of the CLC949 data converter. Use of this evaluation board as a model for your PCB layout is recommended. The schematic for this evaluation board is shown in Figure 8 on the following page. The board layout for the E949PCASM is shown in the E949PCASM datasheet.

Power Supplies, Grounding and Bypassing

To obtain the best possible performance from high speed devices, you must pay close attention to power supplies, bypassing and grounding. This applies not only to the A/D converter itself but to the entire system.

The recommended supply decoupling scheme for the CLC949 includes:

- One 0.01 to 0.033µF capacitor between each power pin and GND.
- One 6.8 to 10µF capacitor per board, placed no more than a few inches from the A/D connected between V_{DD} and GND.
- One 0.1µF capacitor from each of the reference inputs (V_{REFP}, V_{REFN}, V_{REFPC}, V_{REFNC}) to GND.
- If the board has supplies that include excessive digital switching noise, then ferrite beads in series with the power feed to the A/D should also be included.
- Proper bypassing of all other integrated circuits on the board, especially digital logic I.C.s.

Applications Support

Comlinear maintains a staff of applications engineers who are available for design and applications assistance. To make use of this service call **(800) 776-0500 or (970) 225-7422**.

Package Thermal Resistance

Package	θjc	θja
Plastic (ACQ)	10°C/W	35°C/W

Ordering Information

Model	Temperature Range	Description
CLC949ACQ	0°C to +70°C	44-pin PLCC

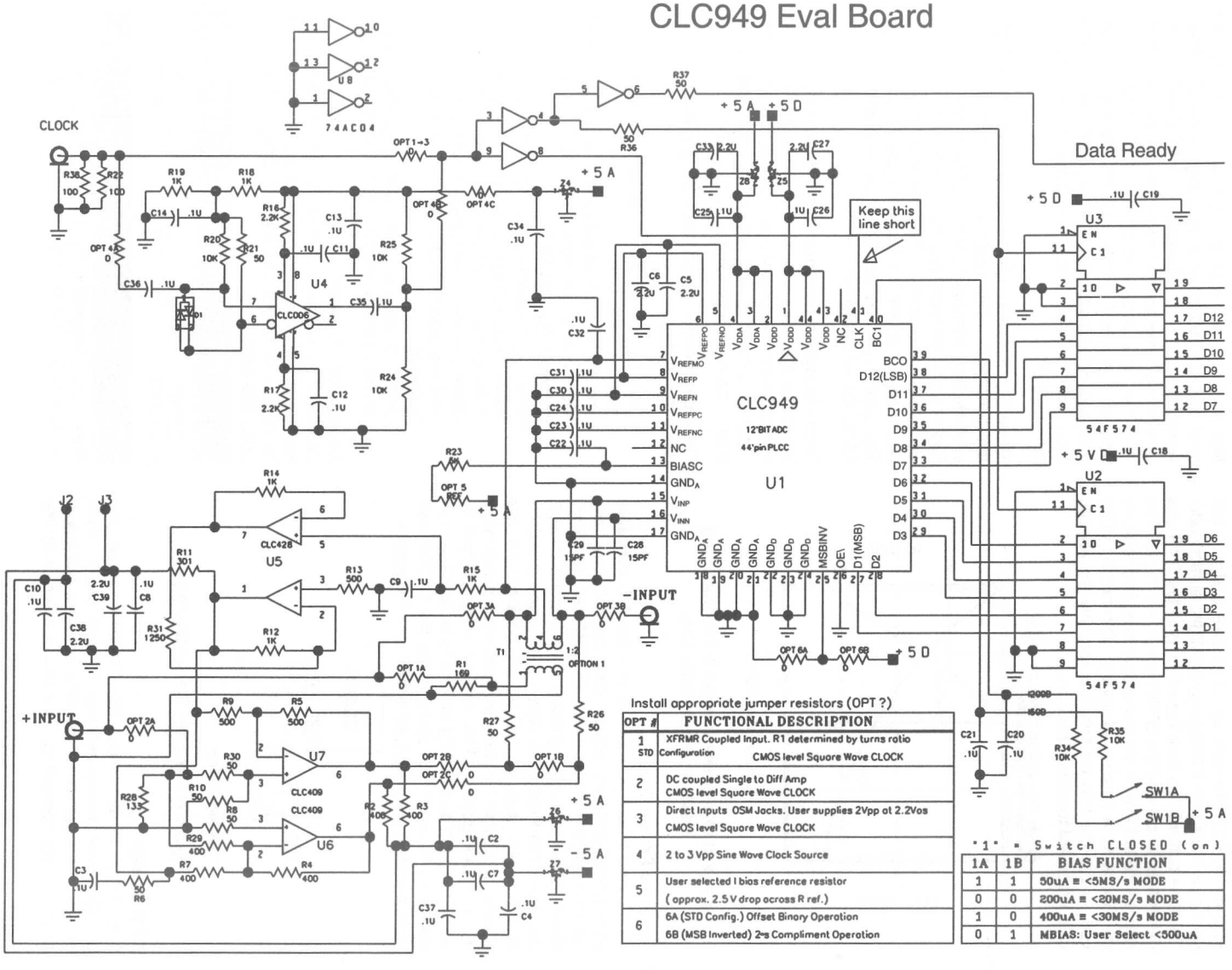


Figure 8: CLC949 Evaluation Board

Serial Digital Interface
Contents

Comlinear
A National Semiconductor Company

Serial Digital Cable Driver with Adjustable Outputs

CLC006

APPLICATIONS:

- Digital video routers, DAs, switchers
- $4f_{SC}$, 4:2:2 and 360Mbps serial digital video interfaces
- Lower power replacement for GS9008 in most applications
- Cable driver for digital data transmission

FEATURES:

- No external pull-down resistors required
- Two amplitude-adjustable outputs
- 650ps rise and fall times
- Operates from single +5V or -5.2V supply
- Low power dissipation
- DC to >400Mbps

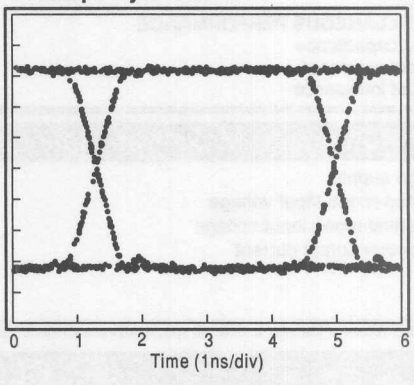
DESCRIPTION

The CLC006 is a monolithic cable driver, designed to conform to the SMPTE 259M standard for the transmission of serial digital video signals. The CLC006 operates at data rates from DC to over 400Mbps, with nominal rise and fall times of 650ps. An internal bandgap reference defines an accurate, low drift, $1.6V_{pp}$ output swing at each of two outputs. When used with a back-matching resistor to drive a terminated cable, the result is a $0.8V_{pp}$ swing at the load. With the addition of one external resistor the output swing may be adjusted from the nominal $1.6V_{pp}$ down to $0.7V_{pp}$. With three external resistors the output swing can be adjusted from $0.7V_{pp}$ to greater than $2V_{pp}$.

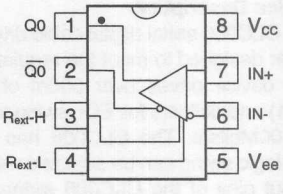
The CLC006 draws less quiescent current than other solutions, and requires no external pull-down resistors to bias the outputs. The result is low power dissipation (185mW with both outputs loaded) and less board space used. The DC coupled differential inputs may be driven with ECL level signals or with DC-shifted ECL signals. Additionally, high voltage gain allows operation with input signal swings that are substantially smaller than ECL swings. As a result, the CLC006 makes an excellent general-purpose, high-speed driver for digital applications.

The CLC006 is packaged in an 8-pin SOIC package and operates from a single +5V or -5.2V power supply.

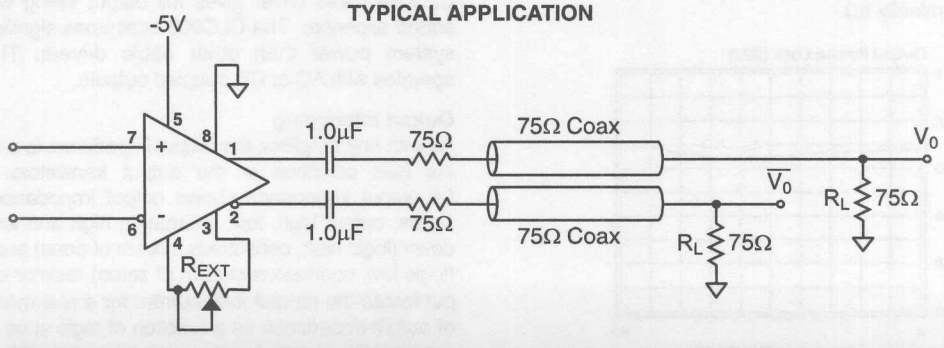
270Mbps Eye Pattern



PINOUT
SOIC



TYPICAL APPLICATION



CLC006 Electrical Characteristics (V_{cc} = 0V, V_{ee} = - 5V; unless specified)

Parameters	Conditions	Typ	Guaranteed MIN/MAX			Units	Notes
Ambient Temperature	CLC006AJE	+25°C	+25°C	0 to 70°C	-40 to 85°C		
STATIC DC PERFORMANCE							
supply current	no load	34	37	39	39	mA	
supply current	driving 2 loads	37				mA	
input bias current		10	30	50	50	µA	
output HIGH voltage		-1.7				V	
output LOW voltage		-3.3				V	
output amplitude	at the load, $R_{EXT} = \infty$	800	750/850	750/850	750/850	mV_{pp}	1
output amplitude	at the load, R_{EXT} = 10kΩ	610				mV_{pp}	1
common mode input range upper limit		-0.7	-0.8	-0.8	-0.8	V	
common mode input range lower limit		-2.6	-2.5	-2.5	-2.5	V	
minimum differential input amplitude		200	200	200	200	mV	
power supply rejection ratio	V_{ee} supply	26	20	20	20	dB	
AC PERFORMANCE							
output rise & fall time		650	425/825	400/850	450/850	ps	
overshoot		5				%	
propagation delay		1.0				ns	
duty cycle distortion		50				ps	2
residual jitter		25				ps_{pp}	3
MISCELLANEOUS PERFORMANCE							
input capacitance		1.0				pF	
output resistance		5				Ω	
output inductance		6				nH	

Absolute Maximum Ratings

voltage supply	6V
common-mode input voltage	V_{ee} to V_{cc}
differential-mode input voltage	±5V
continuous output current	30mA

Comlinear reserves the right to change specifications without notice.

Ordering Information

Model	Temperature Range	Description
CLC006AJE	-40°C to +85°C	8-pin SOIC

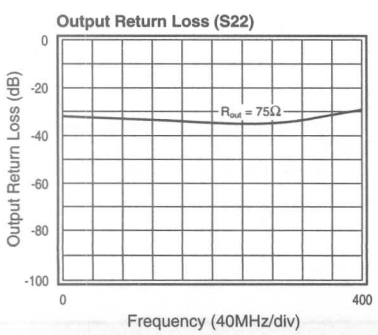
Notes

1) Voltage swing at the load as in Figure 2.
2) t_{pd} (low to high) – t_{pd} (high to low).
3) Noise plus pattern-induced components.

CLC006 OPERATION

Device Description

The CLC006 serial digital cable driver is an ECL-compatible buffer designed to meet the requirements of SMPTE 259M. The device drives over 300m of cable (Belden 1505 or 8281) and delivers full ECL swing to a matched 75Ω load up to 400Mbits/s. The CLC006 has two adjustable outputs. The logic swing can be adjusted with external resistors. The output pins of the CLC006 swing twice the load peak-to-peak logic level; the impedance matching network (load and backmatching resistor) cuts this in half. The output resistance is nominally 5Ω.



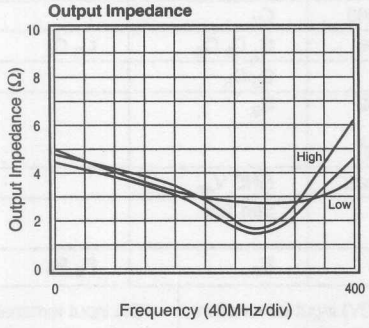
Adding a 75Ω resistor in series with the output yields return loss in compliance with SMPTE standards.

The CLC006 output stage is self-biasing, unlike standard ECL devices. The output stage is a complementary bipolar emitter follower, similar to an op-amp; it does not require a pull-down resistor. Considerable power and cost savings result from this class AB output topology. Typical ECL (class A emitter follower) devices require an emitter load resistor and termination voltage (50Ω & -2V or 150Ω & -5V). The CLC006 cable driver gives full output swing without this added expense. The CLC006 consumes significantly less system power than other cable drivers. The device operates with AC or DC coupled outputs.

Output Interfacing

As with any amplifier, the output impedance is a function of the bias condition of the output transistors. The plot for output impedance shows output impedance in three states; output high, low, alternating high and low. A pull-down (logic high, continuous stream of ones) and a pull-up (logic low, continuous stream of zeros) resistor on the output forces the correct load current for a real measurement of output impedance as a function of logic state. The output impedance graphs also show a curve without a pull-

up/down. While the device would never operate in this DC condition, it does simulate the average output impedance midway between extremes; a continuous stream of alternating zero and one.



Input Interfacing

The CLC006 was designed to be driven directly from ECL outputs. The electrical specifications are guaranteed with differential drive. You may use a single-ended source if you can tolerate some degradation from specified jitter performance at high bit rates. In either case the source must provide bias current to the driven input. Bias the static input with a resistive divider (total resistance 1kΩ) to V_{cc} -1.3V. The following caution on PECL operation is especially important for single-ended drive.

Positive ECL (PECL) Operation

The CLC006 can be used with positive ECL (PECL: V_{cc} = +5V, V_{ee} = 0V) supplies (Figure 1). Due to the AC coupling capacitors on the output, the same ECL peak-to-peak swing levels will appear at the load. ECL output levels are referenced to the positive supply. Keeping clean ground is usually easier than any other voltage. The CLC006 logic internal reference levels are derived from the positive supply, V_{cc}. The PSRR to V_{cc} is low (about 0.5dB). As with any ECL device, PECL operation requires care in bypassing the positive supply. Use 3 bypass capacitors (6.8μF, 0.1μF, 100pF). A choke in series with V_{cc} further reduces supply noise coupling. Keep in mind that the inputs must have a source of bias current. A resistive divider between the supplies set to 3.7V (5V - 1.3V) will both bias the inputs and set the logic threshold. A resistive divider (total series resistance about 1kΩ) at 1.3V below the more positive supply works well.

Output Amplitude Adjustment

The CLC006 needs no external components to drive a 75Ω load to 800mV peak-to-peak. Adding external resistors allows adjustment of the output amplitude. The simplest circuit to reduce the output to <800mV is Figure 2.

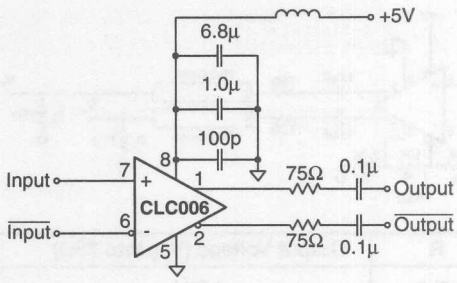
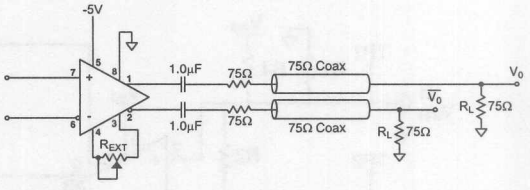


Figure 1. Positive ECL Circuit

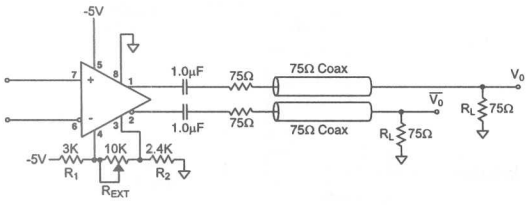
One resistor between pins 3 and 4 trims the output from 800mV to a more optimal value to drive some serial digital video receivers. This resistor can be fixed or variable. Find typical resistor/output voltage values in the tables under the suggested schematics. Add bypass capacitors on pins 3 and 4 to reduce output coupling to the reference pins. Omitting them slightly degrades jitter performance from the datasheet specifications. Adding two more resistors (Figure 3) allows the freedom to adjust the output to >800mV, as well as <800mV. With fixed R_1, R_2 (3kΩ, 2.4kΩ, respectively) the table in Figure 3 shows R vs. typical output voltage. For maximum output voltage, R = ∞, R_1 = R_2 = 2.2kΩ. For reduced output only, consider Figure 2 for its simplicity and power supply rejection.



R	Output Voltage (V_{pp} into 75Ω)
open	800mV
30kΩ	755
20k	690
10k	610
5k	550
2k	460
1k	405
0	340

Figure 2. Reduced Output

8



R	Output Voltage (V_{pp} into 75Ω)
10kΩ	1.02V
5k	905mV
2.6k	755
2k	725
1k	585
0	350

Figure 3. Increasing and Decreasing Output

NOTE: Bypassing pin 3 to ground (0.01µF) may improve transient response in some circuit layouts.

CLC006 Evaluation Board Components

Component	006 used	006 not used
75Ω BNC[1]	V_{in} + , V_{in} - , Q_0 $\overline{Q_0}$	Q_1 $\overline{Q_1}$
0.01µF 1206	C_7	
0.1µF 1206	C_1 C_2 C_8	C_3 C_4
33pF[2]	C_5 C_6	
6.8µF 5032 (Digikey #PCT3685)	C_9	
Banana Jack	GND V_{ee}	
deltaV_{out} resistors	See Text	
75Ω 1206	R_7	R_8 R_9
ECL (50Ω/-2V) input termination: R_1, R_3 = 82.5Ω 1206 R_4, R_5 = 127Ω 1206		75Ω input termination: R_1, R_3 = 75Ω 1206 R_4, R_5 not used

[1]Amphenol 31-5329-72RFX.
[2]As required, see text.

Evaluation Board

Comlinear provides a free evaluation board, part number 730056. This board offers provisions to experiment with interfacing and output level adjustment. This board is used by both CLC006 and CLC007 (fixed outputs). The general schematic is Figure 4. Component values for the CLC006 are in the table above. For proper ECL device termination, the inputs must look like 50Ω at -2V. Figure 4 shows how. R2 is for differential input termination. This is most useful for twisted pair termination. Use simple 75Ω input termination to ground for bench testing.

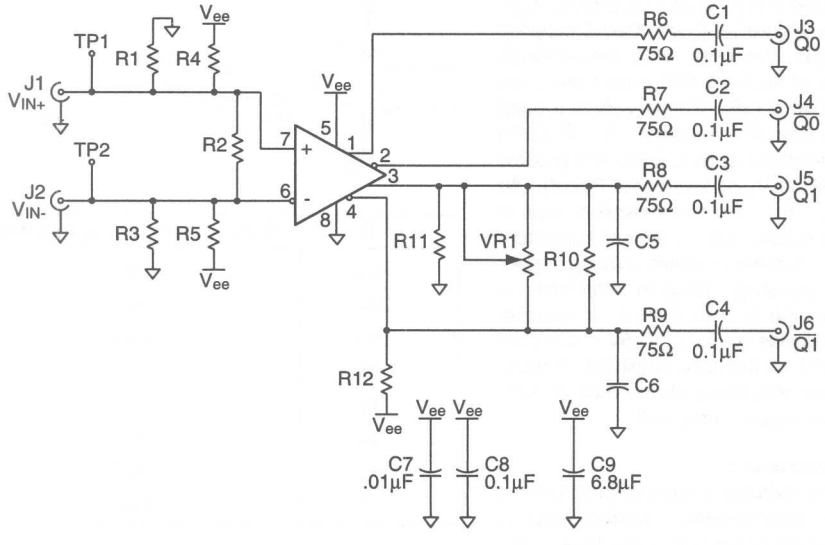


Figure 4. Cable Driver Evaluation Board Schematic

Applications Support

Comlinear maintains a staff of applications engineers who are available for design and applications assistance. To make use of this service call **(800) 776-0500 or (970) 225-7422.**

Comlinear
A National Semiconductor Company

Serial Digital Cable Driver

CLC007

APPLICATIONS:

- Digital video routers, DAs, switchers
- $4f_{SC}$, 4:2:2 and 360Mbps serial digital video interfaces
- Lower power replacement for GS9007 and MC10EL89
- Cable driver for digital data transmission

FEATURES:

- No external pull-down resistors required
- Four outputs (two pairs)
- 650ps rise and fall times
- Operates from single +5V or -5.2V supply
- Low power dissipation
- DC to >400Mbps

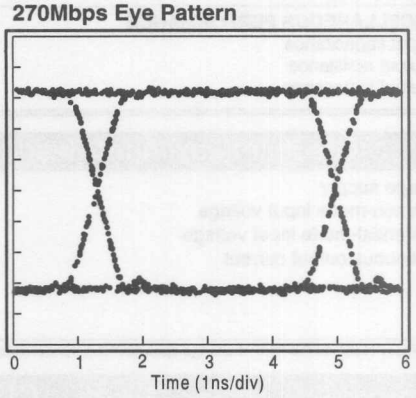
DESCRIPTION

The CLC007 is a monolithic cable driver designed to conform to the SMPTE 259M standard for the transmission of serial digital video signals. The CLC007 operates at data rates from DC to over 400Mbps, with nominal rise and fall times of 650ps. An internal bandgap reference defines an accurate, low drift, 1.6Vpp output swing at each of four outputs. When used with a back-matching resistor to drive a terminated cable, the result is a $0.8V_{pp}$ swing at the load.

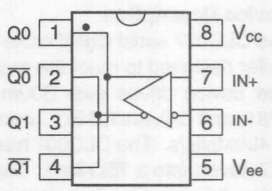
The CLC007 draws much less quiescent current than other solutions, and requires no external pull-down resistors to bias the outputs. The result is low power dissipation (200mW with all four outputs loaded) and less board space used. The DC coupled differential inputs may be driven with ECL level signals or with DC- shifted ECL signals. Additionally, high voltage gain allows operation with input signal swings that are substantially smaller than ECL swings. As a result, the CLC007 makes an excellent general-purpose, high-speed driver for digital applications.

The CLC007 is packaged in an 8-pin SOIC package and operates from a single +5V or -5.2V power supply.

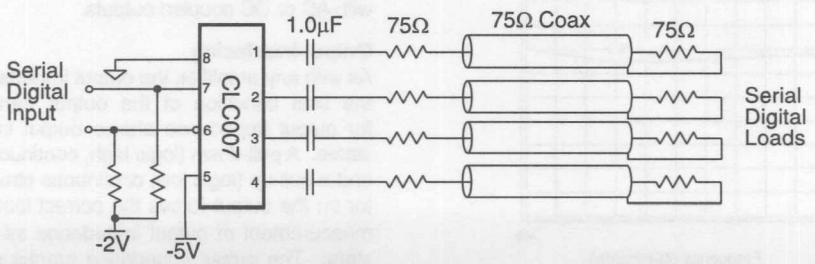
270Mbps Eye Pattern



PINOUT
SOIC



TYPICAL APPLICATION



8

CLC007 Electrical Characteristics (V_{cc} = 0V, V_{ee} = -5V; unless specified)

Parameters	Conditions	Typ	Guaranteed MIN/MAX			Units	Notes
Ambient Temperature	CLC007AJE	+25°C	+25°C	0 to 70°C	-40 to 85°C		
STATIC DC PERFORMANCE							
supply current	no load	34	37	39	39	mA	
supply current	driving 4 loads	39				mA	
input bias current		10	30	50	50	µA	
output HIGH voltage		-1.7				V	
output LOW voltage		-3.3				V	
output amplitude	at the load	800	750/850	750/850	750/850	mV_{pp}	1
common mode input range upper limit		-0.7	-0.8	-0.8	-0.8	V	
common mode input range lower limit		-2.6	-2.5	-2.5	-2.5	V	
minimum differential input amplitude		200	200	200	200	mV	
power supply rejection ratio	V_{ee} supply	26	20	20	20	dB	
AC PERFORMANCE							
output rise & fall time		650	425/825	400/850	450/850	ps	
overshoot		5				%	
propagation delay		1.0				ns	
duty cycle distortion		50				ps	2
residual jitter		25				ps_{pp}	3
MISCELLANEOUS PERFORMANCE							
input capacitance		1.0				pF	
output resistance		5				Ω	
output inductance		6				nH	

Absolute Maximum Ratings

voltage supply	6V
common-mode input voltage	V_{ee} to V_{cc}
differential-mode input voltage	±5V
continuous output current	30mA

Comlinear reserves the right to change specifications without notice.

Ordering Information

Model	Temperature Range	Description
CLC007AJE	-40°C to +85°C	8-pin SOIC

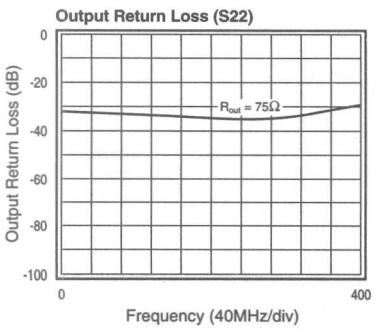
Notes

1) Voltage swing at double-terminated load.
2) t_{pd} (low to high) – t_{pd} (high to low).
3) Noise plus pattern-induced components.

CLC007 OPERATION

Device Description

The CLC007 serial digital cable driver is an ECL-compatible buffer designed to meet the requirements of SMPTE 259M. The device drives over 300m of cable (Belden 1505 or 8281) and delivers full ECL swing to a matched 75Ω load up to 400Mbits/s. The CLC007 has four outputs that drive fixed ECL levels into a 75Ω load. The output pins of the CLC007 swing twice the load peak-to-peak logic level; the impedance matching network (load and backmatching resistor) cuts this in half. The output resistance is nominally, 5Ω.



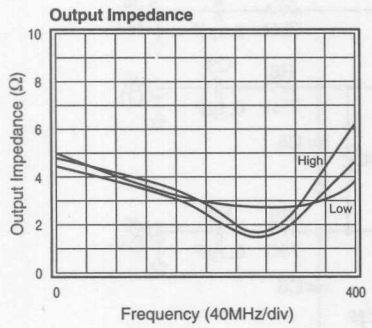
Adding a 75Ω resistor in series with the output yields output levels and return loss in compliance with SMPTE standards.

The CLC007 output stage is self-biasing, unlike standard ECL devices. The output stage is a complementary bipolar emitter follower, similar to an op-amp; it does not require a pull-down resistor. Considerable power and cost savings result from this class AB output topology. Typical ECL (class A emitter follower) devices require an emitter load resistor and termination voltage (50Ω & -2V or 150Ω & -5V). The CLC007 cable driver gives full output swing without this added expense. The CLC007 consumes significantly less system power than other cable drivers. The device operates with AC or DC coupled outputs.

Output Interfacing

As with any amplifier, the output impedance is a function of the bias condition of the output transistors. The plot for output impedance shows output impedance in three states. A pull-down (logic high, continuous stream of ones) and a pull-up (logic low, continuous stream of zeros) resistor on the output forces the correct load current for a real measurement of output impedance as a function of logic state. The output impedance graphs also show a curve

without a pull-up/down. While the device would never operate in this DC condition, it does simulate the average output impedance midway between extremes; a continuous stream of alternating zero and one.



Input Interfacing

The CLC007 was designed to be driven directly from ECL outputs. The electrical specifications are guaranteed with differential drive. You may use a single-ended source if you can tolerate some degradation from specified jitter performance at high bit rates. In either case the source must provide bias current to the driven input. Bias the static input with a resistive divider (total resistance 1kΩ) to V_{cc} -1.3V. The following caution on PECL operation is especially important for single-ended drive.

Positive ECL (PECL) Operation

The CLC007 can be used with positive ECL (PECL: V_{cc} = +5V, V_{ee} = 0V) supplies (Figure 1). Due to the AC coupling capacitors on the output, the same ECL peak-to-peak swings will appear at the load. ECL output levels are referenced to the positive supply. Keeping clean ground is usually easier than any other voltage. The CLC007 logic internal reference levels are derived from the positive supply, V_{cc}. The PSRR to V_{cc} is low (about 0.5dB). As with any ECL device, PECL operation requires care in bypassing the positive supply. Use 3 bypass capacitors (6.8μF, 0.1μF, 100pF). A choke in series with V_{cc} further reduces supply noise coupling. Keep in mind that the inputs must have a source of bias current. A resistive divider between the supplies set to 3.7V (5V - 1.3V) will both bias the inputs and set the logic threshold. A resistive divider (total series resistance about 1kΩ) at 1.3V below the more positive supply works well.

Evaluation Board

Comlinear provides a free evaluation board, part number 730056. This board offers provisions to experiment with interfacing and output level adjustment. This board is used by both the CLC007 and CLC006 (two adjustable outputs).The general schematic is Figure 2. Component values are in the table below. For proper ECL device termination, the inputs must look like 50Ω at -2V. Figure 2 on the next page shows how. R2 is for differential input termination. This is most useful for twisted pair termination. Use simple 75Ω input termination to ground for bench testing.

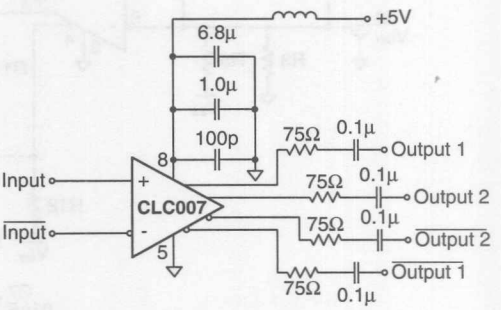


Figure 1. Positive ECL Circuit

CLC007 Evaluation Board Components

Component	007 used	007 not used
75Ω BNC[1]	V_{in} + , V_{in} - , Q_0 $\overline{Q_0}$, Q_1, $\overline{Q_1}$	
0.01μF 1206	C_7	
0.1μF 1206	C_1 C_2 C_3 C_4 C_8	
33pF[2]		C_5 C_6
6.8μF 5032 Digikey #PCT3685	C_9	
Banana Jack	GND V_{ee}	
deltaV_{out} resistors		VR_1 R_{1o} R_{11} R_{12}
75Ω 1206	R_6 R_7 R_8 R_9	
ECL (50Ω/-2V) input termination: R_1, R_3 = 82.5Ω 1206 R_4, R_5 = 127Ω 1206		75Ω input termination: R_1, R_3 = 75Ω 1206 R_4, R_5 not used

[1]Amphenol 31-5329-72RFX.
[2]As required, see text.

Applications Support

Comlinear maintains a staff of applications engineers who are available for design and applications assistance. To make use of this service call **(800) 776-0500 or (970) 225-7422**.

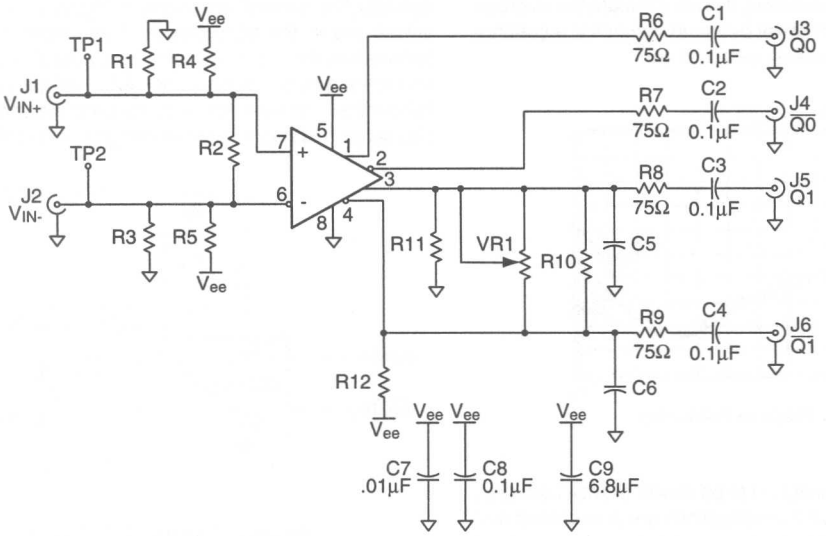


Figure 2. Cable Driver Evaluation Board Schematic

Application Notes
Contents

Application Note OA-24

Measuring and Improving Differential Gain and Differential Phase for Video

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OA-24 April 1994

Measuring Differential Gain and Differential Phase of Video Op-Amps

Differential gain (DG) and differential phase (DP) are two specifications that designers of composite video systems use everyday. We will define them here just to be sure we are all speaking the same language, and to ensure understanding of the rationale of the test technique used by Comlinear.

Composite video encodes brightness (luminance), timing (sync), and colour (chrominance) into one channel. Luminance is the voltage offset from a reference, or "black", level. Sync appears at a level defined as "blacker than black." Chrominance is encoded as a high-frequency (with respect to the luminance signal) subcarrier. The average value (mid-point) of the chrominance is the luminance. The color has two "dimensions": amplitude which determines the saturation, and phase relative to a reference chrominance burst which encodes the hue. For example, pink has the same relative phase as red, but of a lower amplitude, hence a less saturated red. Red in NTSC is shifted 103.7° from the reference, green 241.3°.

DG and DP are measured at one of two chrominance subcarrier frequencies. NTSC (National Television Systems Committee, 1953) uses a 3.579545MHz color subcarrier. Phase Alternation Line (PAL) alternates the phase of the reference burst with every scan line. The PAL subcarrier frequency is 4.433619MHz.

Differential phase is a change in chrominance (high-frequency) phase with luminance level. This manifests itself in the picture as a color hue shift as the illumination changes. A blue parrot indoors does not become a purple parrot in the sun. Differential gain is a change in chrominance gain with luminance level. The saturation changes in the viewed scene as the brightness varies. A red shirt at noon must not turn pink at night. Both are distortions which, if sufficiently large, can be perceived by the eye.

Another way to think of DG error in a signal channel or amplifier is a magnitude variation of a high-frequency sinusoid (the subcarrier) as its offset changes. This offset can be, at its simplest and crudest, a DC offset. It can also take the form of a low-frequency sinusoid or ramp. Similarly, an alternative way to view DP is as a change in the carrier phase shift of the channel over the range of offset simulating the luminance (see Figure 1).

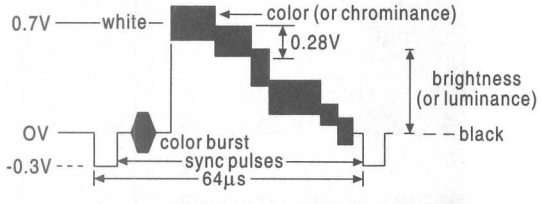

Figure 1

The traditional way of measuring the DG and DP of broadcast video equipment such as a switcher or a distribution amplifier, DA, is with a vectorscope. A distribution amp can have several integrated or discrete amplifiers between the input and output. Vectorscopes can measure such high-level systems to <1% DG and <1°DP. Newer video test equipment based on digital technology, such as the Tektronix ®VM700, can make measurements to <0.03% and <0.03° . This resolution results after the DG and DP errors of the video test signal generator have been calibrated out. This equipment is adequate to measure a complete video system, but cannot measure an individual operational amplifier to the required resolution.

Video designers usually take a worst-case approach when selecting a video op-amp. Consider, for example, the design of a DA with five amplifiers between the input and output. The desired overall system specification for this DA board is to be 0.05% DG and 0.05° DP. One then assumes each of the five op-amps will contribute "+0.01%" and "+0.01°" of DG and DP, respectively. These errors will then add "in phase" for the total of "+0.05." There is not usually a sign associated with DG and DP, rather, the absolute value is used. The VM700 measures signed DG and DP for each step in a modulated staircase. The overall DG and DP, however, are displayed as an unsigned peak-to-peak magnitude. Modern video test equipment can measure the final DA but cannot measure the individual op-amps with the required resolution. Imagine, as well, the design of a system with better than 0.05 numbers. If it were possible to select one op-amp with +0.01% DG and another with -0.01%, the two would cancel to zero. Some state-of-the-art video test equipment is built this way.

Another concern, especially with advanced video test equipment, is squeezing the most out of an op-amp. Refer to Figure 1, a positive video waveform. The video information is at voltages above 0V (positive video); the sync information is below 0V (negative sync). Video equipment must conform to a standard such as this at the input and output. What happens to the signal in between these external ports is only the designer's business. She may choose to invert the video (negative video, or positive sync) for gamma correction with an inverting summing circuit. Another compelling reason to work with inverted video is that a particular amplifier may have better DG, DP or both, with negative video. The "polarity" of DG and DP may change in a predictable way between negative and positive video. This feature (not a bug) may then be exploited to improve the system DG and DP specifications. It is not easy, using current industry-standard test equipment, to measure negative video DG and DP.

How We Do It

Comlinear uses an HP4195 network analyzer to make DG, DP measurements of its devices and customer circuits. There are many good reasons to choose this particu-

lar machine. The network analyser has the gain and phase measuring capability to resolve significantly less than the 0.01% and 0.01° target specfications in the device under test, DUT. This particular analyzer has a built-in DC source which can be used as an independent sweep variable; single-frequency, CW, gain and phase can be measured and displayed parametrically on the DC source voltage. This allows the behavior of the amplifier over the entire luminance range, both positive and negative video, to be observed and characterized in detail. A qualitative, as well as quantitative, measurement of DG and DP can be made.

Trends in amplifiers can easily be seen. This is not possible with a box which only delivers numbers. Since network analyzers measure gain in V/V or dB, the trace mathematics of the HP4195 enable conversion to percentages. Finally the internal programming capability of this analyzer yields a self-contained DG and DP measurement system, which does not require an external computer and interface hardware/software yet still can be used for other purposes.

The machine needs a few ancillary items to make this specialized measurement. The CLC400 with ±6V supplies boosts the HP4195's DC sourcing ability. The DC source has limited drive current. The measurement of a unity gain buffer requires twice the input signal level, relative to a DUT with a gain of two, in order to maintain the correct output amplitudes. Operating the CLC400 with ±6V supplies increases the maximum output voltage of the device ±3.5V. The lowpass filter, with the CLC400, guarantees a 50Ω output impedance over frequency and DC level from the DC source into the power combiner. The power splitter sums the DC swept source (luminance) and AC oscillator (chrominance) passively, so no DG or DP is introduced into the input test signal. The R/T test set is needed for a çontrolled impedance throughout the test system. Comlinear uses a 50Ω test set for a 50Ω environment. A video designer would most likely have a 75 Ω R/T test set at his disposal. In this case the 50Ω resistor on the output of the CLC400 would be 75Ω, the power combiner and filter would be 75Ω, etc.

The DUT, in a 50Ω system, would have a series 100Ω resistor between the DUT output and the 50Ω, 14dB attenuator. Thus the total driven load is the proper 150Ω for a 75Ω environment. With a 75Ω test set, a series resistor of 75Ω and a 14dB 75Ω pad would be used instead. Multiple video loads can be simulated by adding additional 150Ω resistors between the DUT output pin and earth. The AC test signal and the T2 analyzer input are capacitively coupled to isolate the DC from the source oscillator and from the analyzer receiver. The 14dB attenuator ensures that the test signal to be measured is of sufficiently low amplitude so as not to cause overload and distortions in the analyzer front end.

The software is straightforward. Previously, in Application Note OA-08 [Comlinear 1993-1994 data book, pages 11-27], we did a through calibration and subtracted this from the subsequent DUT measurement. This proved unnecessary once the lowpass filter, described above, was added. It is the change in gain and phase being measured here. The absolute gain or phase at any point on the DC sweep is irrelevant. The measurement to be made is S21. The straight amplitude-ratio measurement format is required here, not decibels. Averaging dB and converting to percent is problematic. The mathematics is easy to understand and program if non-dB measurements are made. The AC source is set to CW mode, the frequency to that of the desired color subcarrier for the system requirements. The amplitudes of the DC and AC sources are set.

Once the instrument has been set up, the measurement can begin. A sweep is triggered over the DC source sweep range. It is not necessary to have a large number of measurement points over the sweep. We measure a total of twenty-one points for clarity in the plotted data--10 negative video, 10 positive video, and one reference black level. For the required resolution a number of measurements are averaged. We have found an average of 30 sweeps to be a good compromise between measurement time and resolution for most op-amps. Some, like the CLC400 and CLC410 with DG, DP ≤0.01, require an average of 50 measurements. There comes a point where further averaging does not enhance resolution.

After the raw data are collected, they are scaled and displayed. The gain data are converted to percentages. The percent gain and the phase data are scaled to fit on the screen. The trace mathematics built into the programming language find the maximum deviation, or peak-to-peak change in gain and phase, over the luminance sweep. Minimum and maximum DG and DP are found along the trace, and can be displayed as does the VM700. The final DG and DP numbers are displayed in addition to the sweep graph. A vectorscope also gives DG and DP as peak-to-peak magnitude. This is in accordance with NTSC standards.

There is one small problem with the programming language in this machine. Oscillator and DC source levels must be hard-coded and cannot be stored as variables for easy experimentation with different circuit gains and attenuations. This isn't too inconvenient, as most op-amps will be tested at a gain of two. The exact hardware chosen will have differing insertion losses which must be taken into account. The AC coupling may necessitate changing the oscillator level slightly between NTSC and PAL subcarrier frequencies. In current practice, engineers use the PAL 4.43MHz frequency, as it is considered to be the more demanding test condition. Also, a piece of equipment is often sold to countries with different broadcast standards. If a product meets the more stringent specification, one size fits all. Often a current feedback amplifier with 200MHz bandwidth at a gain of two displays little difference in DG and DP between the NTSC and PAL frequencies.

The practical upshot of this is that one must determine the appropriate oscillator amplitude and DC sweep range of each individual hardware assemblage empirically, with an oscilloscope. NTSC levels can be found as follows:

- Set the oscillator frequency to 3.58MHz.
- To find the necessary DC sweep range, the AC source oscillator amplitude is first manually set to 1mV, as zero is not allowed by the HP4195 soft ware.
- Adjust the DC level from the front panel to yield 0.714V at the equivalent 75W load, or 1.424V the DUT output.
- When the DC sweep range numbers have been found, these are then entered into the program. It is the programmed start- and stop-sweep volt ages which are displayed on the HP4195 screen.

For example, one of our test setups results in 0.95V at the maximum luminance level. When the HP4195 DC source is set to 0.95V, a DUT at a gain of two has an output of 1.424V. To set the AC oscillator, begin by manually resetting the DC source to 0V. From the front panel, adjust the oscillator amplitude to yield 286mVpp at the equivalent 75ohms load, or 572mVpp at the DUT output. Note the oscillator setting and edit this into the test program (see Figure 2).

Look Carefully At How DG, DP Are Specified In Datasheets

It is much easier to make measurements
than it is to know exactly what you are measuring.
-- J.W.N. Sullivan, physicist, 1928

Figure 3 shows the measurement results of this test system. A CLC406 is shown. DG and DP are measured for both positive and negative sync (negative and positive video, respectively). The marked points show the specified DG and DP, (peak-to-peak) that is quoted in Comlinear's data sheet. Notice that we would get better numbers if we just took the delta between the endpoints of the sweep range, essentially a DC test at only two luminance levels. This is neither what the video standards delineate, or what vectorscopes or the VM700 report. Another interpretation of these standards implies an RMS value of the error. Neither Comlinear or Tektronix do this.

The VM700 display shows the DP/DG as the largest peak-to-peak delta over the luminance range. Simply giving the endpoint delta between black level and the white level can be misleading. DG and DP do not behave linearly with luminance. The VM700 gives signed DG, DP numbers to each step of the modulated staircase, similar to the HP4195 program. Both pieces of equipment can be used for device characterization and screening for best system performance. The final DG, DP number is the worst-case, peak-to-peak magnitude measured over the entire, continuous, luminance range.

Some manufacturers measure gain and phase at 0V and 0.714V and then tell you the difference. With elan, they call this DG and DP in the data sheet discussion. This would only make sense if the amplifier's DG and DP errors were perfectly linear with respect to luminance. Comlinear

R/T Test Set

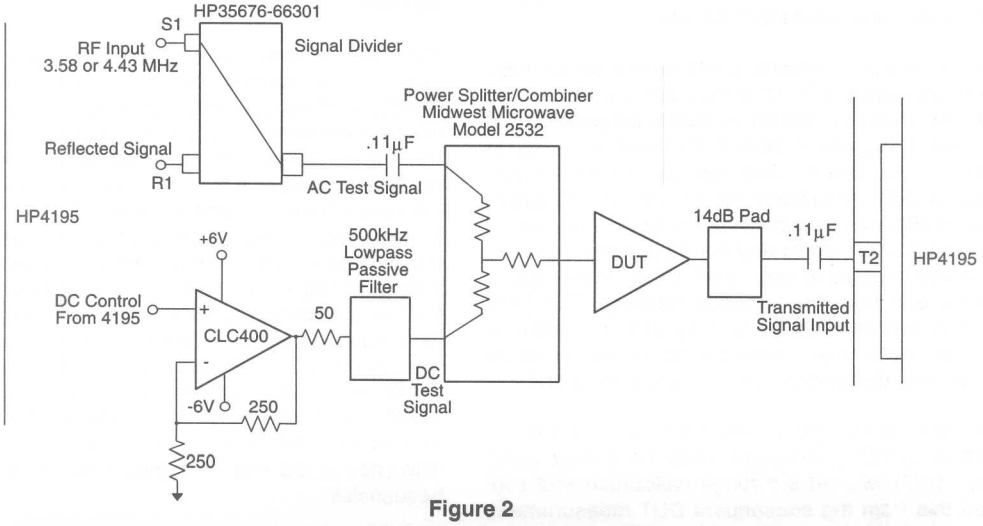

Figure 2

has never measured such a device from any manufacturer. When represented graphically, as in Figure 3, DG and DP are not represented by a straight line, but appear more like a quadratic or even cubic function.

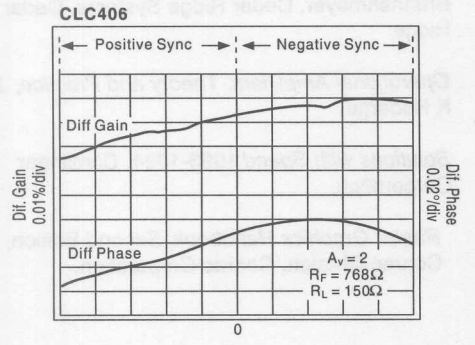

Figure 3

Let's take a closer look at the endpoint measurement. If we could change the intercepts or the shape of this "parabola," we could come up with just about any number for DG and DP we wished (see Figure 3). If one could change the bias current in a typical complementary emitter follower output stage (figure 4), this can be accomplished .

Even complementary bipolar processes leave something to be desired in PNP and NPN matching. The PNP is better than a lateral PNP, but still worse than the NPN. Beta, for one thing, and Early voltage, for another, are not as good as in the NPN. The PNP is the limitation in the output stage. Many Comlinear amplifiers specify the maximum output voltage and current capabilities based on PNP. Often the device is significantly better than this especially when the output is sourcing current from the NPN. The PNP simply cannot sink an equal magnitude of current without compromising other device performance specifications. Some devices, like the CLC406, specify two output voltage ranges, e.g. +3.1, -2.7 (see Figure 4).

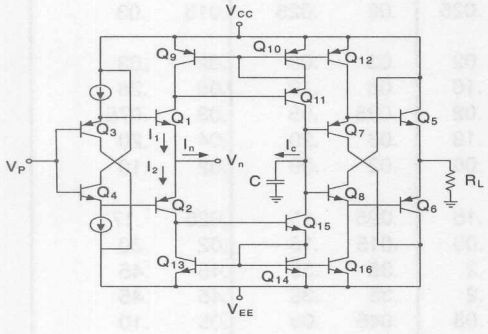

Figure 4

An old trick which can improve the situation (at the expense of burning more circuit power) is to place a "pulldown" resistor on the output. This increases the collector current in the NPN and relieves the burden on the feeble PNP. Notice the effect of this pulldown resistor on DG and DP. Increasing the output stage NPN collector current flattens the DG, DP curves. It is possible to reduce the peak-to-peak DG, DP and force it to zero at the endpoints. Figure 5 shows the CLC430 driving two video loads (total R_L = 75ohms). After adding a pulldown resistor, the DG, DP went from 0.04%, 0.1° to 0.01%, 0.02°.

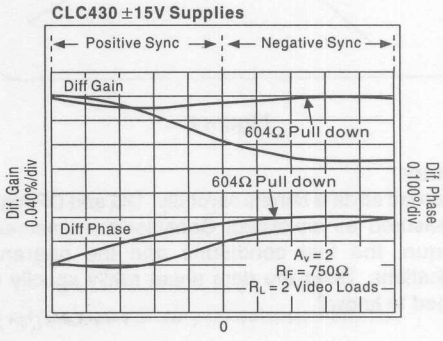

Figure 5

Another test method used in an attempt to measure DG and DP of individual op-amps employs a vectorscope, in spite of its limited resolution. If you assume that five amplifiers in a row each have +0.2 DG and DP, you could theoretically estimate the accumulated error of this chain. We have already seen that amps can be selected to cancel DG, DP errors, so this method is highly suspect (see Figure 6).

Careful reading of the data sheets from other manufacturers will reveal anomalous devices' test conditions for DG and DP. A frequent dodge is to specify a 500Ω or even a 1000Ω load. Most video designers need to know DG and DP into a 150Ω load. DG and DP frequently are not the best at a gain of two. The DUT may be "measured" in a gain of three, or another gain where DG/DP are best. Always look for the amplitude of the test signal. It is rarely specified. The proper luminance may be stated in the test conditions, but the chrominance will not (or vice versa). It should come as no surprise that an amplifier will have better DG and DP when delivering 100mV at 3.58MHz into 1k ohms.

If a manufacturer's DG, DP specifications appear to meet the required test conditions for carrier frequency, luminance levels, load and gain, there is still the question of whether the RMS, peak-to-peak or endpoint delta error is measured. This is rarely, if ever, stated. Finally, you may wish to ask for maximum guarantees on DG and DP.

Comlinear guarantees DG and DP, others offer only typical (see Figure 7).

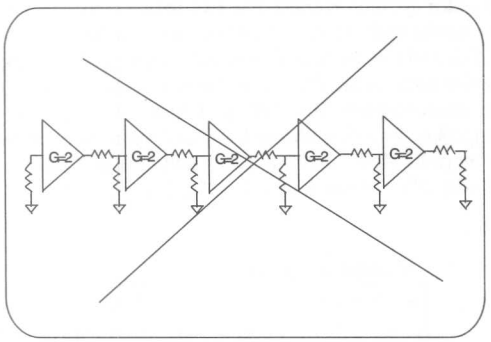

Figure 6

Summary

Please read all data sheets carefully. DG and DP may not be "measured" as you expect. Consider the measurement technique, the test conditions and the guaranteed specifications. Does the data sheet really specify what you need to know?

References

1. *More Random Walks Through Science,* Robert L. Weber, editor, The Institute of Physics, Bristol, England.
2. *Television Measurements*, NTSC Systems, Margaret Craig.
3. *Video Technology Tutorial*, May 1992, Dennis Brunnenmeyer, Cedar Ridge Systems, Cedar Ridge.
4. *Operational Amplifiers, Theory and Practice,* J. K Roberge.
5. *Solutions with Speed* 1993-1994, Comlinear Corporation.
6. *Raster Graphics Handbook*, Second Edition, Conrac Division, Conrac Corporation.

Video - Differential Gain/Phase Comparison

	1 Load		2 Loads		3 Loads		4 Loads	
Part #	DG	Df	DG	Df	DG	Df	DG	Df
CLC231	.005	.09	.006	.10	.007	.11	.008	.14
CLC400	.025	.01	.025	.015	.025	.015	.025	.015
CLC404	.05	.03	.05	.06	.05	.10	.06	.13
CLC406	.03	.02	.03	.025	.04	.03	.04	.03
CLC409	.02	.02	.015	.025	.02	.025	.015	.03
CLC410	.02	.015	.02	.02	.03	.03	.02	.03
CLC411	.02	.05	.05	.10	.06	.19	.08	.26
CLC412	.02	.02	.02	.02	.025	.05	.03	.075
CLC414	.02	.16	.02	.18	.03	.20	.04	.20
CLC415	.02	.07	.02	.08	.02	.09	.02	.10
CLC420	.02	.14	.02	.15	.025	.15	.025	.17
CLC430	.02	.02	.02	.09	.015	.18	.02	.30
CLC431	.1	.1	.2	.2	.35	.35	.45	.45
CLC432	.1	.1	.2	.2	.35	.35	.45	.45
CLC522	.03	.07	.04	.08	.045	.09	.05	.10
CLC532	.05	.01	.11	.08	.19	.15	.34	.24
CLC533	.03	.01	.11	.09	.19	.15	.34	.24

Figure 7

Application Note OA-25

Stability Analysis of Current Feedback Amplifier

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9

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OA-25 May 1995

Introduction

High frequency current-feedback amplifiers (CFA) are finding a wide acceptance in more complicated applications from dc to high bandwidths. Often the applications involve amplifying signals in simple resistive networks for which the data sheets provide adequate information to complete the task. Too often the CFA application involves amplifying signals that have a complex load or parasitic components at the external nodes that creates stability problems.

This application note covers the discussion of using Bode analysis to determine the gain and phase margin while including external parameters. It discusses how to determine the input buffer gain and its effect on the closed-loop gain. A more appropriate mathematical model is developed for a clearer understanding of the poles and zeros of the CFA amplifier. Finally a summary of how parasitic components influence the frequency and time domain response.

Stability Review

Bode analysis is one of the more useful methods for determining stability for an amplifier. When an engineer selects a unity gain stable voltage-feedback amplifier, the internal compensation of the amplifier is transparent to the end user of the amplifier. If the VFA is connected to a complex load and it alters the phase margin then often the part will oscillate or peak the frequency response. Adding external compensation networks with capacitors and resistors will generally stabilize the amplifier. Of course, this is done at the expense of additional components and cost. With a CFA amplifier, stabilization is accomplished by adjusting the feedback resistor. Thus one component, the feedback resistor, controls the phase and gain margin of the amplifier. The most practical way to determine stability of current-feedback amplifier is by Bode plots generated from computer simulations.

Review of Bode analysis

Bode analysis is the easiest predictor for determining amplifier stability. The measurement is based upon creating an open-loop magnitude and phase plot to arrive at the closed-loop stability, indicators of gain and phase margin. The phase margin is derived by finding the intersection of the closed-loop unity gain frequency response curve to the open-loop response curve as shown in Figure 1. At this frequency the phase is read from the phase plot. This value is subtracted from 180° to arrive at the desired phase margin. Similarly the frequency at 180° is used to determine the gain margin in the magnitude plot shown in Figure 1. A recommended phase margin is at least 60° with gain margin of 12dB.

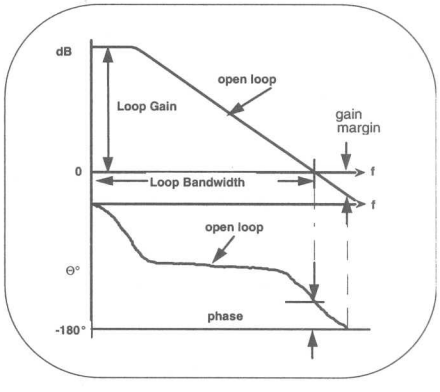


Figure 1 Bode analysis

A Better Model

A practical voltage follower has output resistance which creates a need for a more comprehensive model. That model is developed in Figure 2 and allows us to mathematically model the effects of critical parameters. For example, if an application consists of amplifying continuous waveforms, then this model allows us to determine gain-accuracy, stability, impedances, frequency response and output swing for a particular load requirement.

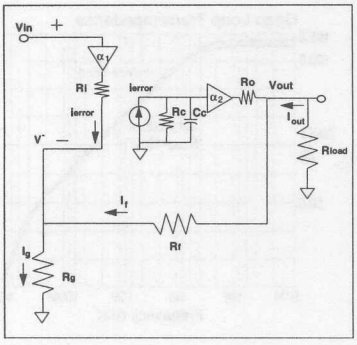


Figure 2 Practical Model

Mathematical Justification

Our first task is to derive a transfer function by nodal analysis for an infinite load condition.

$$I_{error} = I_g - I_f$$

$$I_{error} = \frac{V^-}{R_g} - \frac{V_{out} - V^-}{R_f}$$

$$V_{out} = I_{error}(\alpha_2 \cdot Z(s)) - I_f \cdot R_o$$

$$V^- = \alpha_1 \cdot V_{in} - I_{error} \cdot Ri$$

Equation 1

After combining and eliminating the terms V- and Ierror in Equation 1, a transfer function is derived by dividing Vout by Vin as seen in Equation 2.

$$\frac{V_{out}}{V_{in}} = \frac{\alpha_1 \cdot A_v\left(1 + \frac{R_o}{A_v \cdot \alpha_2 \cdot Z(s)}\right)}{1 + \frac{R_f + R_i \cdot A_v + R_o\left(1 + \frac{R_i}{R_g}\right)}{\alpha_2 \cdot Z(s)}}$$

$$A_v = 1 + \frac{R_f}{Rg}$$

Equation 2

The Z(s) in Equation 2 is the open-loop transimpedance gain and its value is derived by dividing the output voltage Vout by the current through Vin, shown in the schematic of Figure 3. The terms "α_1 and α_2" are the buffer gains while Ro is the open loop output resistance.

Although this equation has many variables, most of the terms are reduced by the open-loop response Z(s). The gain bandwidth independance for CFA is still true when Z(s) approaches infinity and the gain Av remains small. The denominator term, "Ri" is multiplied by closed-loop gain Av, and is small with a range of 16 to 490Ω for current feedback amplifiers. For a CLC406 Ri is 60Ω. The series output resistance Ro in the denominator is scaled by the ratio of the Ri and gain setting resistor Rg. While the Ro in the numerator is divided by the gain Av, α_2, and Z(s). Typically, the open-loop Ro will vary from 5 to 25 ohms.

The closed-loop output resistance approaches zero at dc, and is a function of the open-loop Z(s) frequency response. This is an important point when matching an output impedance by a back matching resistor. Typically back matching consists of placing a resistor that matches the characteristic impedance of a coaxial cable or specific devices input impedance, such as 50 ohms.

The denominator term:

$$\frac{\alpha_2 \cdot Z(s)}{R_f + R_i \cdot A_v + R_o\left(1 + \frac{R_i}{R_g}\right)}$$

is referred to as the loop gain, and its closed-loop bandwidth is determined by denominator:

$$R_f + R_i \cdot A_v + R_o\left(1 + \frac{R_i}{R_g}\right)$$

As you increase gain Av, you need to decrease Rf to maintain the largest possible -3dB bandwidth. Manufacturers of CFA amplifiers specify a gain of 1 or 2 at a recommended Rf in the data sheet. For large gain changes the designer can select a value that best fits the desired new closed-loop gain Av. This maximizes the bandwidth and maintains the same stability based upon maintaining the same ratio used to select

the original Rf in the datasheet. For small changes in gain, using the recommended Rf while changing the gain by Rg is acceptable unless stability becomes an issue.

As Rf decreases, a fundamental limit is reached by the approximate parallel combination of Rload and Rf. At this new load, the output voltage limit is set by the output current capability or the maximum output voltage swing into a no load condition. An alternative is to increase Rload or increase Rf. A bandwidth reduction in the ratio of the open-loop to closed-loop will result. This ratio decrease results in secondary effects such as a decrease in distortion, noise, gain accuracy, etc. Therefore, small changes are acceptable and large ratio changes are not recommended.

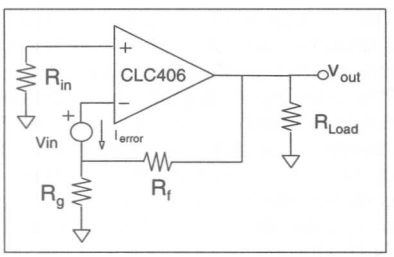


Figure 3 Simulation Method

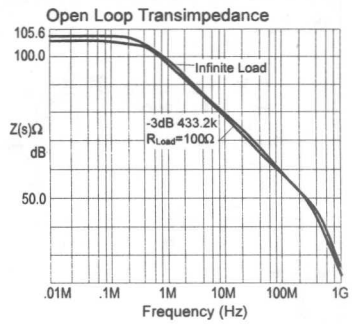
Open Loop Transimpedance Plot

At first it may seem strange to determine Z(s) by placing the voltage source in the inverting node of Figure 3. But this simplifies the simulation steps and has advantages for deriving the stability plot for investigating loads at the output pin.

The circuit in Figure 3 simulates the open-loop transimpedance response Plot 1, while looking at 2 conditions:

1. Infinite load.
2. 100Ω load.

This plot helps explain the accuracy of our spice model and its effects for a practical application. Later this transimpedance gain Z(s) is normalized to an open-loop magnitude function.



Plot 1 Open Loop Transimpedance

The open loop transimpedance gain Plot 1 has axis in dB ohms versus frequency, and shows an approximate first order roll off function $Z(s) = \frac{R_c}{sR_cC_c + 1}$ that includes secondary poles at the higher frequencies. To derive the value of Rc you take the inverse log of the axis:

$$10^{Z(s)/20}$$

at low frequencies while the 3dB bandwidth gives Cc by the following:

$$\frac{1}{2\pi R_c f_{-3dB}}$$

Equation 3:

$$T(s) = \frac{Z(s) \cdot A_v}{R_f + R_i \cdot A_v}$$

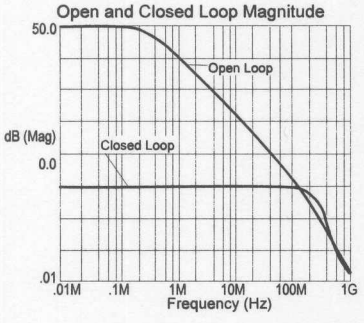
where Z(s) is:

$$\frac{V_{out}}{I(V_{in})}$$

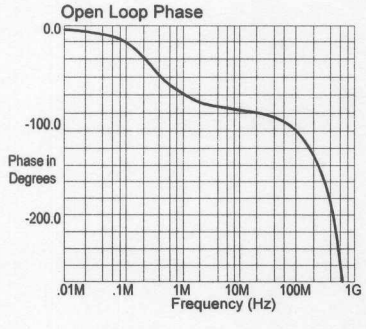
and I is the current in Vin.

If we plot this transfer function for a CLC406 at an Av=1 with an Rf=768Ω and Rg=∞, the magnitude and phase information is shown in Plot 2 and 3. The output Ro term is ignored since Ri is low. The gain and phase margin is now available for determining the stability of our CLC406 Current Feedback Amplifier.

With Plot 2, you find the unity gain crossover frequency point. This frequency point determines the phase of the amplifier on Plot 3 and it is subtracted from a 180° to derive the Phase Margin. The value at zero dB is at a frequency of 108MHz and infers a phase margin of 62°. The gain margin is measured from the -180° phase point and is the difference between the open-loop gain intersection and the 0dB gain line in Plot 2, which is approximately 12dB. From control theory, these values are the indicators for optimum amplifier performance, although many designers will set the phase margin to 45° and 9dB of gain margin. This results in 3dB of frequency peaking or in the time domain signal preshoot and undershoot. Yet, we will still have a difference in the unity gain -3dB frequency response of 220MHz in simulation versus 200MHz in an actual part. The explanation for the difference will be explained later.



Plot 2 Open and Closed Loop Magnitude



Plot 3 Open Loop Phase

Including Z(s)

The transfer function derived in Equation 2 has little meaning when looking at the poles and zeros for the amplifier without including transimpedance gain Z(s). At first let's substitute the first order pole of Z(s) into Equation 2. After some mathematical manipulation we discover a pole plus a zero as shown in Equation 3. This is not intuitively obvious until you think about the amplifier's independent and dependent source and the inclusion of Ro to produce this zero.

$$\frac{V_{out}}{V_{in}} = \frac{\alpha_1 \cdot A_v\left(1+\frac{R_o}{A_v \cdot R_c}\right)}{1+\frac{R_t}{R_c}} \cdot \frac{1+s\left(\frac{R_o \cdot C_c}{A_v}\right)}{1+s\left(R_t \| R_c \cdot C_c\right)}$$

Equation 3

Where the term:

$$R_t \cong R_f + A_v \cdot R_i + \left(1+\frac{R_i}{R_g}\right) \cdot R_o,$$

$s=j\omega$, and $\omega=2\pi f$.

At s=0 the open-loop Rc reduces the terms in Equation 3 to the gain Av times a_1. The zero in the numerator is an order of magnitude higher than the pole in denominator, while the pole has a new value of Rt times Cc where Rc >> Rt. Yet, we have not considered the effects of "Parasites" and their influences upon the stability of the amplifier.

External Parasites and Complex Loads

Connecting multiple circuits that have complex values (capacitance or inductance) at the nodes often results in stability issues for all types of amplifiers. Recall the bandwidth of the CLC406 model indicated its -3dB bandwidth to be higher than the measured unity-gain frequency. This increase bandwidth is largely the result of parasitic components of the package and evaluation board layout[1]. This adds additional zeros and poles to the equation that peaks the frequency response. Adding

complex loads to various pins of our model causes stability questions that are probably more easily answered through simulation analysis rather than mathematical analysis.

If a capacitance is in parallel with the load resistance, a decrease in phase margin will result. Capacitance in parallel with Rg decreases the loop gain, while capacitance in parallel with Rf increases the loop gain. All of these effects are seen in simulations for an amplifier.

A common designed circuit is a transimpedance amplifier. The circuit in Figure 4 shows replacing the Rg resistor with the equivalent photo-diode capacitance to simulate closed-loop stability for the CFA. Using the earilier spice simulation method to generate a Bode plot that determines the stability of the design. Adding an independent current source in parallel with the diode capacitance provides a method to simulate the transimpedance gain versus frequency.

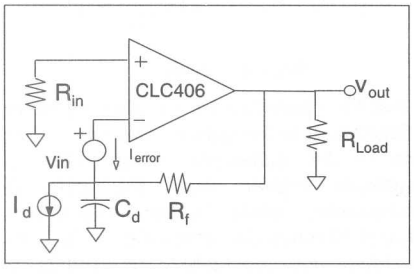


Figure 4 Photo Diode Analysis

Summary

Models are available from Comlinear Corporation for modeling many of the important parameters for high speed op amps. Application note OA-18 "Simulation SPICE Models For Comlinear's Op Amps", details the schematics and parameters that are modeled. Ask for Comlinear's latest spice model diskette.[2]

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[1] R. Schmid, "Technique targets board parasites.", EDN April 14, 1994 page 147.

Spice Models
Contents

10

Application Note OA-18

Simulation SPICE Models for Comlinear's Op Amps

Rea Schmid and Kumen Blake

MMD.05

This application note is updated as new products are released. Please check with Comlinear for the latest revision.

10

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OA-18 July 1994

Comlinear Corporation is a manufacturer and supplier of high-performance analog signal processing components. Comlinear's broad signal conditioning product line includes high-speed hybrid and monolithic operational amplifiers, buffers, video amplifiers, multiplexers, automatic gain control integrated circuits, track/hold amplifiers, and analog-to-digital converters. Comlinear continues as a leader in developing products offering exceptional performance, speed, quality, reliability and service.

INTRODUCTION

This diskette is a collection of PSpice compatible models for Comlinear amplifiers. For additional information about SPICE Models supporting existing or new products, Comlinear customers can contact Comlinear Corporation directly at 1-800-776-0500. The SPICE Models found on this disk are created for use on an IBM compatible computer using analysis programs that accept Spice formats. Comlinear assumes no responsibility for designs created from these SPICE Models. These SPICE Model files model typical performance at room temperature. Before designs are released to production, Comlinear suggests that topologies be verified by prototyping the circuit. The part-to-part and over-temperature performance variations of Comlinear amplifiers are specified in current data sheets (see Reference 1). The changes from the last SPICE Model diskette version are listed in this table:

TABLE I. UPDATES TO SPICE MODEL DISKETTE

CLC109.CIR A new SPICE Model.
CLC111.CIR A new SPICE Model.
CLC402.CIR An updated version that gives better noise, dc bias, and CMRR performance.
CLC426.CIR A new SPICE Model.
CLC428.CIR A new SPICE Model.
CLC431.CIR A new SPICE Model.
CLC432.CIR A new SPICE Model.
CLC502.CIR An updated version that gives better noise, dc bias, and CMRR performance.

TABLE II. SPICE MODEL SUBCIRCUIT FILES ON THIS DISKETTE

File Name Description

CLC109.CIR A Low-Power, Wideband, Closed-Loop Buffer.
CLC111.CIR A Very Wideband, Ultra-High Slew Rate, Closed-Loop Buffer.
CLC400.CIR A Wideband, Low-Gain Monolithic Current Feedback Op Amp with Fast Settling,(.05% in 12 ns), Low Power and an Input Offset Adjustment Pin.
CLC401.CIR A Wideband, High-Gain Monolithic Current Feedback Op Amp with Fast Settling (.01% in 10 ns) and Low Power.
CLC402.CIR A Low-Gain Monolithic Current Feedback Op Amp with Fast 14-bit Settling (.0025% in 25 ns) and Low Power.
CLC404.CIR A Wideband Monolithic Current Feedback Op Amp with High Slew Rate.
CLC406.CIR A Wideband Low-Cost, Low-Power Monolithic Current Feedback Op Amp.
CLC409.CIR A Very Wideband, Low Distortion Monolithic Current Feedback Op Amp.
CLC410.CIR A Video Monolithic Current Feedback Op Amp with disable, Fast Settling (0.05% in 12 ns) and an Input Offset Adjust Pin.
CLC414.CIR A Quad, Low-Power Monolithic Current-Feedback Op Amp.
CLC415.CIR A Quad Wideband Monolithic Current Feedback Op Amp.
CLC420.CIR A High-Speed, Unity Gain Stable Monolithic Voltage Feedback Op Amp.
CLC425.CIR An Ultra Low-Noise, Wideband Monolithic Voltage Feedback Op Amp with Current Supply Adjust.
CLC426.CIR An Ultra Low-Noise, Wideband Monolithic Voltage Feedback Op Amp with Current Supply Adjust and External Compensation.
CLC428.CIR An Ultra Low-Noise, Wideband, Dual Monolithic Voltage Feedback Op Amp
CLC430.CIR A Wideband Monolithic Current Feedback Op Amp with disable and +/-5V to +/-15V supply capability.
CLC431.CIR A Dual, Wideband Monolithic Current Feedback Op Amp with high slew rate.
CLC432.CIR A Dual, Wideband Monolithic Current Feedback Op Amp with disable and +/-5V to +/-15V supply capability.
CLC501.CIR A High-Speed Output Clamping Monolithic Current Feedback Op Amp for high gains.
CLC502.CIR A High-Speed Output Clamping Monolithic Current Feedback Op Amp with Fast 14-bit Settling (0.0025% in 25 ns) for low gain.
CLC505.CIR A High-Speed, Programmable-Supply Current, Monolithic Current Feedback Op Amp.
CLC520.CIR A Monolithic Amplifier with Voltage Controlled Gain (AGC).
CLC522.CIR A Monolithic Wideband Variable Gain Amplifier.
CLC532.CIR A High-Speed, 2:1 Analog Multiplexer with fast 12-bit settling (0.01% in 17 ns), low noise, low distortion and adjustable noise bandwidth.

SPICE Models are found in the root directory of the data disk supplied.

START UP INSTRUCTIONS

Make a backup copy of the SPICE files contained on this disk to another floppy. Copy all SPICE Model files of interest to a library on the hard disk. If the library directory is not in the SPICE program's path, the user should set that path in the autoexec.bat for easier excess. The .INC statement in PSpice should be used in the simulation file to include the SPICE Models subcircuit.

Example" .INC CLC400.CIR"

AMPLIFIER SPICE MODELS

These SPICE Model files are written in ASCII file format for IBM-compatible PC's. They are compatible with PSpice and other Spice 2G simulators. For additional detailed information about using PSpice please contact MicroSim

(See Reference 2). Comlinear amplifier SPICE Models are written in a subcircuit format for easy incorporation into larger circuits. A listing of any amplifier subcircuit may be obtained by printing its CLC*.CIR file to a local printer. The subcircuit node assignments match the device pin-outs as shown in the individual device data sheets. An example is an 8 pin op amp.

```
* Connections: NON-INVERTING INPUT PIN
*    | INVERTING INPUT PIN
*    | | OUTPUT
*    | | | +Vcc
*    | | | | -Vcc
*    | | | | |
.SUBCKT (NAME)   3 2 6 7 4
```

Some schematic capture software packages require a different pin connection order than what Comlinear uses. Changing the pin order in the .SUBCKT statement will not affect the SPICE Model performance.

PERFORMANCE RESULTS

When substitutions of current feedback op amps are made for voltage feedback op amps, results may not be acceptable. Refer to Comlinear's application note OA-13 for a tutorial on current feedback op amp design.

PARAMETERS MODELED

The following typical performance parameters are modeled by the SPICE Models.

DC Effects

* VIO, IBI, IBN
* Supply current vs. Supply voltages
* Common Mode Input/Output Voltage range
* Load current from supplies
* CMRR

AC Effects

* Frequency response vs. gain & load.
* Open loop gain & phase
* Noise
* Small signal Input/Output Impedance

Time Domain

* Rise / fall times
* Slew Rates

Special Features (where applicable)

* Output Clamping
* Supply Current Adjustment
* Offset voltage adjust
* Disable / Enable times
* External Compensation

PARAMETERS NOT MODELED

* Differential gain and phase
* PSRR
* Harmonic distortion
* Fine scale settling performance
* Thermal tail
* Overdrive recovery time (Except for the CLC501 and the CLC502)
* Variation in performance vs. temperature
* Part-to-part performance variation

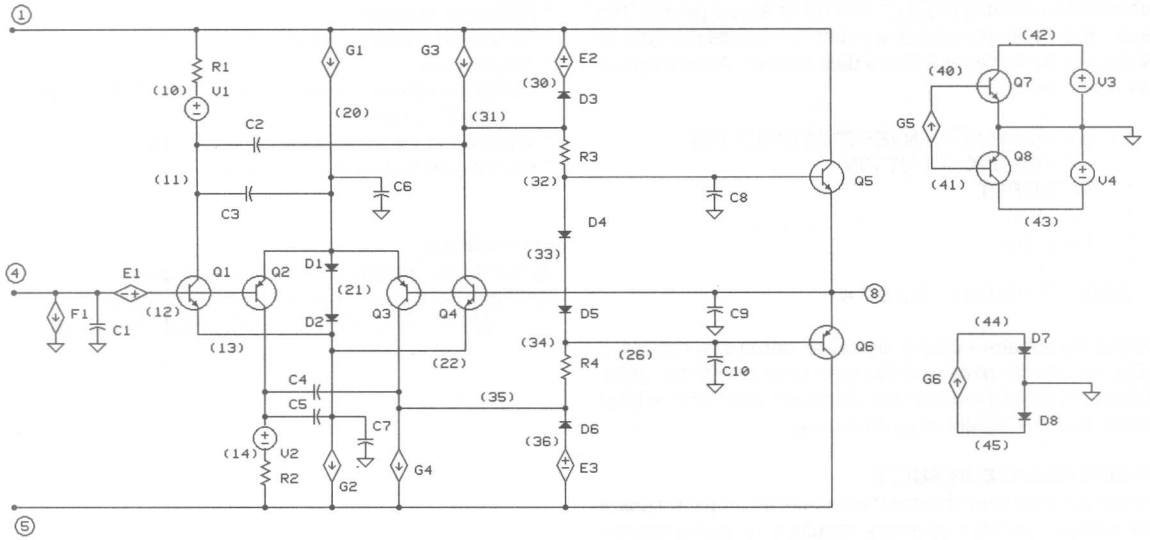
REFERENCES

1) Comlinear Databook of standard products.
2) MicroSim Corporation, 20 Fairbanks, Irvine, CA 92718 USA, (714) 770-3022, (800) 245-3022.

10

NOTICE

CLC109



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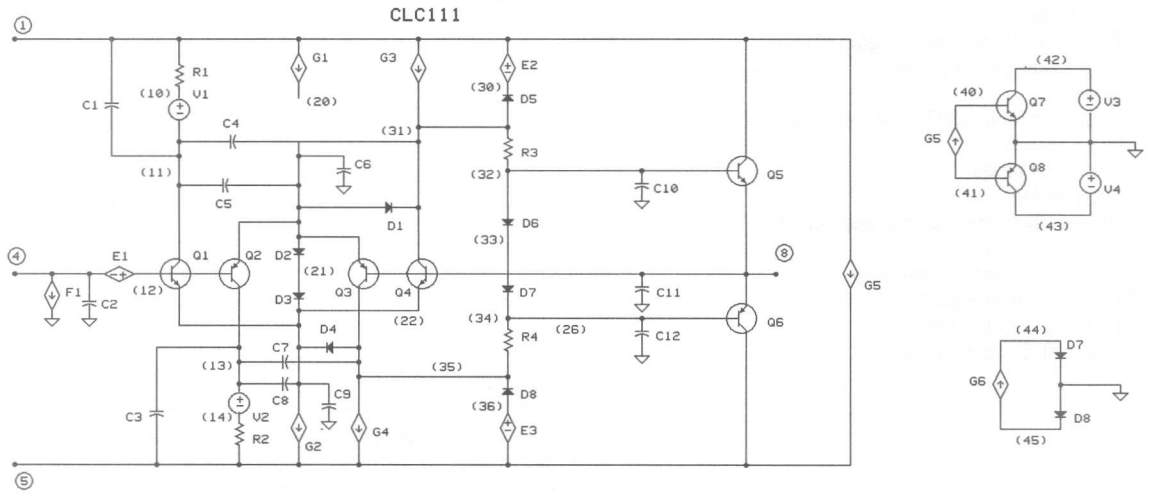
Number in Parenthesis Denotes NODE Number

CLC111



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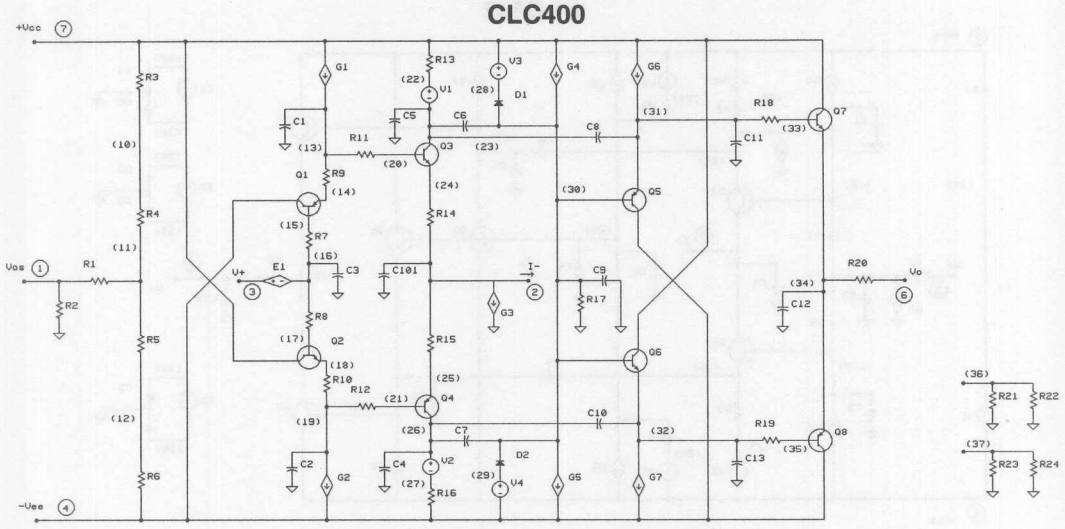

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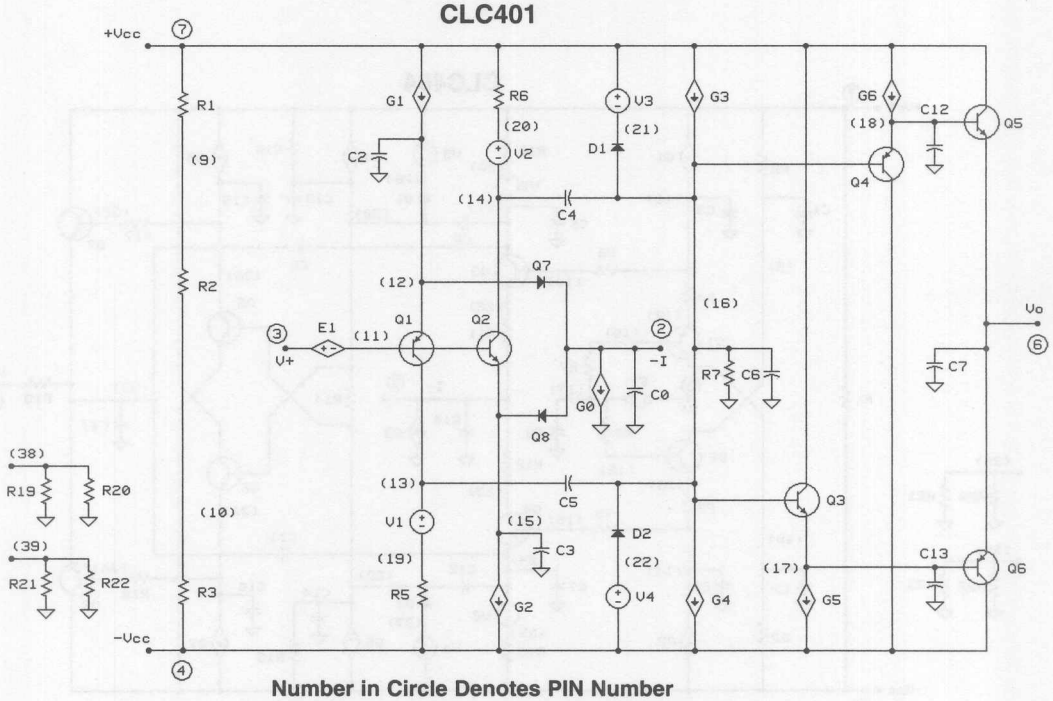

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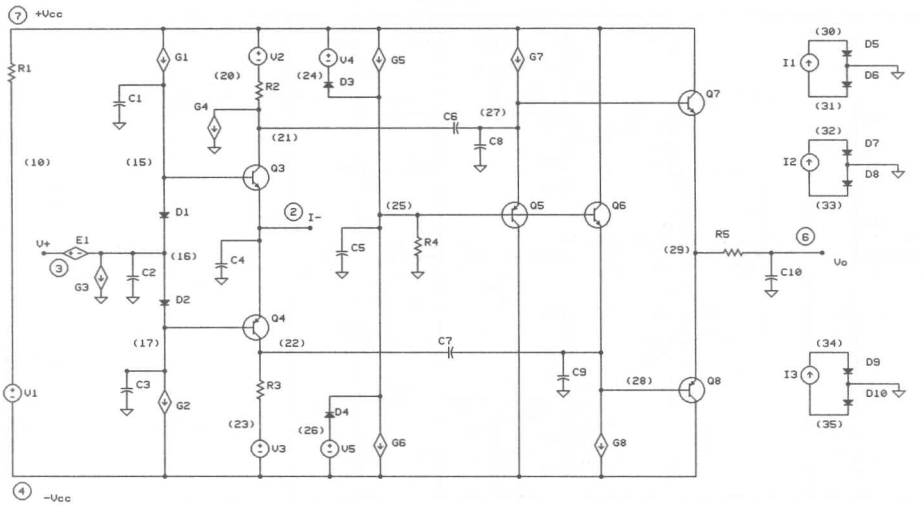

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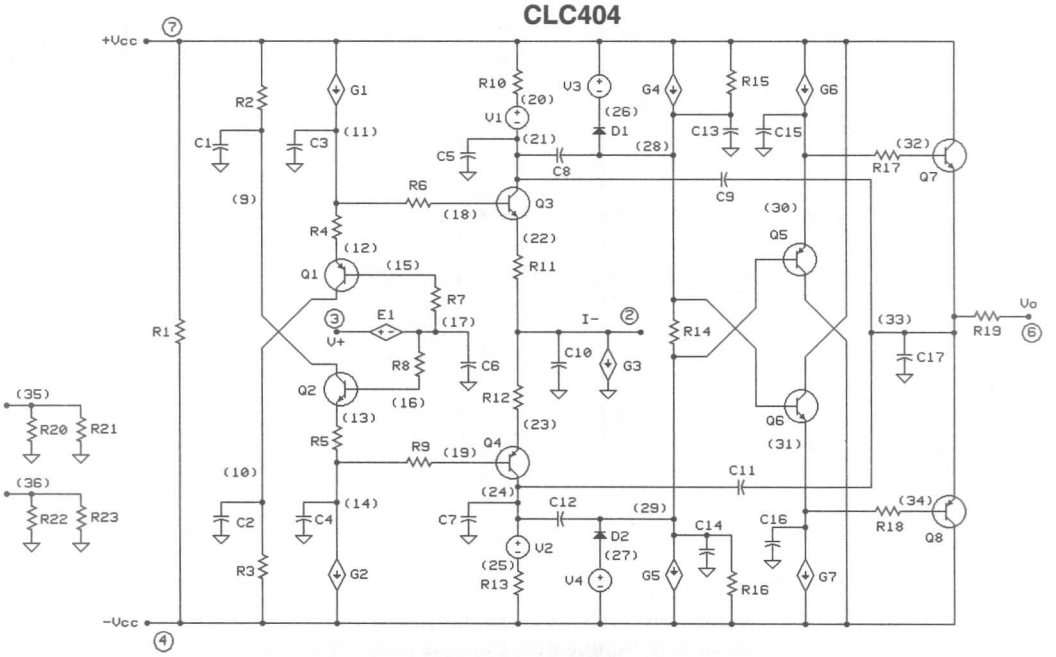

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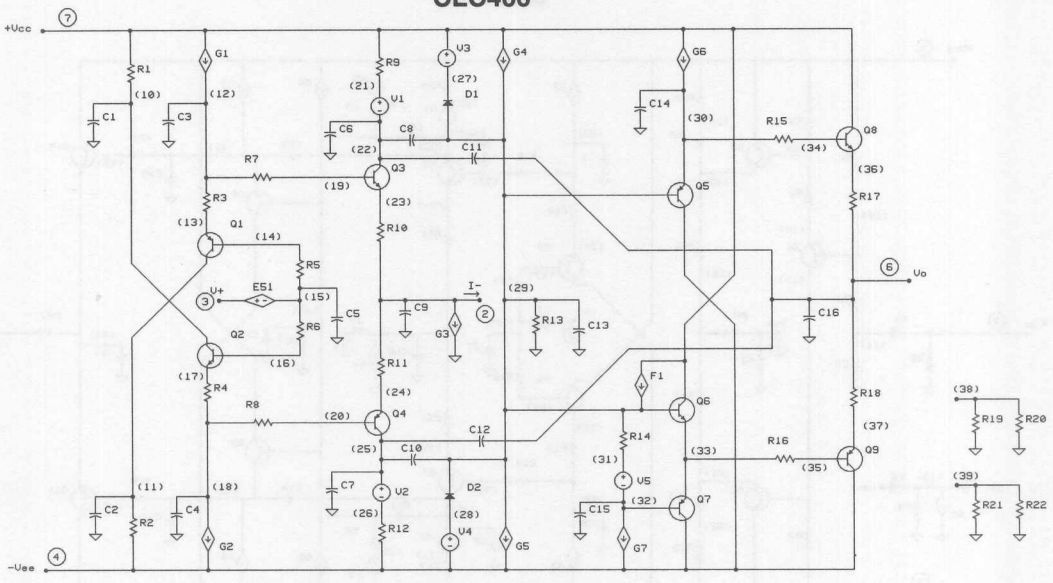

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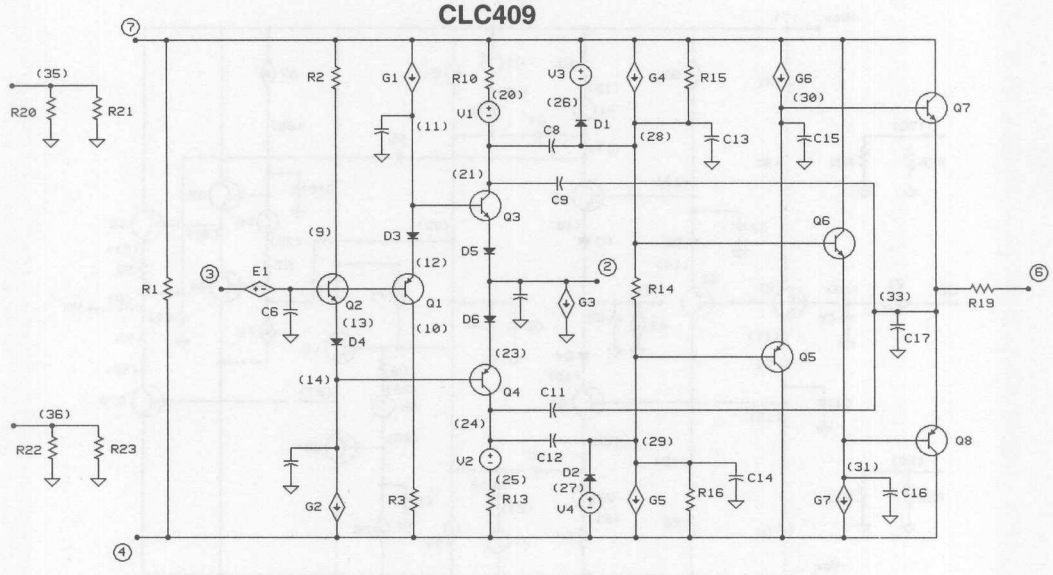

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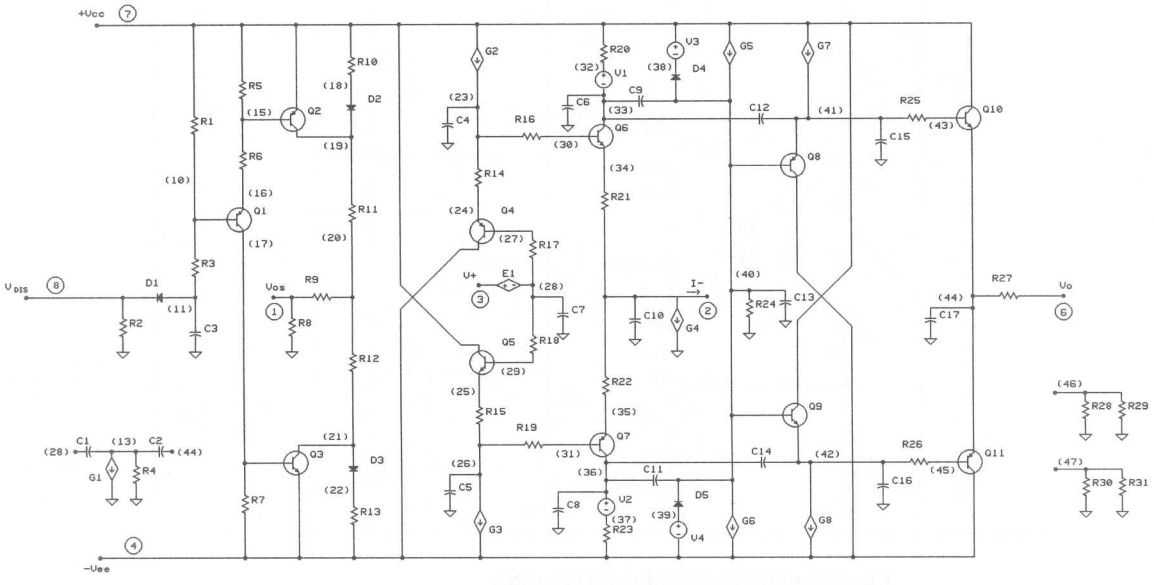

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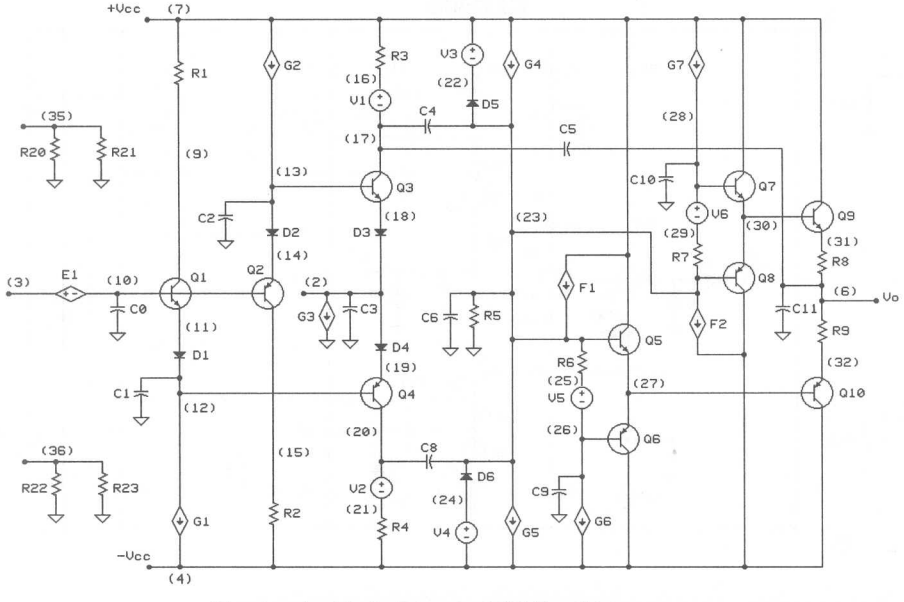

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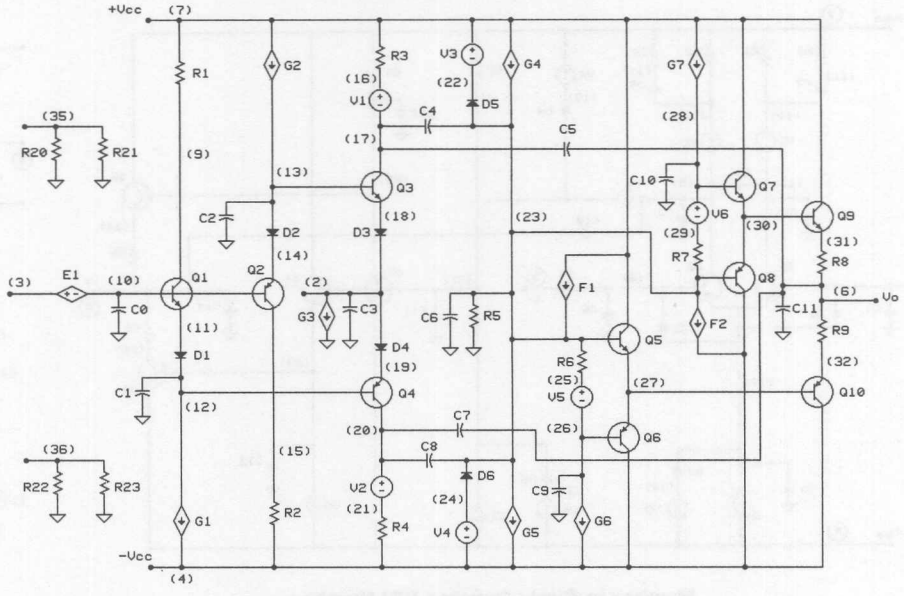

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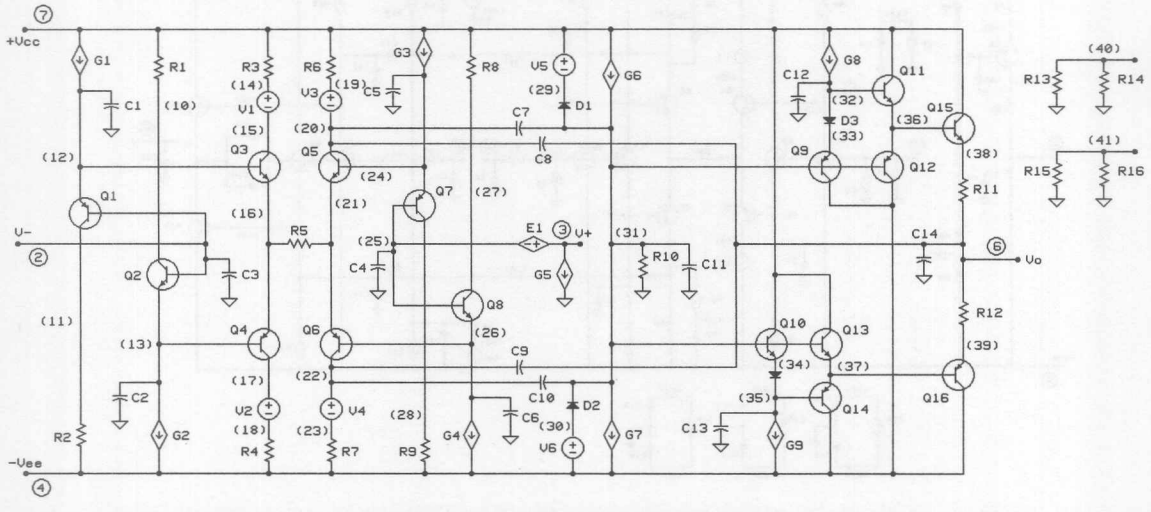

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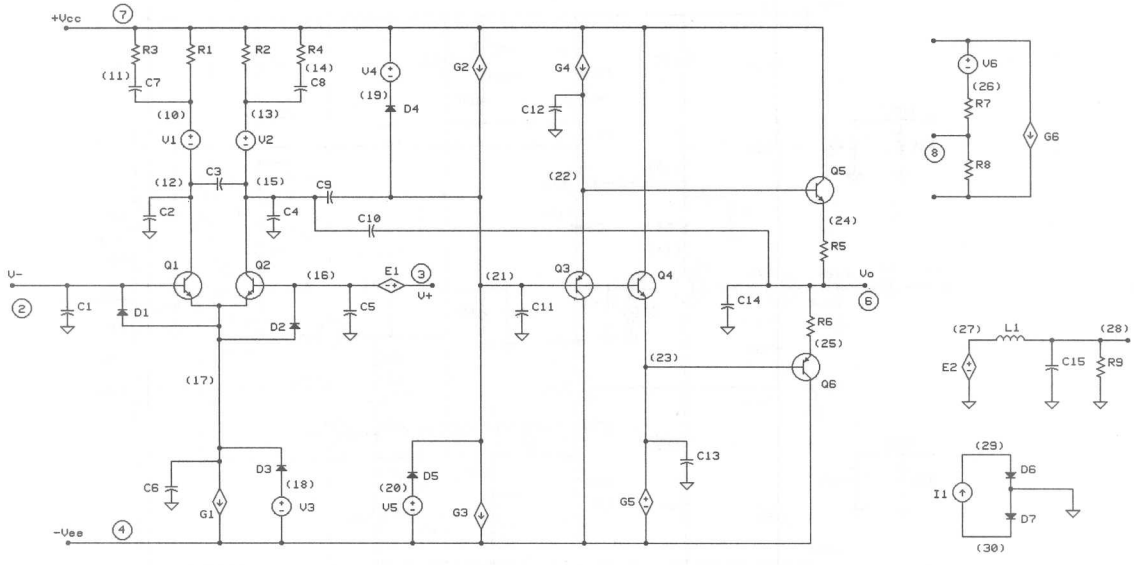

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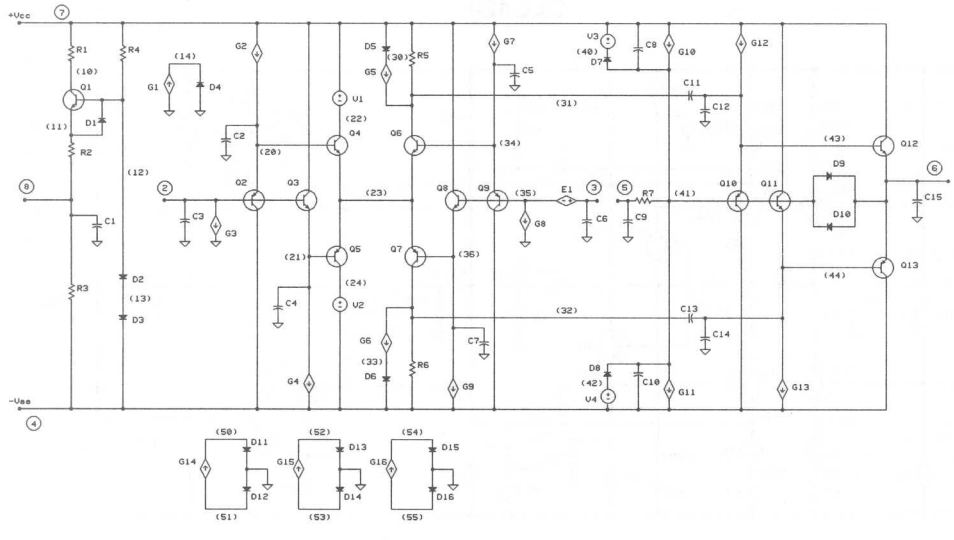

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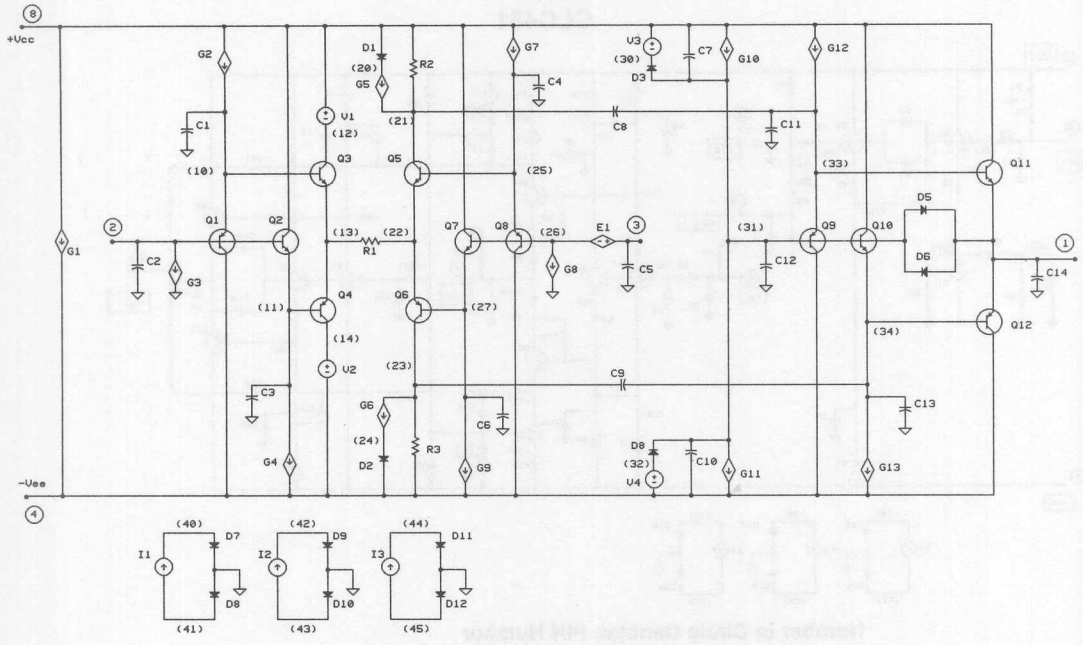

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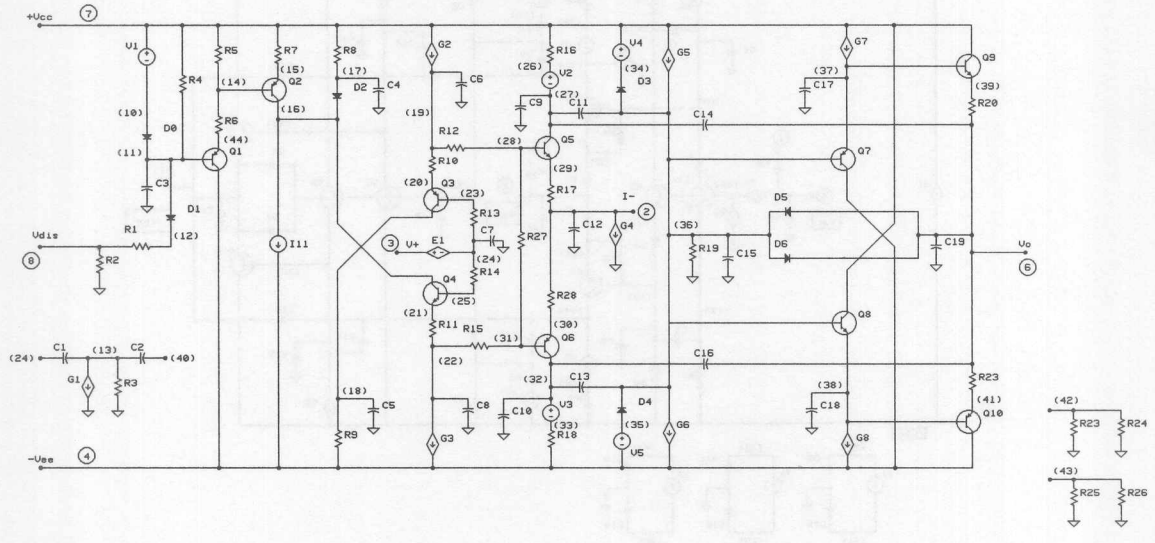

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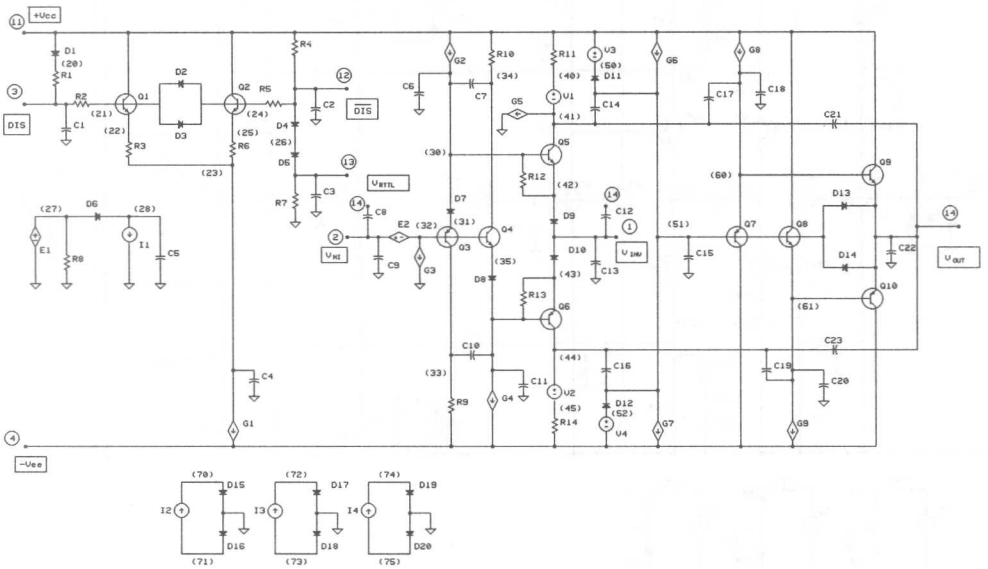

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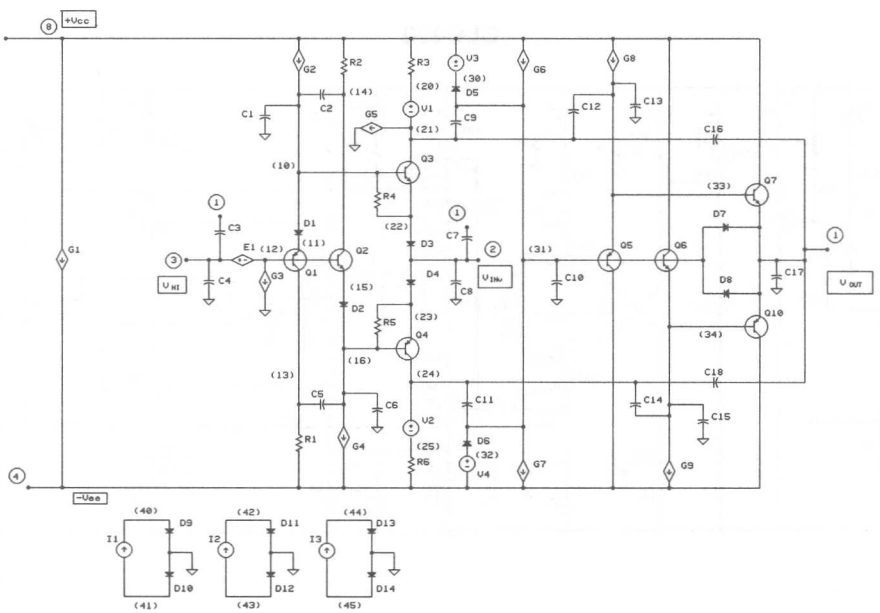

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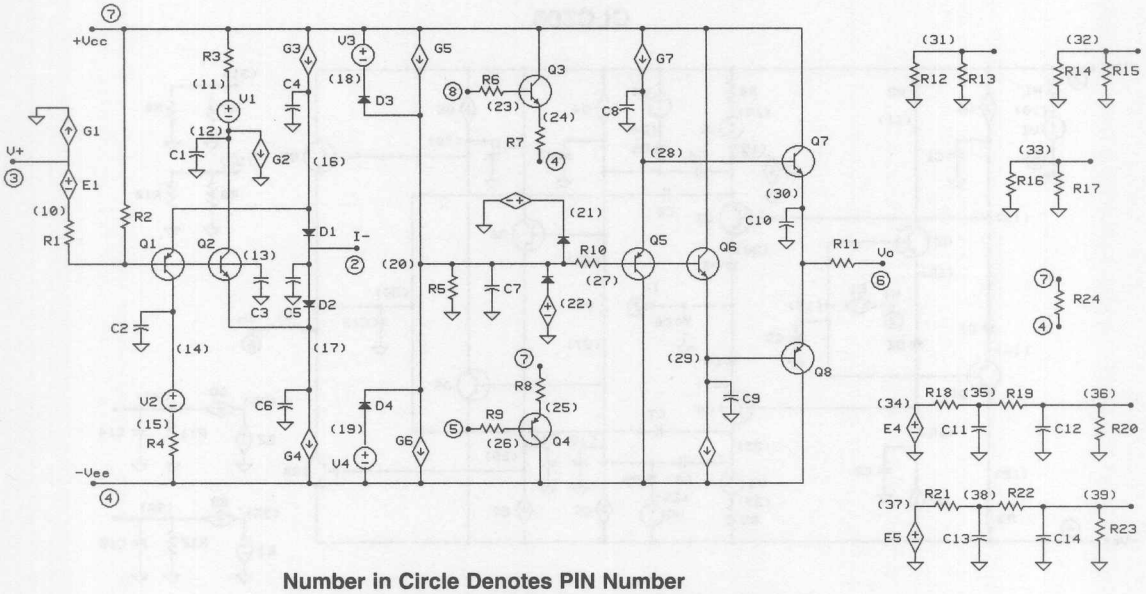
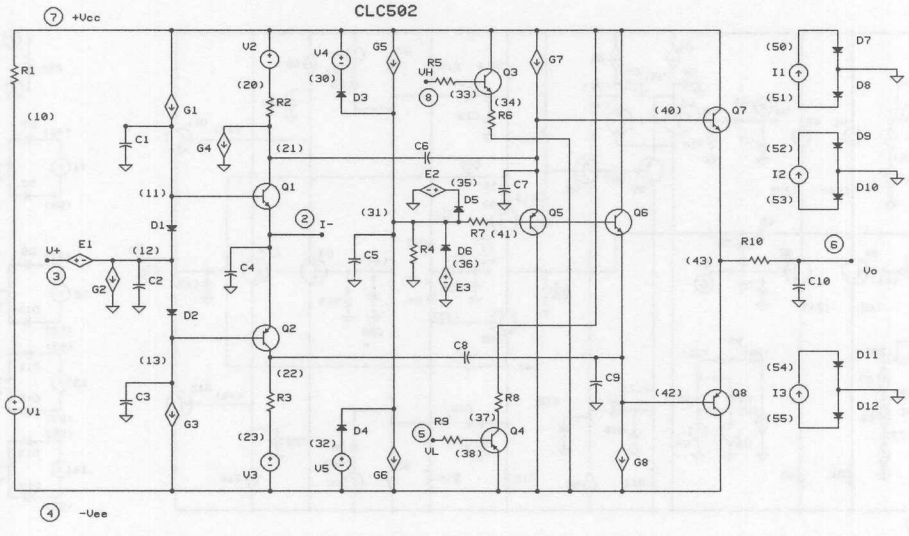
Number in Parenthesis Denotes NODE Number

CLC501



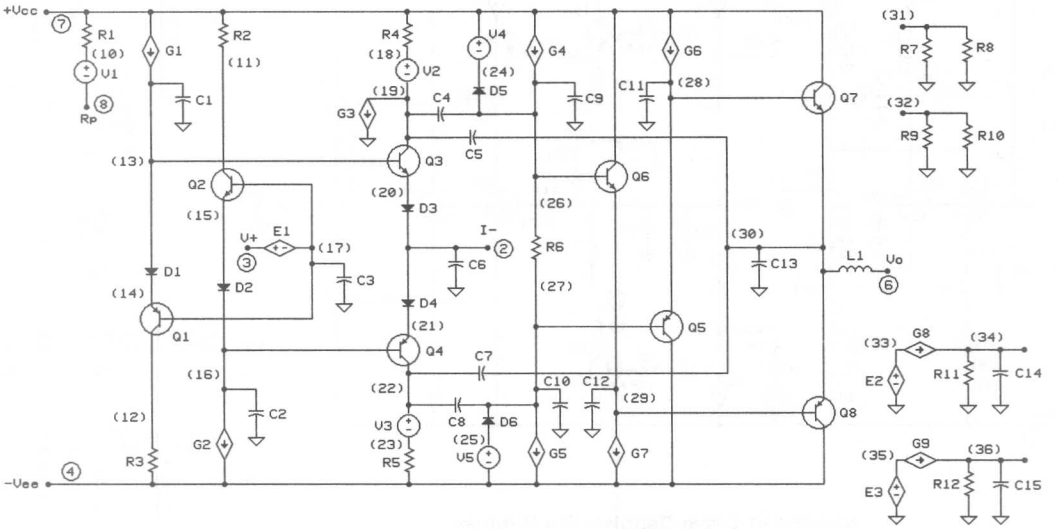
Number in Circle Denotes PIN Number
Number in Parenthesis Denotes NODE Number

CLC502



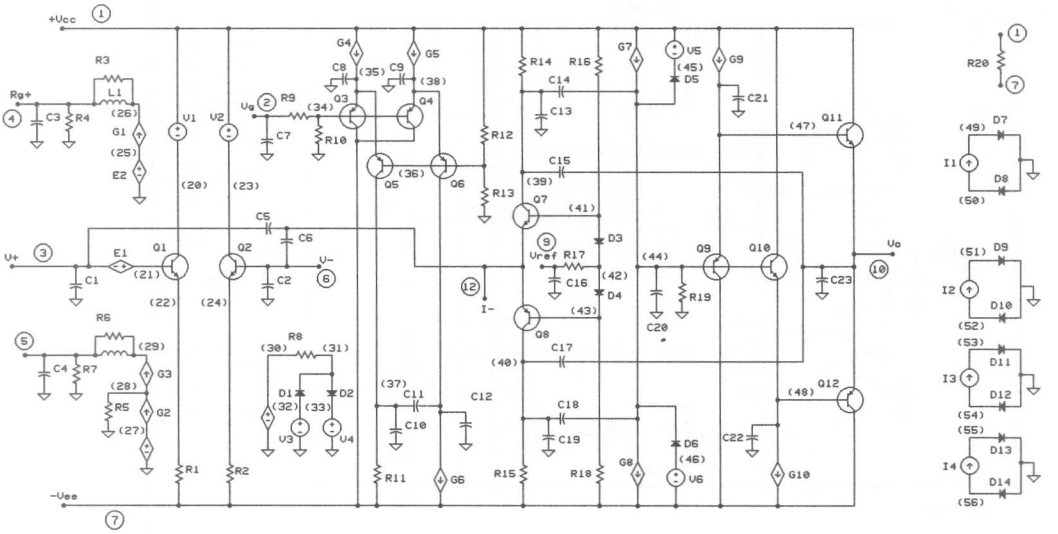
Number in Circle Denotes PIN Number
Number in Parenthesis Denotes NODE Number

CLC505



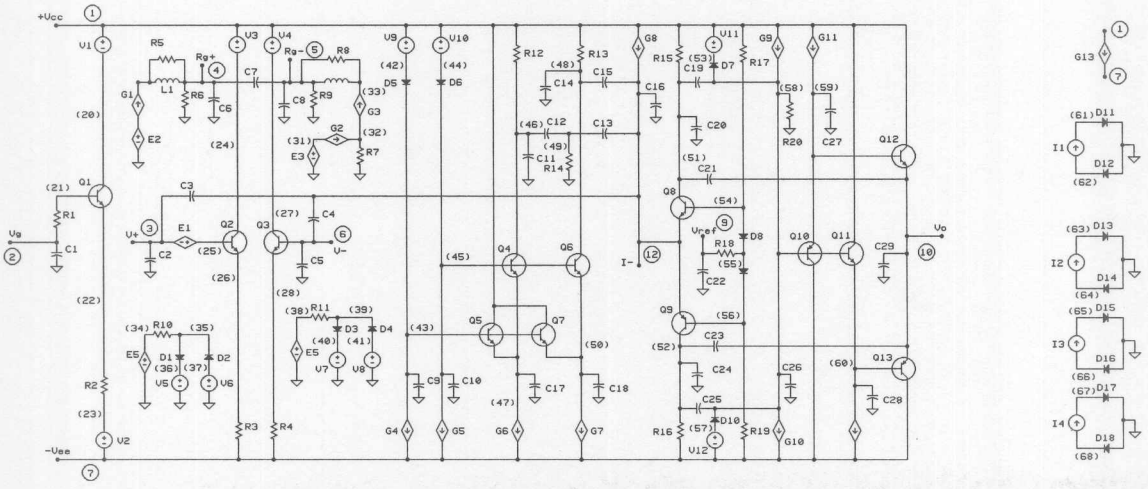
Number in Circle Denotes PIN Number
Number in Parenthesis Denotes NODE Number

CLC520



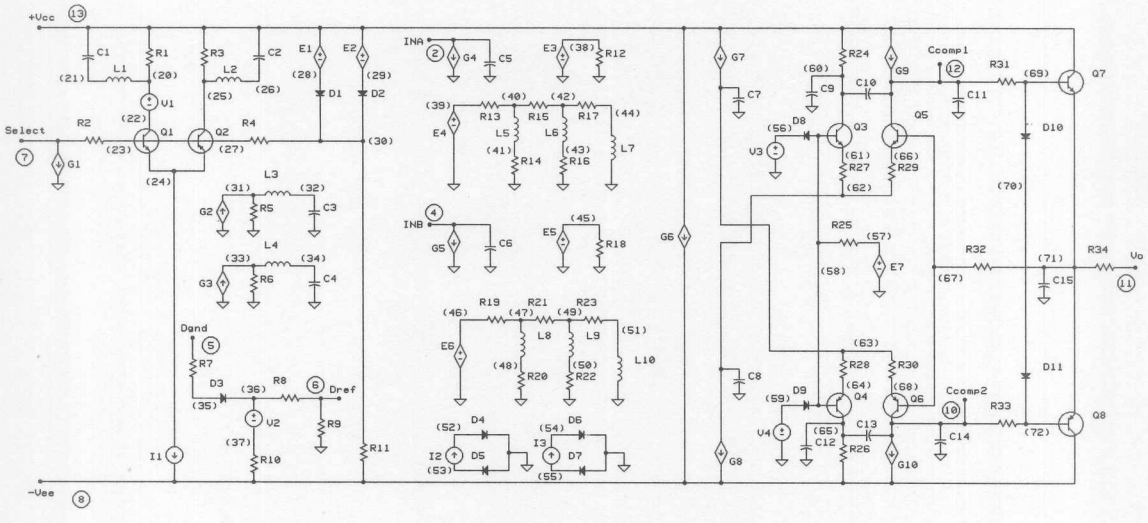
Number in Circle Denotes PIN Number
Number in Parenthesis Denotes NODE Number

CLC522



Number in Circle Denotes PIN Number
Number in Parenthesis Denotes NODE Number

CLC532



Number in Circle Denotes PIN Number
Number in Parenthesis Denotes NODE Number

Packaging and Die Information

Contents

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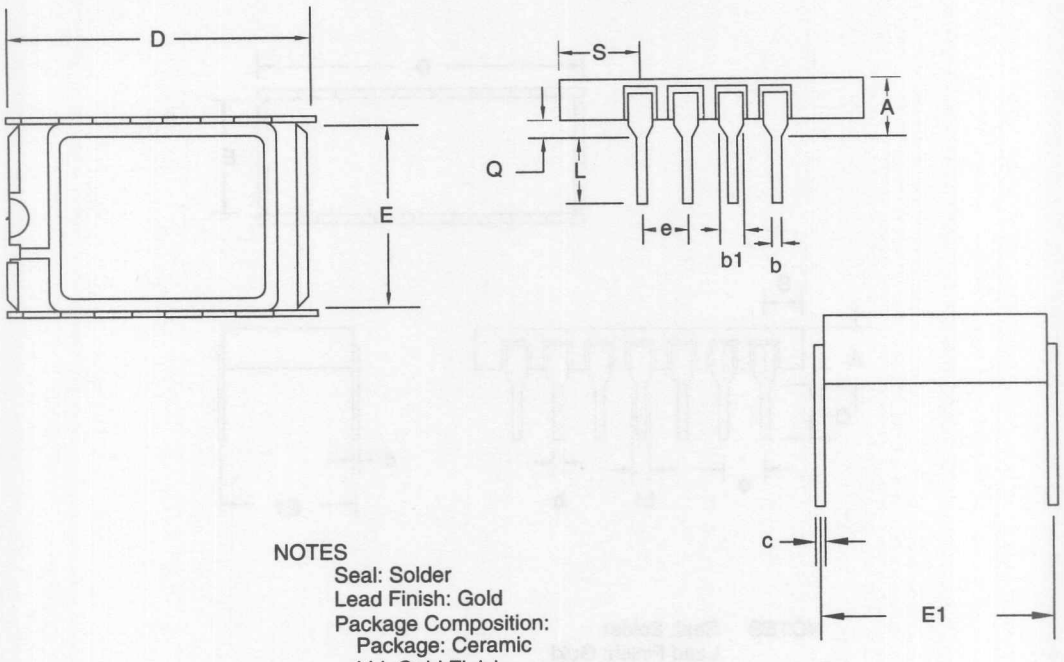
*Where Applicable

8-Pin Side-Brazed Ceramic DIP

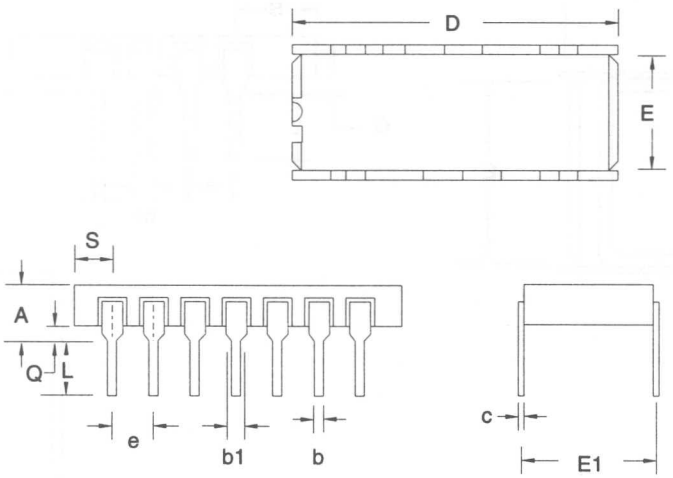


NOTES

Seal: Solder
Lead Finish: Gold
Package Composition:
Package: Ceramic
Lid: Gold Finish
Lead Material: Iron/Nickel Alloy
Die Attach: Eutectic

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A		0.200		5.08
b	0.016	.022	0.41	0.56
b1	0.054 BSC		1.37 BSC	
c	0.009	0.014	0.23	0.36
D	0.386	0.402	9.80	10.21
E	0.282	0.310	7.16	7.87
E1	.290	.320	7.37	8.13
e	0.100 BSC		2.54 BSC	
L	.175 BSC		4.45 BSC	
Q	.025	.045	0.64	1.14
S		.055	.127	

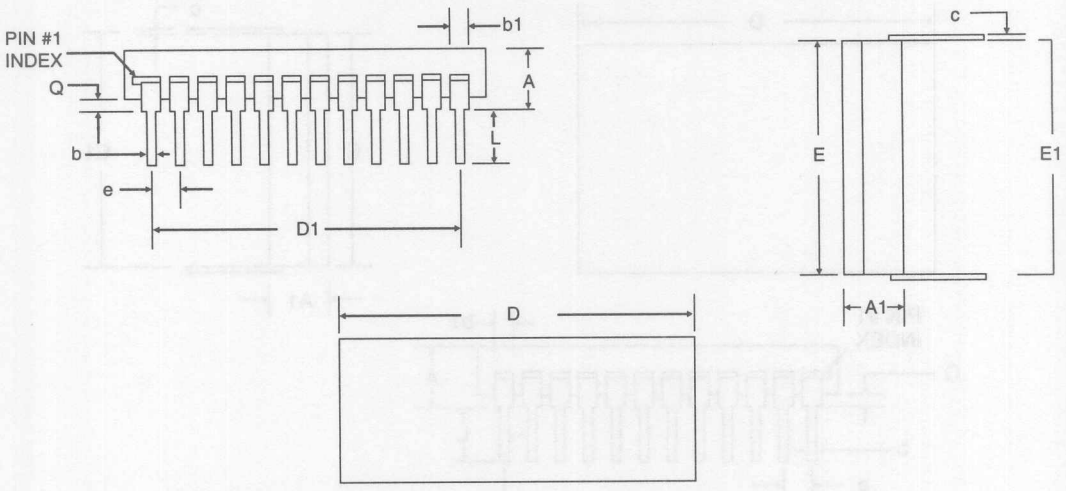
14-Pin Side-Brazed Ceramic DIP



NOTES Seal: Solder
Lead Finish: Gold
Package Composition:
Package: Ceramic
Lid: Gold Finish
Lead Material: Iron/Nickel Alloy
Die Attach: Eutectic

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A		0.200		5.08
b	0.016	0.022	0.41	0.56
b1	0.045	0.065	1.14	1.65
c	0.009	0.012	0.23	0.31
D	0.693	0.710	17.60	18.03
E	0.287	0.308	7.29	7.82
E1	0.290	0.320	7.37	8.13
e	0.100 BSC		2.54 BSC	
L	0.150	0.200	3.81	5.08
Q	0.015	0.045	0.38	1.14
S	0.030	0.060	0.76	1.52

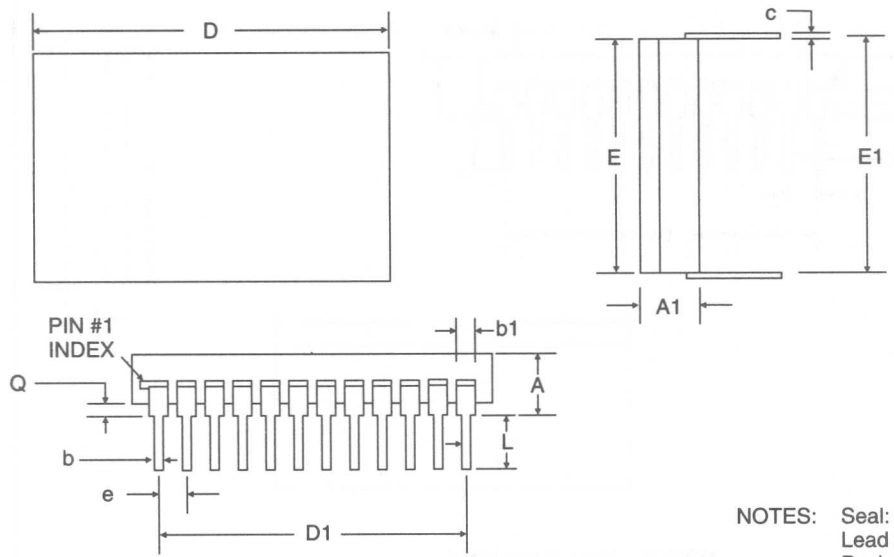
24-Pin 0.6" Side-Brazed Ceramic DIP



NOTES
Seal: Seam Weld
Lead Finish: Gold Finish
Package Composition:
Package: Ceramic
Lid: Kovar/Nickel
Leadframe: Alloy 42
Die Attach: Epoxy

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A		0.225		5.72
A1	0.139	0.192	3.53	4.88
b	0.016	0.020	0.41	0.51
b1	0.050 BSC		1.27 BSC	
c	0.008	0.012	0.20	0.30
D	1.190	1.210	30.23	30.73
D1	1.095	1.105	27.81	28.07
E	0.586	0.602	14.88	15.29
E1	.590	0.610	14.99	15.49
e	0.100 BSC		2.54 BSC	
L	0.165 BSC		4.19 BSC	
Q	0.035	0.065	0.89	1.65

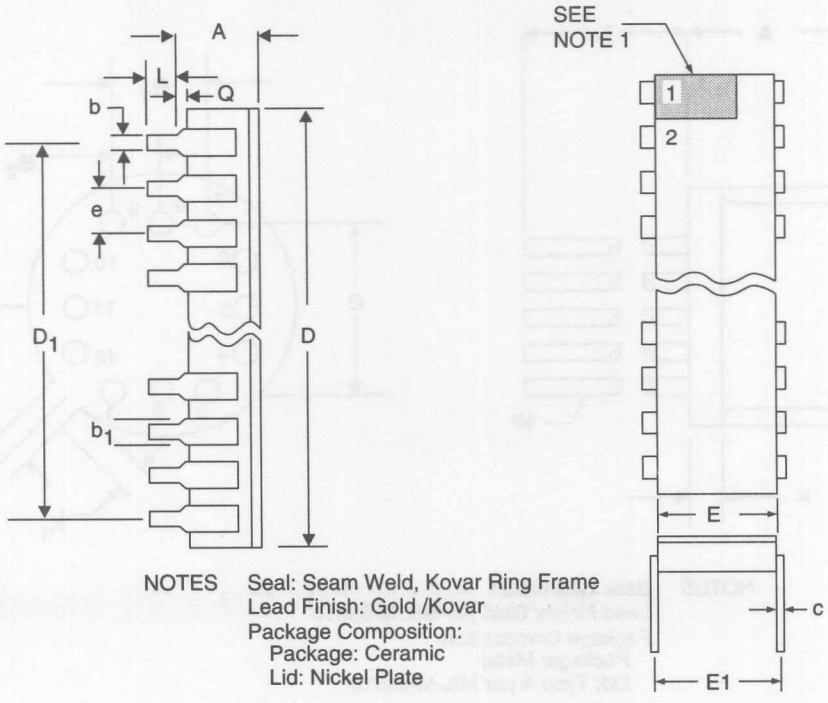
24-Pin 0.8" Side-Brazed Ceramic DIP



NOTES: Seal: Seam Weld
Lead Finish: Gold
Package Composition:
Package: Ceramic
Lid: Kovar/Nickel
Leadframe: Alloy 42
Die Attach: Epoxy

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A-METAL LID	0.180	0.240	4.57	6.10
A-CERAMIC LID	0.195	0.255	4.95	6.48
A1-METAL LID	0.145	0.175	3.68	4.45
A1-CERAMIC LID	0.160	0.190	4.06	4.83
b	0.016	.020	0.41	0.51
b1	0.050 BSC		1.27 BSC	
c	0.008	0.012	0.20	0.30
D	1.275	1.310	32.39	33.27
D1	1.095	1.105	27.81	28.07
E	0.785	0.815	19.94	20.70
E1	0.790	0.810	20.07	20.57
e	0.100 BSC		2.54 BSC	
L	0.165 BSC		4.19 BSC	
Q	0.035	0.065	0.89	1.65

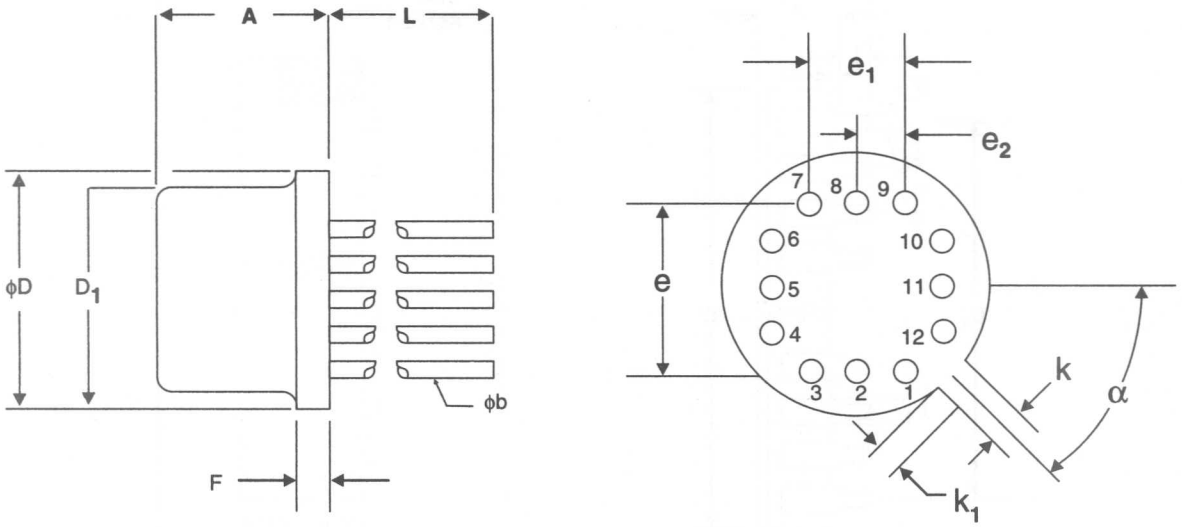
40-Pin Side-Brazed Ceramic DIP



NOTES
Seal: Seam Weld, Kovar Ring Frame
Lead Finish: Gold /Kovar
Package Composition:
Package: Ceramic
Lid: Nickel Plate

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.198	0.252	5.03	6.40
b	0.016	0.020	0.41	0.51
b1	0.050 BSC		1.27 BSC	
c	0.009	0.012	0.23	0.30
D	2.075	2.115	52.71	53.72
D1	1.892	1.908	48.06	48.46
E	1.100 BSC		27.940 BSC	
E1	1.096 BSC		27.84 BSC	
e	0.100 BSC		2.54 BSC	
L	0.175 BSC		4.45 BSC	
Q	0.040	0.060	1.02	1.52

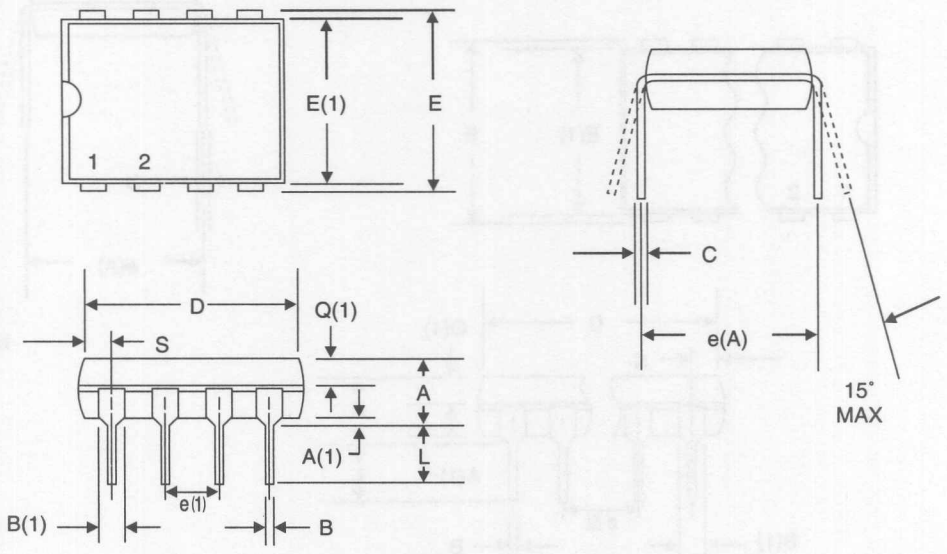
12-Pin TO-8 Metal Can



NOTES Seal: Cap Weld
Lead Finish: Gold per MIL-M-38510
Package Composition:
Package: Metal
Lid: Type A per MIL-M-38510

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.142	0.181	3.61	4.60
ϕb	0.016	0.019	0.41	0.48
ϕD	0.595	0.605	15.11	15.37
ϕD_1	0.543	0.555	13.79	14.10
e	0.400 BSC		10.16 BSC	
e_1	0.200 BSC		5.08 BSC	
e_2	0.100 BSC		2.54 BSC	
F	0.016	0.030	0.41	0.76
k	0.026	0.036	0.66	0.91
k_1	0.026	0.036	0.66	0.91
L	0.310	0.340	7.87	8.64
α	45° BSC		45° BSC	

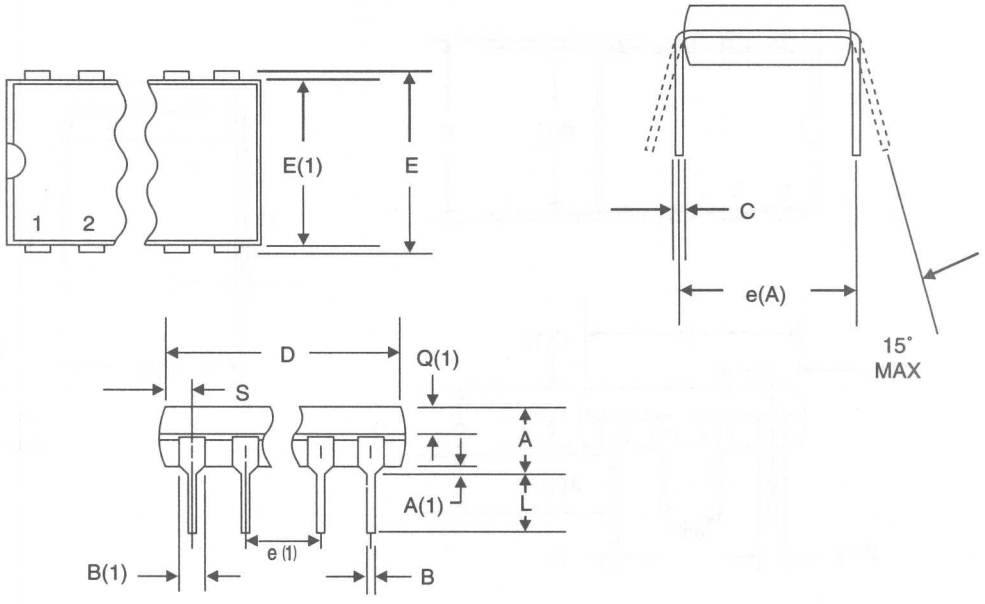
8-Pin Plastic DIP



NOTES Lead Finish: Solder
Package Composition:
Package: Plastic
Lead Frame: Copper/Iron
Die Attach: Epoxy

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.145	0.200	3.68	5.08
A(1)	0.015	0.050	0.38	1.27
B	0.015	0.020	0.38	0.51
B(1)	0.035	0.065	0.89	1.65
C	0.008	0.012	0.20	0.30
D	0.370	0.460	9.40	11.68
E	0.300	0.325	7.62	8.26
E(1)	0.220	0.280	5.59	7.11
e(1)	0.090	0.110	2.29	2.79
e(A)	0.290	0.310	7.37	7.87
L	0.120	0.150	3.05	3.81
Q(1)	0.050	0.080	1.27	2.03
S	0.040	0.080	1.02	2.03

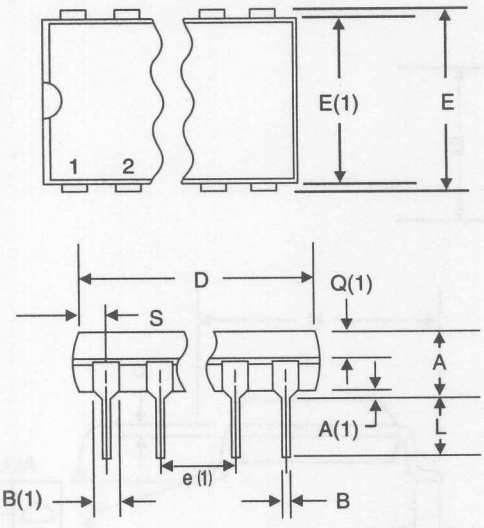
14-Pin Plastic DIP

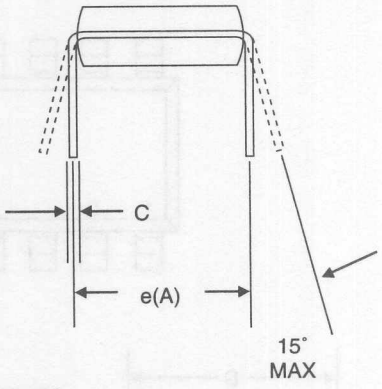


NOTES Lead Finish: Solder
Package Composition:
Package: Plastic
Lead Frame: Copper/Iron
Die Attach: Epoxy

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.145	0.200	3.68	5.08
A(1)	0.015	0.050	0.38	1.27
B	0.015	0.020	0.38	0.51
B(1)	0.035	0.065	0.89	1.65
C	0.008	0.012	0.20	0.30
D	0.680	0.770	17.27	19.56
E	0.300	0.325	7.62	8.26
E(1)	0.220	0.280	5.59	7.11
e(1)	0.090	0.110	2.29	2.79
e(A)	0.290	0.310	7.37	7.87
L	0.120	0.150	3.05	3.81
Q(1)	0.050	0.080	1.27	2.03
S	0.040	0.080	1.02	2.03

16-Pin Plastic DIP

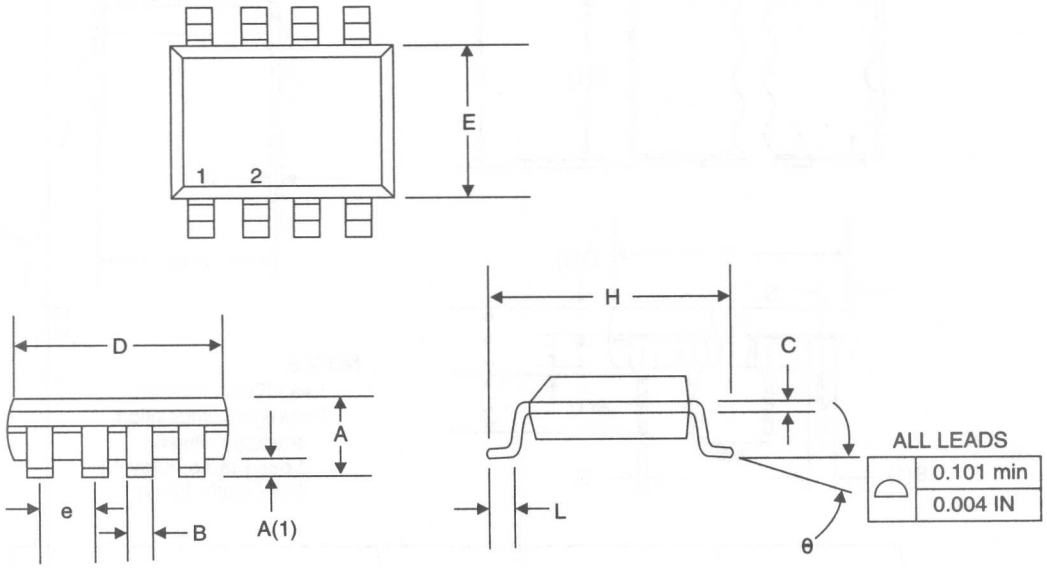




NOTES
Lead Finish: Solder
Package Composition:
Package: Plastic
Lead Frame: Alloy 42
Die Attach: Epoxy

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.125	0.135	3.17	3.43
A(1)	0.015	0.050	0.38	1.27
B	0.015	0.020	0.38	0.51
B(1)	0.040	0.072	1.22	1.83
C	0.011	0.013	0.28	0.33
D	0.745	0.755	18.92	19.18
E	0.300	0.325	7.62	8.26
E(1)	0.220	0.280	5.59	7.11
e(1)	0.080	0.120	2.03	3.05
e(A)	0.290	0.310	7.37	7.87
L	0.125	0.150	3.18	3.81
Q(1)	0.060	0.070	1.52	1.78
S	0.015	0.060	0.38	1.52

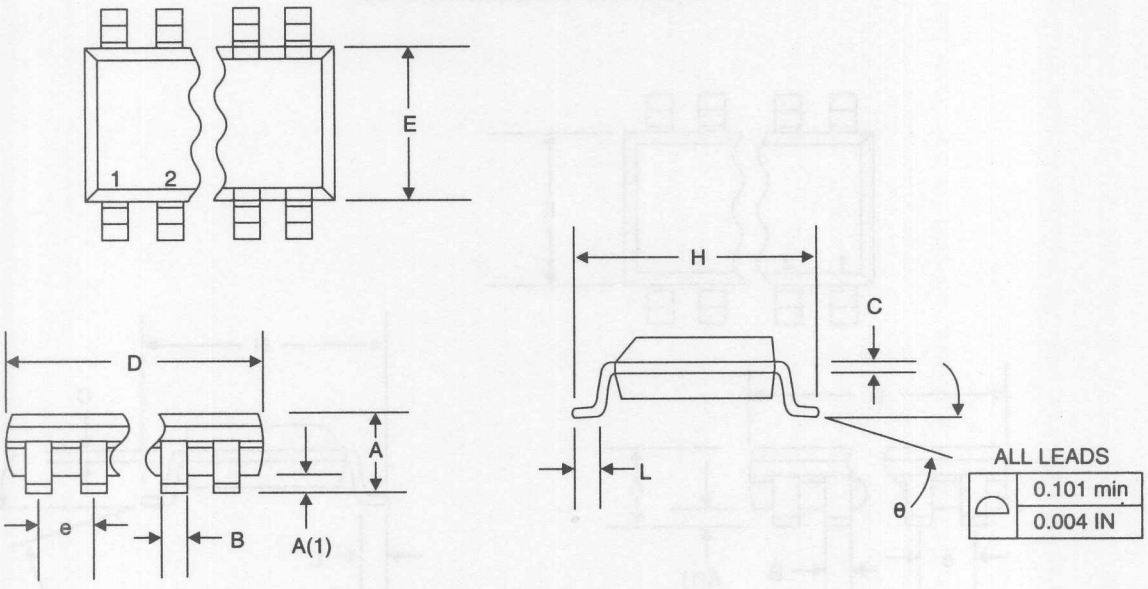
8-Pin Plastic SOIC



NOTES Lead Finish: Solder
Package Composition:
Package: Plastic
Lead Frame: Copper/Iron
Die Attach: Epoxy

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.053	0.069	1.35	1.75
A(1)	0.004	0.010	0.10	0.25
B	0.014	0.018	0.36	0.46
C	0.007	0.009	0.18	0.23
D	0.181	0.205	4.60	5.20
E	0.140	0.160	3.56	4.06
e	0.050 BSC		1.27 BSC	
H	0.224	0.248	5.70	6.30
L	0.024	0.031	0.60	0.80
θ	0º	8º	0º	8º

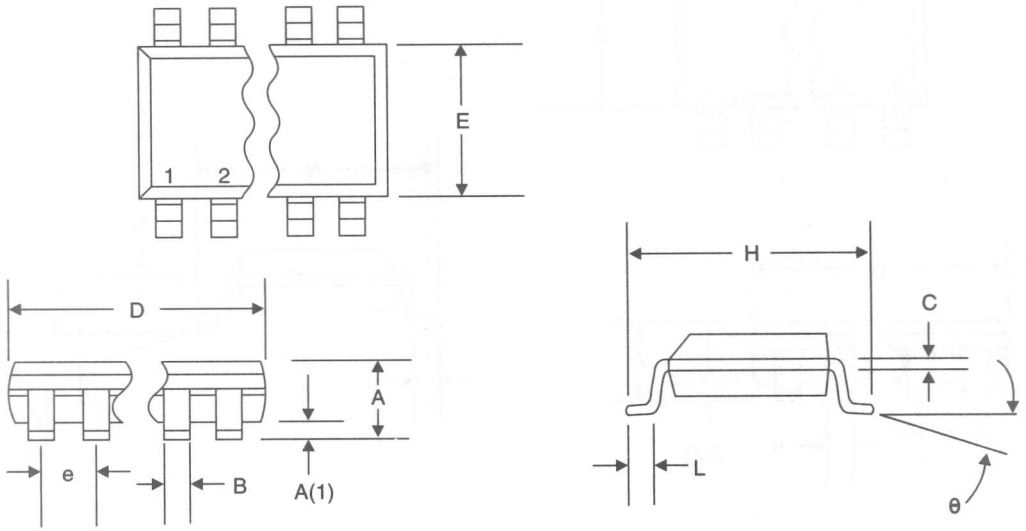
14-Pin Plastic SOIC



NOTES Lead Finish: Solder
Package Composition:
Package: Plastic
Leadframe: Copper/Iron
Die Attach: Epoxy

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.053	0.069	1.35	1.75
A(1)	0.004	0.010	0.10	0.25
B	0.014	0.018	0.36	0.46
C	0.007	0.009	0.18	0.23
D	0.329	0.352	8.36	8.94
E	0.140	0.160	3.56	4.06
e	0.050 BSC		1.27 BSC	
H	0.224	0.248	5.69	6.30
L	0.024	0.031	0.60	0.80
θ	0º	8º	0º	8º

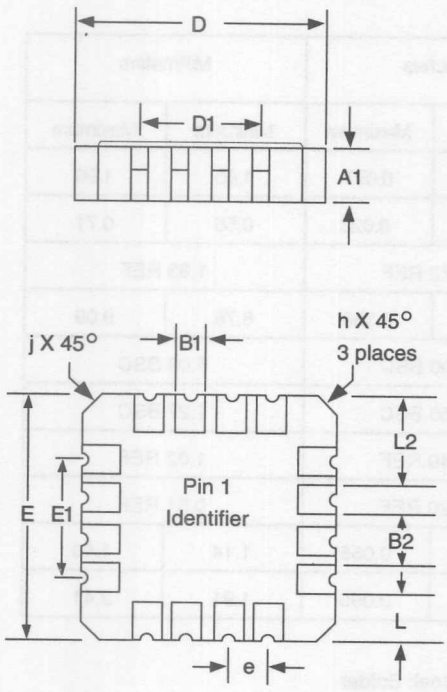
16-Pin Plastic SOIC



NOTES Lead Finish: Solder
Package Composition:
Package: Plastic
Leadframe: Copper
Die Attach: Epoxy

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.058	0.062	1.47	1.57
A(1)	0.005	0.013	0.13	0.33
B	0.014	0.018	0.36	0.46
C	0.006	0.010	0.15	0.25
D	0.386	0.394	9.80	10.01
E	0.150	0.158	3.81	4.01
e	0.050 BSC		1.27 BSC	
H	0.232	0.240	5.89	6.10
L	0.026	0.034	0.66	0.86
θ	0º	8º	0º	8º

16-Terminal Leadless Chip Carrier



Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.065	0.078	1.65	1.98
B1	0.015	0.025	0.38	0.64
B2	0.080 REF		2.03 REF	
D,E	0.245	0.260	6.22	6.60
D1,E1	0.150 BSC		3.81 BSC	
e	0.050 BSC		1.27 BSC	
h	0.040 REF		1.02 REF	
j	0.020 REF		0.51 REF	
L	0.045	0.055	1.14	1.40
L2	0.075	0.095	1.91	2.41

NOTES Seal: Solder
Lead Finish: Solder
Package Composition:
Package: Ceramic
Lid: Gold
Die Attach: Eutectic

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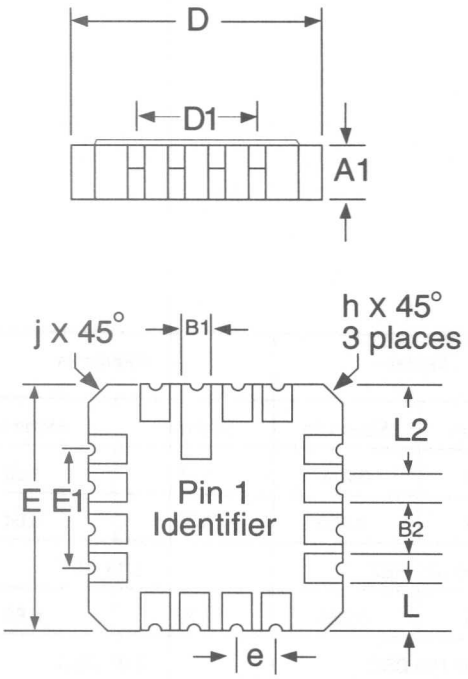
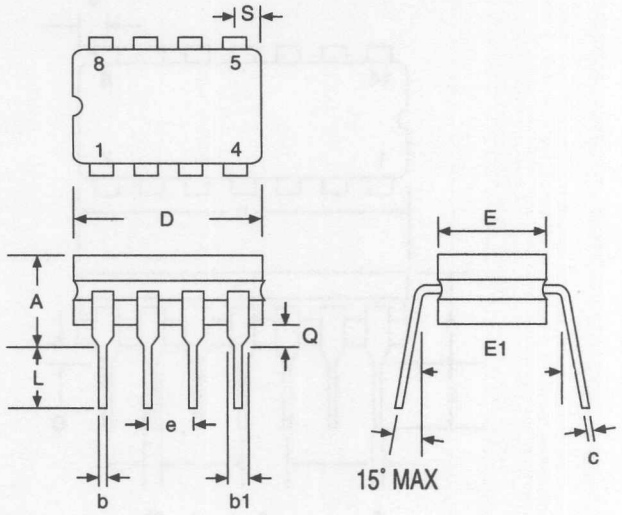
20-Terminal Leadless Chip Carrier



Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.063	0.077	1.60	1.96
B1	0.022	0.028	0.56	0.71
B2	0.072 REF		1.83 REF	
D,E	0.345	0.358	8.76	9.09
D1,E1	0.200 BSC		5.08 BSC	
e	0.050 BSC		1.27 BSC	
h	0.040 REF		1.02 REF	
j	0.020 REF		0.51 REF	
L	0.045	0.055	1.14	1.40
L2	0.075	0.095	1.91	2.41

NOTES
Seal: Solder
Lead Finish: Solder
Package Composition:
Package: Ceramic
Lid: Gold
Die Attach: Eutectic

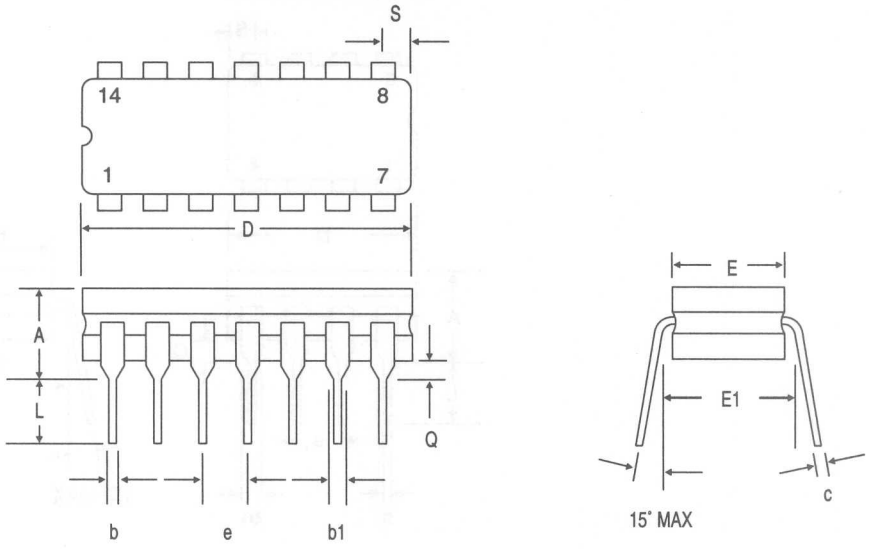
8-Pin CERDIP



NOTES
Seal: Glass
Lead Finish: Solder
Package Composition:
Package: Ceramic
Leadframe: Kovar
Die Attach: Eutectic

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A		0.200		5.08
b	0.014	0.022	0.36	0.56
b1	0.038	0.064	0.97	1.63
c	0.008	0.014	0.20	0.36
D	0.355	0.405	9.02	10.29
E	0.238	0.258	6.05	6.55
E1	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.175	3.18	4.45
Q	0.028	0.058	0.71	1.47
S		0.055		1.40

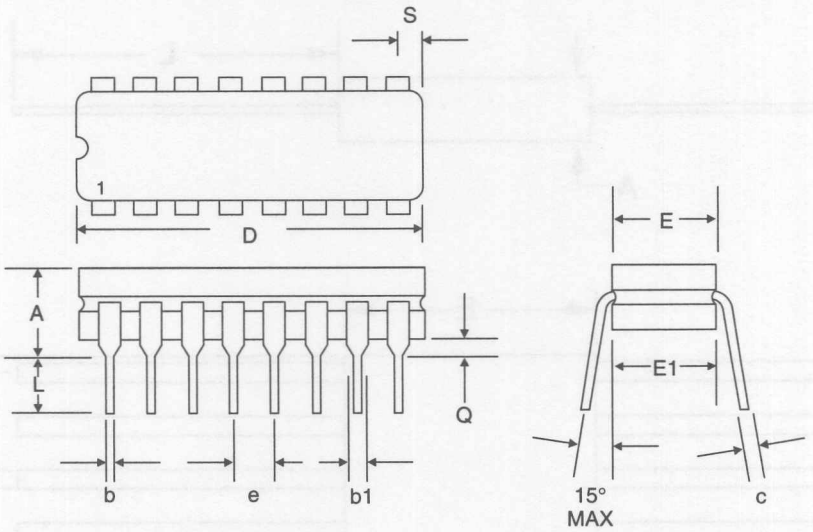
14-Pin CERDIP



NOTES Seal: Glass
Lead Finish: Solder
Package Composition:
Package: Ceramic
Leadframe: Kovar
Die Attach: Eutectic

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A		0.200		5.08
b	0.014	0.026	0.36	0.66
b1	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D		0.785		19.94
E	0.220	0.310	5.59	7.87
E1	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
Q	0.015	0.060	0.38	1.52
S	0.030	0.060	0.76	1.52

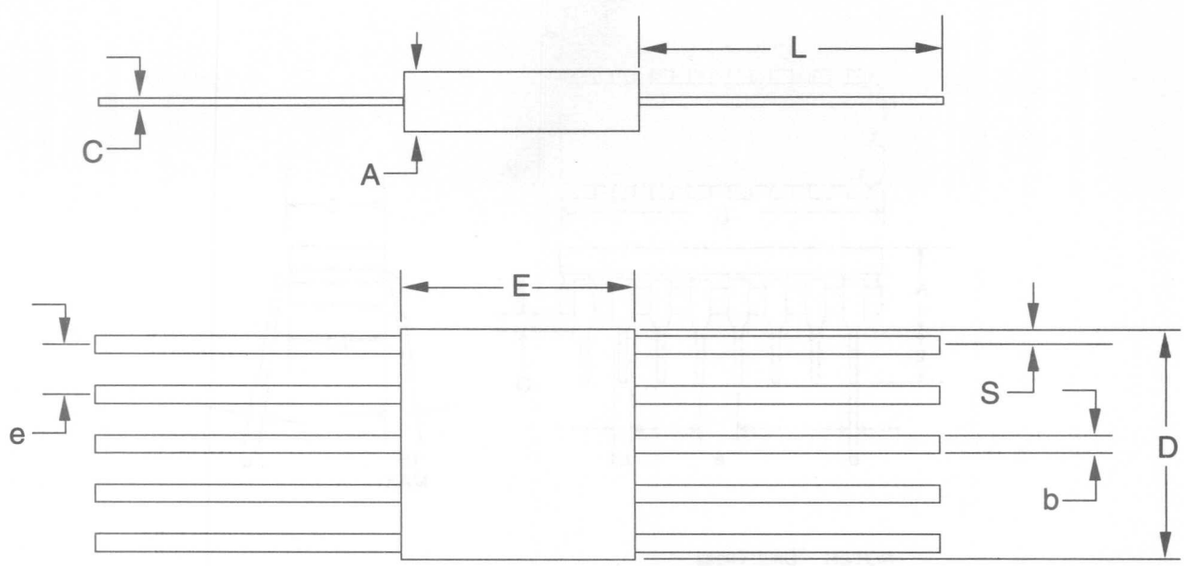
16-Pin CERDIP



NOTES Seal: Glass
Lead Finish: Solder
Package Composition:
Package: Ceramic
Leadframe: Kovar
Die Attach: Eutectic

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A		0.200		5.08
b	0.014	0.026	0.36	0.66
b1	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D		0.840		21.34
E	0.220	0.310	5.59	7.87
E1	0.300 BSC		7.62 BSC	
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
Q	0.015	0.060	0.38	1.52
S	0.030	0.060	0.76	1.52

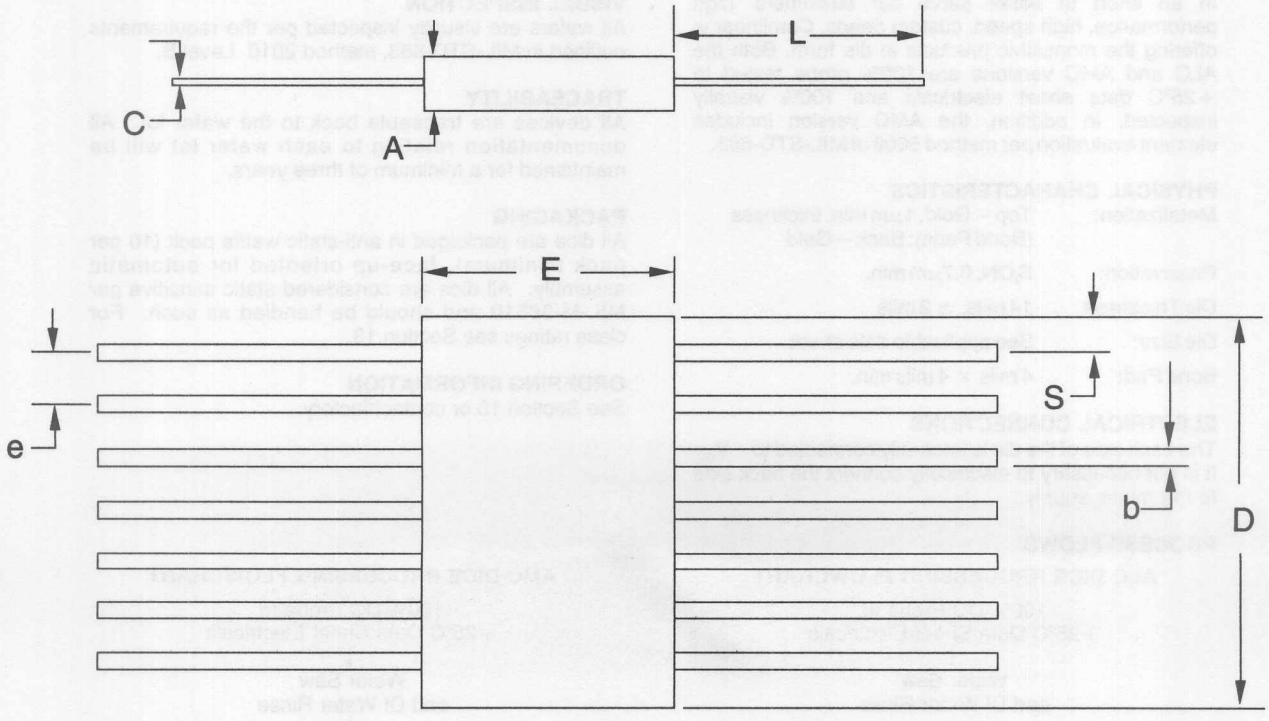
10-Pin CERPACK



NOTES Seal: Glass
Lead Finish: Solder
Package Composition:
Package: Ceramic
Leadframe: Kovar
Die Attach: Eutectic

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.054	0.082	1.37	2.08
b	0.015	0.019	0.38	0.48
C	0.003	0.006	0.08	0.15
D	0.238	0.244	6.05	6.20
E	0.238	0.244	6.05	6.20
e	0.050 BSC		0.127 BSC	
L	0.250	0.370	6.35	9.40

14-Pin CERPACK



NOTES
Seal: Glass
Lead Finish: Solder
Package Composition:
Package: Ceramic
Leadframe: Kovar
Die Attach: Eutectic

Symbol	Inches		Millimeters	
	Minimum	Maximum	Minimum	Maximum
A	0.045	0.090	1.14	2.29
b	0.010	0.022	0.25	0.56
C	0.004	0.009	0.010	0.23
D		0.390		9.91
E	0.235	0.260	5.97	6.60
e	0.050 BSC		0.127 BSC	
L	0.250	0.370	6.35	9.40

In an effort to better serve our customers' high performance, high speed, custom needs, Comlinear is offering the monolithic products in die form. Both the ALC and AMC versions are 100% probe tested to +25°C data sheet electricals and 100% visually inspected. In addition, the AMC version includes element evaluation per method 5008 of MIL-STD-883.

PHYSICAL CHARACTERISTICS

Metalization:	Top – Gold, 1 μm min. thickness (Bond Pads); Back – Gold
Passivation:	S_iON, 0.7 μm min.
Die Thickness:	14 mils, ± 2 mils
Die Size:	See applicable data sheet
Bond Pad:	4 mils × 4 mils min.

ELECTRICAL CONNECTIONS

The back side of the die is internally connected to $-V_{cc}$. It is not necessary to electrically connect the back side to the minus supply.

PROCESS FLOWS

ALC DICE PROCESSING FLOWCHART

100% DC Probe to
+25°C Data Sheet Electricals
↓
Wafer Saw
and DI Water Rinse
↓
Wafer Inspection
↓
Wafer Lot
Qualification
↓
Die Sort
Into Waffle Packs
↓
100% Die Visual
Inspection to
M2010 MIL-STD-883
↓
QA Sample Visual
Inspection and
Document Review
↓
Seal in
Waffle Pack
↓
Stock
(storage in Dry N_2)

AMC DICE PROCESSING FLOWCHART

100% DC Probe to
+25°C Data Sheet Electricals
↓
Wafer Saw
and DI Water Rinse
↓
Wafer Inspection
↓
Element Evaluation
MIL-H-38534
1. Electrical Test per Device SCD
DC at – 55°C, + 25°C, + 125°C
2. Wire Bond Evaluation
↓
Die Sort
Into Waffle Packs
↓
100% Die Visual
Inspection to
M2010 MIL-STD-883
↓
QA Sample Visual
Inspection and
Document Review
↓
Seal in
Waffle Pack
↓
Stock
(storage in Dry N_2)

VISUAL INSPECTION

All wafers are visually inspected per the requirements outlined in MIL-STD-883, method 2010, Level B.

TRACEABILITY

All devices are traceable back to the wafer lot. All documentation relating to each wafer lot will be maintained for a minimum of three years.

PACKAGING

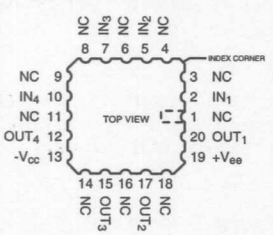
All dice are packaged in anti-static waffle pack (10 per pack minimum), face-up oriented for automatic assembly. All dice are considered static sensitive per MIL-M-38510 and should be handled as such. For class ratings see Section 13.

ORDERING INFORMATION

See Section 15 or contact factory.

LCC Pinouts

CLC114A8L-2



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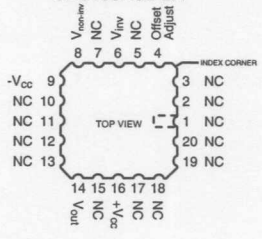

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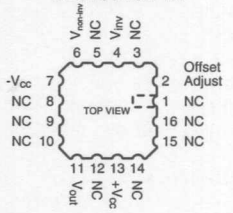

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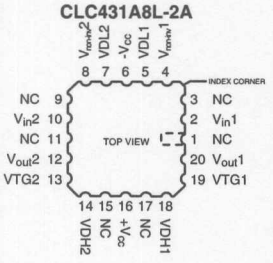

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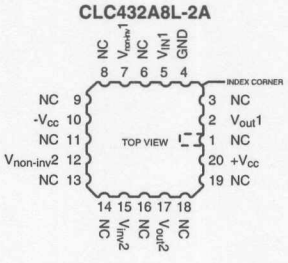

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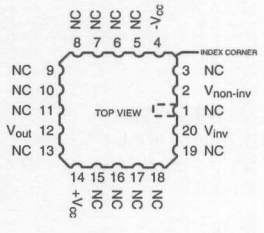

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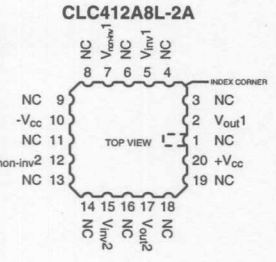

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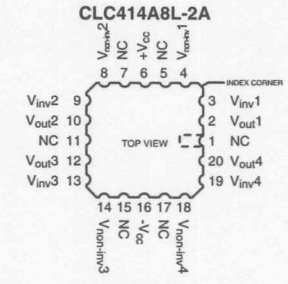

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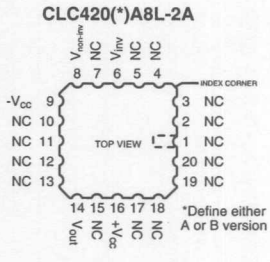
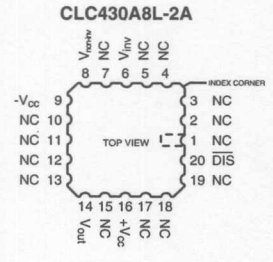


*Define either A or B version

CLC430A8L-2A



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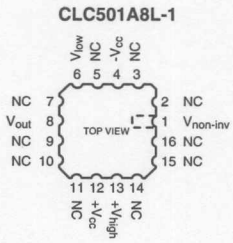

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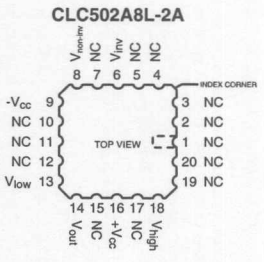

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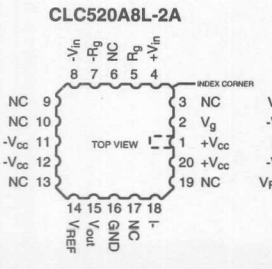

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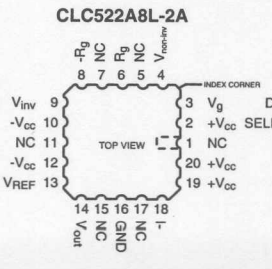

DREF
SELECT
NC
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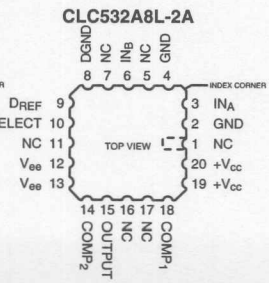
Vee

CLC532A8L-2A



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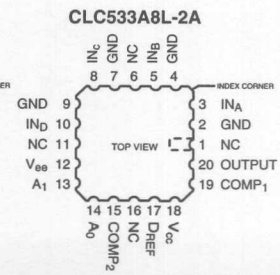

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Product Accessories
Contents

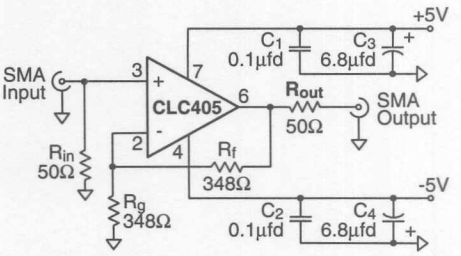
To evaluate Comlinear products, use the following product accessories available from your area representative, distributor, or Comlinear directly.

CLC405

The sample evaluation board for the CLC405 is part number 730061.

The CLC405 uses:

- 2 SMA connectors for both the input and output connections.
- 348Ω R_f and R_g resistors.
- 50Ω R_{in} and R_{out} resistors.
- 0.1µFd ceramic bypass capacitors for C_1 and C_2.
- 6.8µFd tantalum bypass capacitors fro C_3 and C_4.
- split ±5V power supply for +5 and -5V.



The CLC405 does not use:

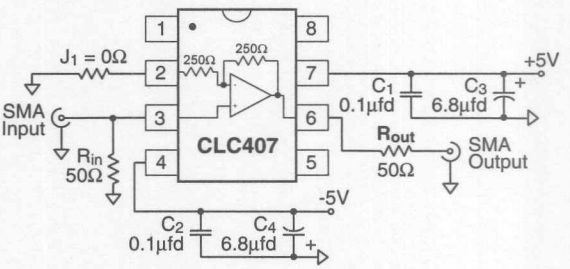
- 0Ω short, J_1.
- "cut here for 407" (do **NOT** cut this trace for 405).

CLC407

The sample evaluation board for the CLC407 is part number 730061.

The CLC407 uses:

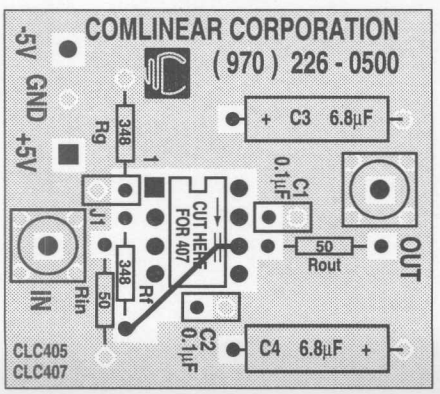
- 2 SMA connectors for both the input and output connections.
- 50Ω R_{in} and R_{out} resistors.
- 0.1µFd ceramic bypass capacitors for C_1 and C_2.
- 6.8µFd tantalum bypass capacitors for C_3 and C_4.
- split ±5V power supply for +5 and -5V.
- "cut here for 407" (carefully cut trace).
- 0Ω short, J1.



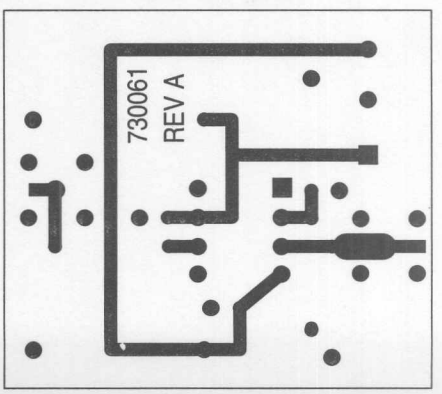
The CLC407 does not use:

- R_f and R_g.

TOP SIDE



BOTTOM SIDE



12

CLC44X Evaluation Boards

Part Numbers 730055, 730060

To aid in the evaluation of the CLC440, CLC446, and CLC449 series of wide bandwidth parts, Comlinear has created the 730055 and the 730060 evaluation boards for the 8-pin DIP and 8-pin SOIC respectively. Both DIP and SOIC evaluation boards are optimized for use with high quality surface-mount resistors and capacitors for obtaining the best high frequency response.

I. Basic Component Selection

The evaluation boards are laid out for a non-inverting gain of 2V/V using low-parasitic surface-mount resistors and capacitors. The CLC44X very high frequency amplifiers can be sensitive to component parasitics that may alter AC performance especially in the high frequency domain. Small adjustments in R_f and/or R_g are recommended to shape the final desired frequency response.

For CFB (the CLC446, and CLC449), increasing R_f from its recommended value will band limit the device's frequency response, while decreasing R_f from its recommended value will peak frequency response. However, substantially decreasing the feedback resistor of a current-feedback amp from its recommended value may cause a part to oscillate. Application note OA-13 "Current-Feedback Amplifier Loop-Gain Analysis and Performance Enhancements" of the data book elaborates on the selection of feedback resistors and their influence on AC performance.

For VFB (the CLC440), increasing both/either R_f and R_g from recommended values may cause high frequency peaking. Decreasing both/either R_f and R_g may help decrease high frequency peaking (without causing oscillations).

II. Basic Connections & Operation

Both the DIP and SOIC evaluation boards provide for input and output signal connections through SMA connectors. These SMAs are connected to the non-inverting input pin (pin 3) and the R_{out} resistor as shown in Figure 1. The recommended feedback resistor value for the CLC44X series is 250Ω. The appropriate gain setting resistor (R_g) is calculated with Eq. 1.

$$A_V = 1 + \frac{R_f}{R_g} \qquad \text{Eq. 1} \qquad (\text{for } A_V = +2 \;\; R_f = R_g = 250\Omega)$$

The R_{out} resistor, of Figure 1, should always be inserted between pin 6 and the output SMA when driving coaxial cable or capacitive loads. The plot in the typical performance section labeled "Settling Time vs. Capacitive Load" of the data sheets should be used to determine the optimum resistor value for R_{out} when driving coax or capacitive loads. This optimal resistance improves settling time for pulse-type applications and increases stability.

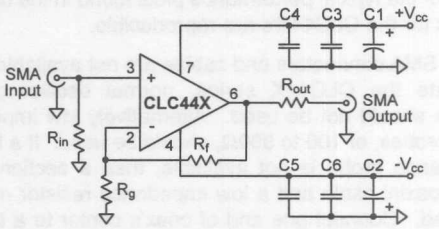


Figure 1: Schematic for 73055/60 Evaluation Boards

Although no DC trim network was included on the evaluation board, OA-07 has specific circuits to correct DC offsets.

Power-supply bypassing capacitors perform a very important function for the CLC44X series and should not be omitted when evaluating these amplifiers. The bypass capacitors not only provide a low impedance current path at the supply pin, but also provide high frequency filtering on the power supply traces. C1 and C2 of Figure 1 should be quality 6.8μF tantalum capacitors. C3 and C4 should be quality 0.01μF ceramic capacitors. C4 and C5 should be quality 500pF ceramic capacitors.

The use of standard dip sockets is not recommended for the CLC44X series DIP amplifiers. These sockets may severely degrade AC performance and may cause oscillations. The 730055 PDIP evaluation board will easily accommodate flush-mount socket pins when socketing is necessary. The printed circuit board device holes are sized for Cambion P/N 450-2598 socket pins or their equivalent.

III. Printed Circuit Board Layout Considerations

The evaluation boards have been carefully laid out to optimize the performance of the CLC44X series. The ground plane on the evaluation boards was removed

near the sensitive nodes (pins 2,3,6) to reduce parasitic capacitances between these nodes and the ground plane. Trace lengths were also minimized to reduce series inductances associated with all components and all nodes.

The CLC44X series is sensitive to the parasitics on traces. This sensitivity includes capacitive coupling from trace to power and trace to ground planes. If leaded components are used, then a low inductive resistor supplied by Precision Resistor Products or its equivalent is highly recommended. In all instances surface-mount components are recommended over leaded components.

IV. Measurement Hints

If 50Ω coax and 50Ω R_{in}/R_{out} resistors are used, many of the typical performance plots found in the data sheets for the CLC44X's are reproducible.

When SMA connectors and cables are not available to evaluate the CLC44X series, normal oscilloscope probes should not be used. Alternatively low impedance probes, of 100 to 500Ω, should be used. If a low impedance probe is not available, then a section of 50Ω coaxial cable and a low impedance resistor may be used. Connect one end of coax's center to a test measurement box terminated in 50Ω and the other end of the cable's center conductor to the low impedance resistor. The open side of the low impedance resistor is now a probe. The ground shield of the cable should be connected to evaluation board ground and test box ground. This cable/resistor probe forms a voltage attenuator between the resistor and the 50Ω termination resistance of the test box. This method allows measurements to be performed directly on the output pin of the amplifier (pin 6). Since the CLC44X series has large bandwidths, measurement equipment should have sufficient bandwidth to accurately measure pulse and frequency responses of the CLC44X series.

V. Parts List for Evaluation Boards

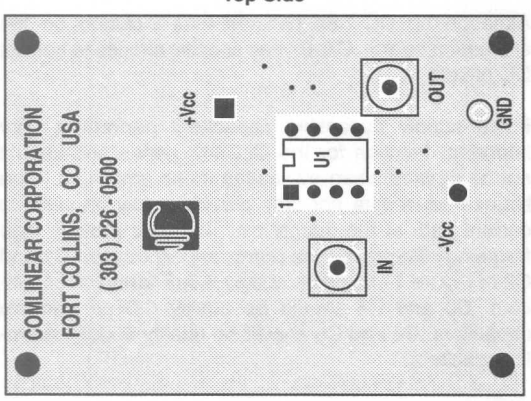
Evaluation Board Parts List - Use the device data sheets with the discussion and examples shown here to select component values.

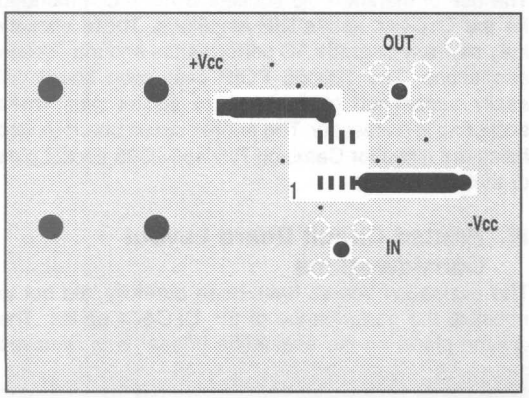
I/O connectors (both board styles):
-SMA (straight) Amphenol 901-144
-SMA (right-angled) Amphenol 901-143

Resistors - 1206 surface-mount type.
Capacitors - Bypassing - 1206 surface-mount type.
Tantalum - TE -Series from Panasonic.

Precision Resistive Products, Inc., Highway 61 South, Mediapolis, Iowa (319) 394-9131.

Top Side





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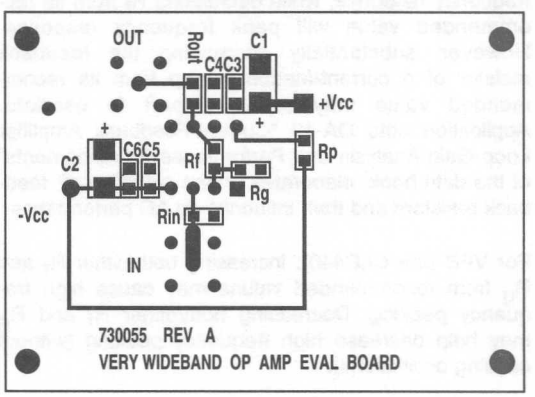
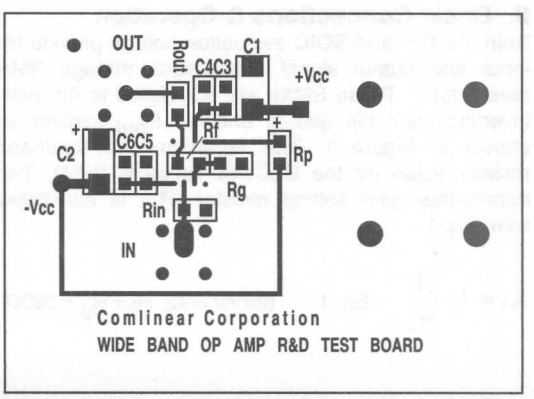




CLC949 Evaluation Board
E949PCASM

Description
The CLC949 Evaluation board is designed to support simple and effective evaluation of the CLC949 Analog-to-Digital Converter. To operate the converter you need only supply power, a clock and a signal to be digitized. The evaluation board uses a common Eurocard connector to make the power, ground and data connections with the rest of the evaluation system. Options exist on the board to use an amplifier based input to the converter, a transformer coupled input, or direct input, as well as options to generate a clock from a sinusoidal source or to use a suitable CMOS clock. The bias points for the converter can be selected via a DIP switch. For a complete description of these various options, please refer to the CLC949 datasheet.

Default Configuration
The CLC949 Evaluation board is shipped loaded with all components except the CLC949, and is configured for options 2 and 4 (D.C. coupled input using amplifiers, sinusoidal clock source). The output data format is Offset Binary and the bias point is selected to be 200µA, allowing 20MHz operation.

Clock Generation
The evaluation circuitry includes a clock generation circuit that will convert a sinusoidal input to a CMOS clock for use by the CLC949. When using this option the clock signal that is provided should be 2-3V_{PP}(10-14dBm). For best results when digitizing high speed input signals, the converter must have a very low jitter clock. To generate this the sinusoidal input must have very low phase noise. In a laboratory environment, Comlinear suggests the use of a low phase noise synthesizer such as the HP8662 or the HP8643 as a clock source.

There is also an option that will enable you to provide a TTL or CMOS clock directly to the board. The clock is provided through an SMA connector, labeled "CLK", regardless of the clocking option chosen. To enable the input of a digital clock, remove the three jumpers labeled "OPT4" and insert a jumper at the point labeled "OPT1-3". These jumpers can be found on the opposite side of the board to the CLC949 and are surface mount 0Ω resistors.

Analog Input Conditioning
The CLC949 requires a differential input signal, centered around a bias point of approximately 2.25V. The evaluation board offers three options for providing this input: option 1 takes a single-ended input signal connnected to the SMA labeled "VIN+" and uses a transformer to phase split the input signal and to provide the appropriate offset voltage. This option will result in the lowest distortion signal for input frequencies of 1MHz or higher. Since the transformer is not able to pass frequencies lower than about 50kHz, this option is not a good choice if your signal must be D.C. coupled. If you want to use this option, install the transformer into the socket on the back side of the board, the "MCL" on the transformer should be near the end labeled "MCL" on the board. Install the two jumpers labeled "OPT1", and remove the three jumpers labeled "OPT2". All of these jumpers can be found on the back side of the board. The transformer, which is tacked into the breadboarding area of the board, is a 1:1 transformer, therefore the input to it should be $2V_{PP}$ in order to obtain a full scale output. Option 2 uses an amplifier based circuit to perform the phase splitting and D.C. offset. This circuit is described in more detail in the CLC949 datasheet. Option 2 is the default condition in which the board is shipped. Using this option, a $2V_{PP}$ signal, with no D.C. offset is applied to the "VIN+" SMA to obtain a full scale output. Option 3 requires that you provide a differential input signal with the proper offsets to the SMA connectors labeled "VIN+" and "VIN-". To enable this option, remove the three jumpers labeled "OPT2" and install the two jumpers labeled "OPT3", and remove the transformer from the socket (if previously installed).

DATA and Clock Outputs
The CLC949 Evaluation board is equipped with 74F574 latches which latch the CLC949 output data and drive the Eurocard connector. An inverted version of the A/D clock is also provided on the Eurocard connector. The output data format of the CLC949 is selectable between Offset Binary or Two's Complement via the jumper "OPT6". For Offset Binary operation install the jumper in the location "OPT6A", Two's Complement is achieved by use of "OPT6B". These jumpers can be found on the front of the board, just above the CLC949 chip.

Bias Control

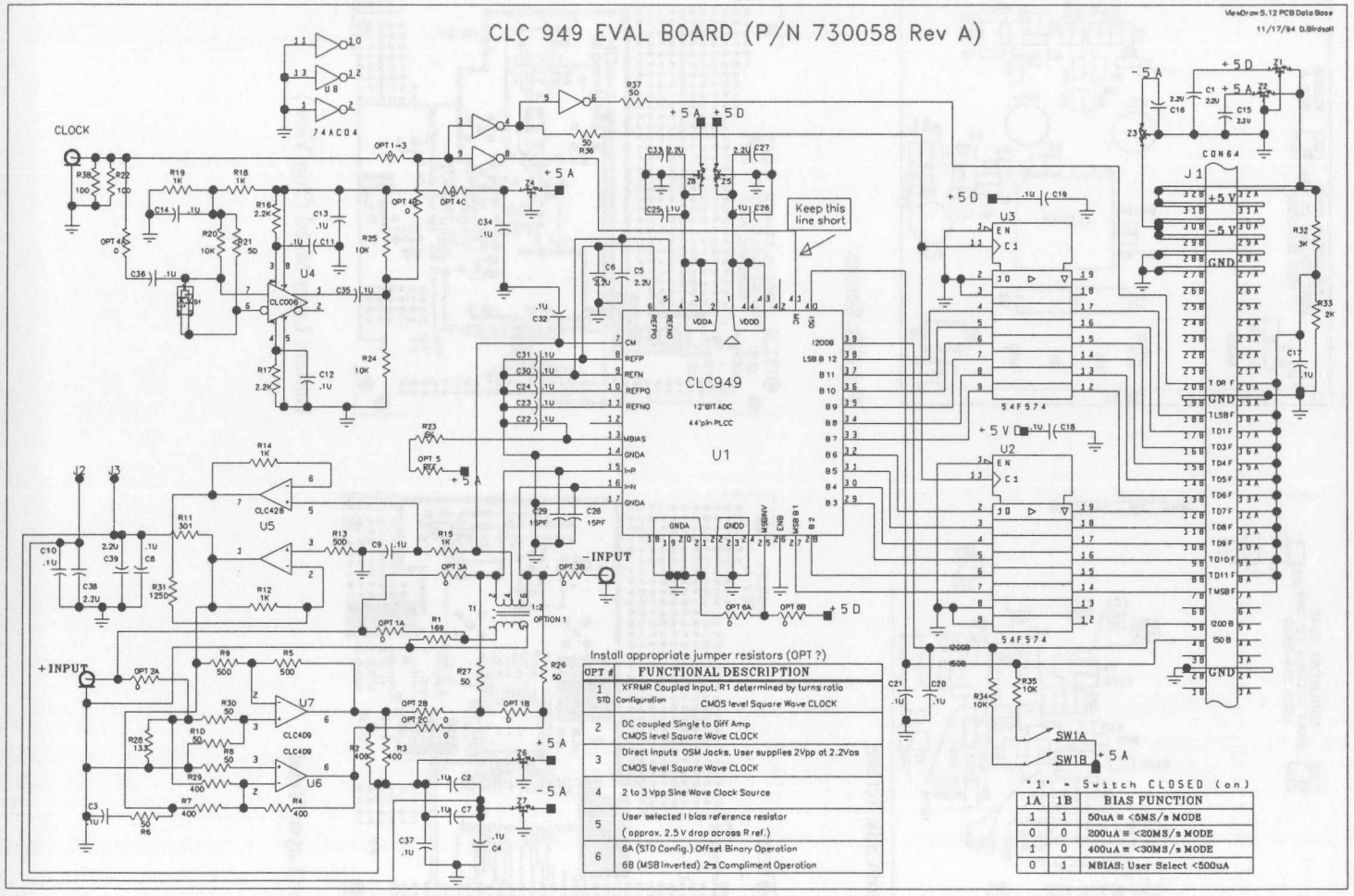
The CLC949 offers you the ability to make a tradeoff between dynamic performance and power dissipation. This can be done by selecting one of three discrete bias points with the DIP switch on the board, or by selecting option 5 which allows analog control of the bias current through the selection of R23. The bias point can be selected according to the following table:

SW1A	SW1B	Bias point
ON	ON	Low Bias
OFF	OFF	Medium Bias
ON	OFF	High Bias
OFF	ON	Set with R23

If you select option 5, you must install the jumper labeled "OPT5". Please refer to the CLC949 datasheet for assistance in selecting an appropriate value for R23.

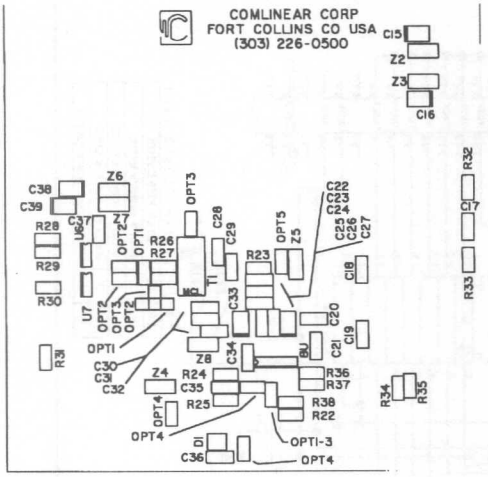
Applications Support

Comlinear maintains a staff of applications engineers who are available to assist you in evaluating the CLC949 or in designing with Comlinear products. They can be reached at:
(800) 776 0500
(303) 225 7422
FAX (303) 226 0564
Email: CLC.APPS@CC.COM

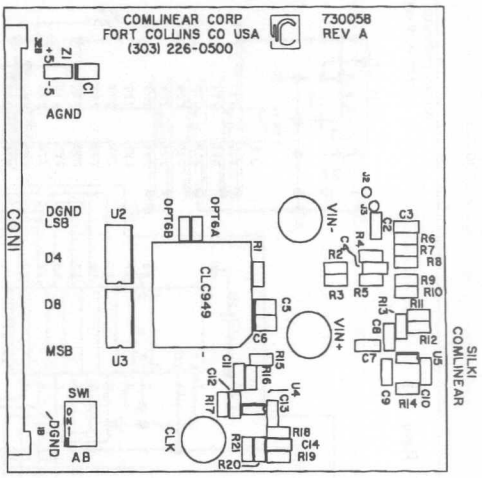


OPT #	FUNCTIONAL DESCRIPTION
1 STD	XFRMR Coupled Input. R1 determined by turns ratio Configuration CMOS level Square Wave CLOCK
2	DC coupled Single to Diff Amp CMOS level Square Wave CLOCK
3	Direct Inputs OSM Jacks. User supplies 2Vpp at 2.2Vos CMOS level Square Wave CLOCK
4	2 to 3 Vpp Sine Wave Clock Source
5	User selected I bias reference resistor (approx. 2.5 V drop across R ref.)
6	6A (STD Config.) Offset Binary Operation 6B (MSB Inverted) 2's Compliment Operation

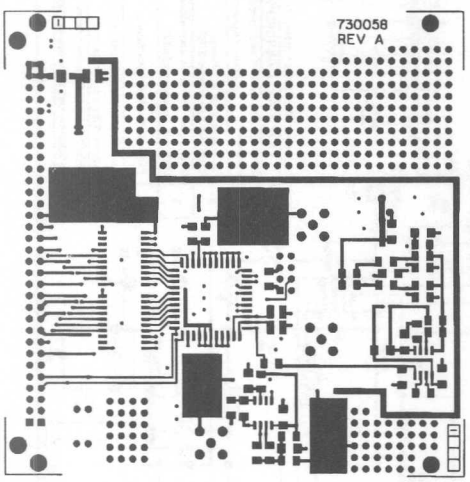
1A	1B	BIAS FUNCTION
1	1	50uA = <5MS/s MODE
0	0	200uA = <20MS/s MODE
1	0	400uA = <30MS/s MODE
0	1	MBIAS: User Select <500uA



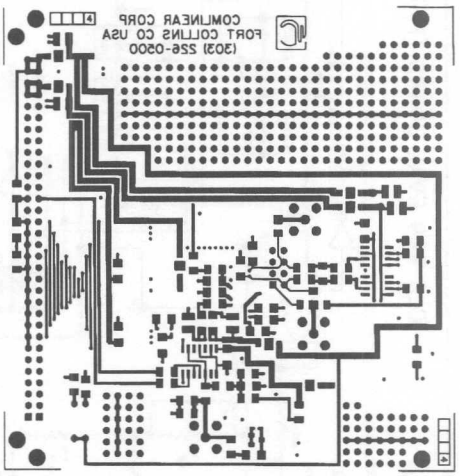
Bottom Silk Screen



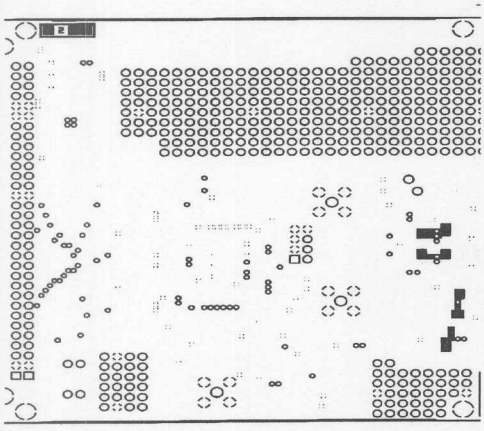
Top Silk Screen



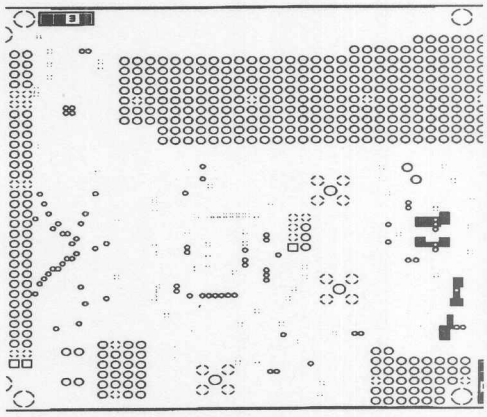
Top Layer Metal



Bottom Layer Metal (Top View)



Layer 2 (Negative)



Layer 3 (Negative, top view)

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Customer Support
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Customer Support

ORDER PLACEMENT

Orders may be placed and information obtained from either your area representative or distributor, via telephone, facsimile and mail, or by contacting National Semiconductor's Customer Response Center at 1-800-272-9959.

If it is determined that a "special" product is required, such as SCD (Specification Control drawing) products, or specially tested products, we recommend that you call your area representative or National Semiconductor's Customer Response Center.

In order to provide maximum service and satisfaction, products should be ordered in their country of end use.

When placing your order, please provide as a minimum, the purchase order number, part number, and ship-to and bill-to address.

TECHNICAL ASSISTANCE

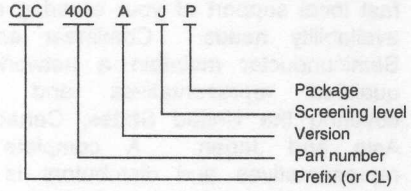
Comlinear and National Semiconductor are dedicated to providing innovative solutions to high-speed signal processing challenges. To support this effort, Comlinear and National Semiconductor maintain a staff of research and development level applications engineers, to provide both technical and design assistance. Their experience, laboratory, and computer simulation resources uniquely qualify them to assist you.

SALES SUPPORT

Comlinear and National Semiconductor's solution to your signal processing needs continues with fast local support of your ordering and product availability needs. Comlinear and National Semiconductor maintain a network of highly qualified representatives and distributors, covering the United States, Canada, Europe, Asia and Japan. A complete listing of representatives and distributors is located in Section 14 of this data supplement.

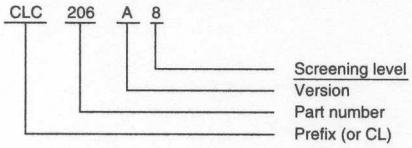
Part Numbering System

MONOLITHIC PRODUCTS:



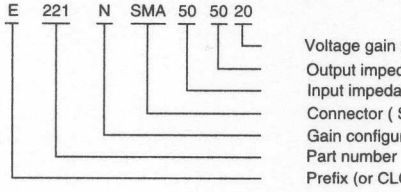
PACKAGE	SCREENING LEVEL[2]
B - CERDIP	C - Commercial
C - Die	I - Industrial
D - Sidebrazed ceramic DIP	J - Industrial
E - Small outline (SO)[1]	L - Industrial (Die)
L - Leadless chip carrier	M - Military Hi-Rel
P - Plastic DIP	S - Level S
	8 - MIL-STD-883, Level B

HYBRID PRODUCTS:

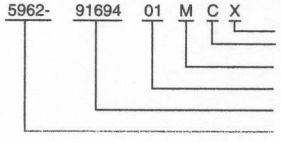


SCREENING LEVEL[2]
I - Industrial
K - Industrial Hi-Rel
M - Military Hi-Rel
S - "Comlinear" S level
8 - MIL-STD-883, Level H

MODULAR AND ENCASED PRODUCTS:



DESC SMD PRODUCTS:



LEAD FINISH
A - Hot solder dip
C - Gold electroplate
X - Any of the above

NOTES:
1. Tape and reel packaging available; order by putting "-TR9 (for 9" reels) or -TR13 (for 13" reels) at the end of part number.
2. See Section 2, Quality and Reliability, for detail process flows.
3. DESC SMD devices are marked with the SMD number ONLY; no Comlinear number.