LM20k POL Module Reference Design

Texas Instruments
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Introduction

The LM20k is a full-featured synchronous buck switching regulator capable of driving up to 6A of load current and converting an input voltage between 2.95V and 5.5V down to an output voltage as low as 0.8V. Fault protection features include cycle-by-cycle current limit, output power good, and output over-voltage protection. The dual function soft-start/tracking pin can be used to control the startup response and the precision enable pin can be used to easily sequence the LM20k in applications with sequencing requirements. The LM20k is available in an eTSSOP-16 package with an exposed pad for enhanced thermal performance.

The LM20k POL module described in this application note has been designed to balance overall solution size with the efficiency of the regulator while showcasing high power density. Note the content that follows is somewhat specific to the LM20146 6A regulator yet the concepts, recommendations and guidelines set forth generally apply to all members of the LM20k low voltage family.

The reference design module measures just under 0.9" x 0.6" on a four layer PCB. The power stage and compensation components of the LM20k module have been optimized for an input voltage of 5V and a switching frequency of 500 kHz, but for testing purposes the input can be varied across the entire operating range. The output voltage of the evaluation board is nominally 1.8V and this voltage can be easily changed by replacing one of the feedback resistors (R_{FB1} or R_{FB2}). The output voltage can also be adjusted within the range of ±30% by attaching a resistor between the TRIM pin to ground to trim up the output voltage or between the TRIM pin to VOUT to trim down the output voltage. The control loop compensation has been designed to provide a stable solution over the entire input and output voltage range with a reasonable transient response.

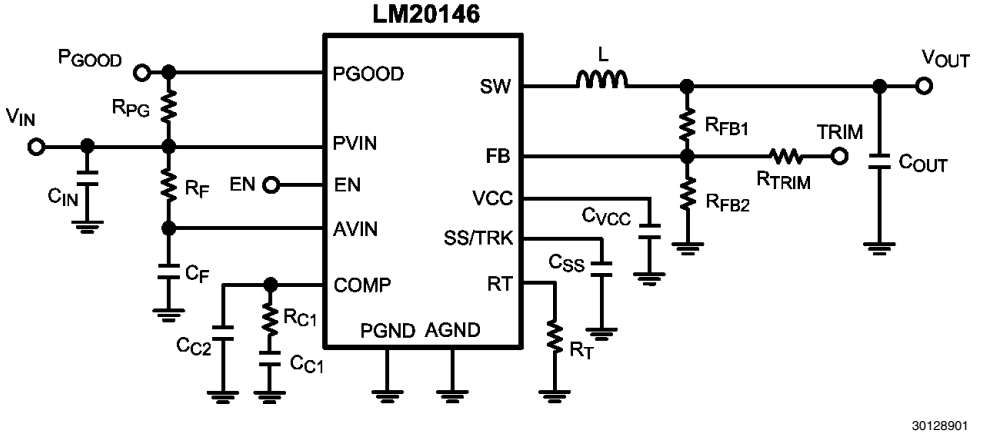


FIGURE 1. Reference Design Schematic

Bill of Materials

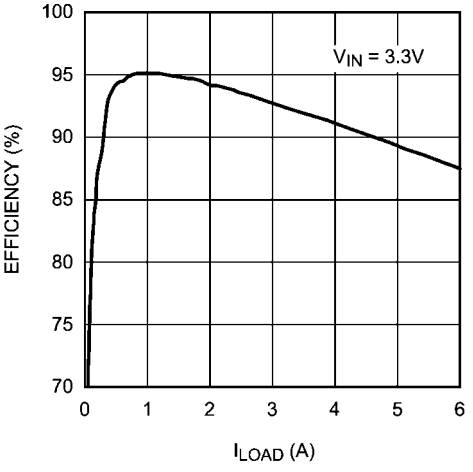
Designator	Description	Part Number	Qty	Manufacturer
U1	Synchronous Buck Regulator	LM20146MH	1	National Semiconductor
C_{IN}	100 µF, 20%, 1206, X5R, 6.3V	GRM31CR60J107ME39	1	Murata
C_{OUT}	100 µF, 20%, 1206, X5R, 6.3V	GRM31CR60J107ME39	1	Murata
L	1.5 µH, 20%, 9.7 mΩ	SPM6530T-1R5M100	1	TDK
R_F	1Ω, 5%, 0.063W, 0402	CRCW04021R00JNED	1	Vishay
C_F	100 nF, 10%, 0402, X7R, 10V	GRM155R61A104KA01	1	Murata
C_{VCC}	1 µF, 10%, 0402, X5R, 6.3V	GRM155R61A105KE15	1	Murata
R_{PG}	10 kΩ, 1%, 0.063W, 0402	CRCW040210K0FKED	1	Vishay
R_{C1}	7.5 kΩ, 1%, 0.063W, 0402	CRCW04027K5FKED	1	Vishay
C_{C1}	1.5 nF, 5%, 0402, X7R, 25V	C0402C152J3RACTU	1	Kemet
C_{C2}	OPEN	OPEN	0	N/A
C_{SS}	33 nF, 10%, 0402, X7R, 25V	C0402C333K3RACTU	1	Kemet
R_T	100 kΩ, 1%, 0.063W, 0402	CRCW0402100K0FKED	1	Vishay
R_{FB1}	15 kΩ, 1%, 0.063W, 0402	CRCW040215K0FKED	1	Vishay
R_{FB2}	12 kΩ, 1%, 0.063W, 0402	CRCW0402112K0FKED	1	Vishay
R_{TRIM}	10 kΩ, 1%, 0.063W, 0402	CRCW040210K0FKED	1	Vishay
R_{EN}	10 kΩ, 1%, 0.063W, 0402	CRCW040210K0FKED	1	Vishay
VIN, VOUT, GND, EN, TRIM, PGOOD	Solder Mount PCB Pin	3125-2-00-34-00-00-08-0	6	Mill-Max

Connection Descriptions

Terminal Silkscreen	Description
VIN	This terminal is the input voltage to the device. The device will operation over the input voltage range of 2.95V to 5.5V. The absolute maximum voltage rating for this pin is 6V.
GND	This terminal is the ground connection to the device. There are two different GND connections on the PCB. One should be used for the input supply and the other for the load.
VOUT	This terminal connects to the output voltage of the power supply and should be connected to the load.
EN	This terminal connects to the enable pin of the device. There is a 10 kΩ pull-up resistor from this pin to the input voltage. If driven externally, a voltage typically greater than 1.18V will enable the device. The operating voltage for this pin should not exceed 5.5V. The absolute maximum voltage rating on this pin is 6V.
TRIM	This terminal enables the output to be trimmed up or down. Connect TRIM to GND or VOUT using a resistor to trim up or down, respectively.
PGOOD	This terminal connects to the power good output of the device. There is a 10 kΩ pull-up resistor from this pin to the input voltage. The voltage on this pin should not exceed 5.5V during normal operation and has an absolute maximum voltage rating of 6V.

Performance Characteristics

Efficiency vs Output Current (V_{IN} = 3.3V)



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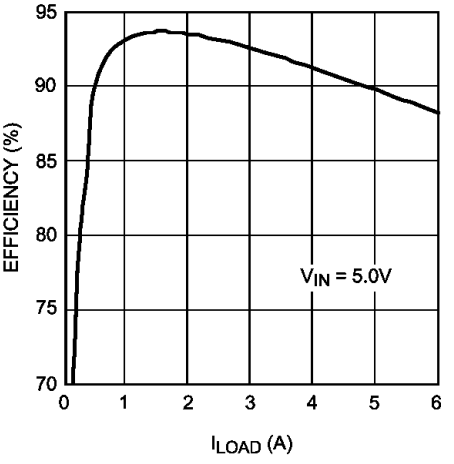
Efficiency vs Output Current (V_{IN} = 5.0V)



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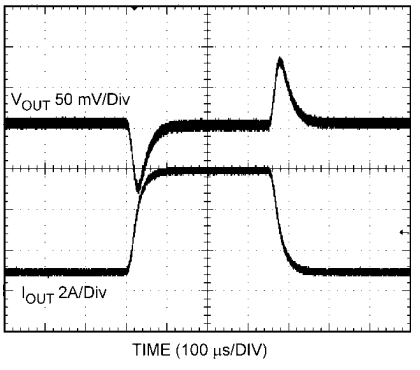
1A to 6A Load Transient Response



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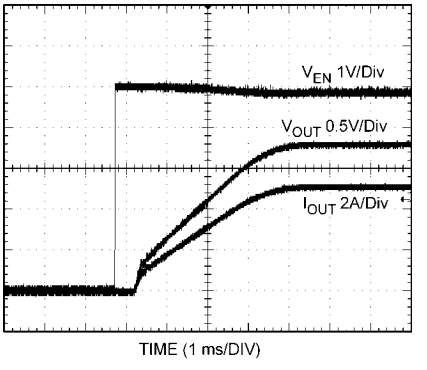
Startup Waveform



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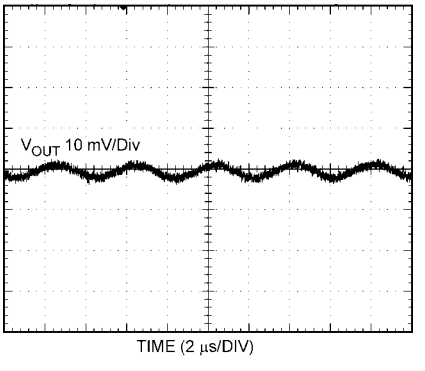
Output Ripple Waveform



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Component Selection

This section provides a walk-through of the design process of the LM20k POL module. Unless otherwise indicated all equations assume units of Amps (A) for current, Farads (F) for capacitance, Henries (H) for inductance, and Volts (V) for voltages.

INPUT CAPACITOR

The required RMS current rating of the input capacitor for a buck regulator can be estimated by the following equation:

$$I_{CIN(RMS)} = I_{OUT}\sqrt{D(1 - D)}$$

The variable D refers to the duty cycle and can be approximated by:

$$D = \frac{V_{OUT}}{V_{IN}}$$

From this equation, it follows that the maximum $I_{CIN(RMS)}$ requirement will occur at a full 6A load current with the system operating at 50% duty cycle. Under this condition, the maximum $I_{CIN(RMS)}$ is given by:

$$I_{CIN(RMS)} = 6A\sqrt{0.5 \times 0.5} = 3A$$

Ceramic capacitors feature a large I_{RMS} rating in a small footprint, making a ceramic capacitor ideal for this application. A 100 µF X5R ceramic capacitor from Murata with a 5.4A I_{RMS} rating provides the necessary input capacitance for this implementation.

AVIN FILTER

An RC filter should be added to prevent any switching noise on PVIN from interfering with the internal analog circuitry connected to AVIN. These can be seen on the schematic as components R_F and C_F. There is a practical limit to the size of the resistor R_F as the AVIN pin will draw a short 60mA burst of current during startup, and if R_F is too large the resulting voltage drop can trigger the UVLO comparator. For this reference design, a 1Ω resistor is used for R_F ensuring that UVLO will not be triggered after the part is enabled. A recommended 1 µF C_F capacitor coupled with the 1Ω resistor provides roughly 10dB of attenuation at the 500 kHz switching frequency.

INDUCTOR

As per datasheet recommendations, the inductor value should initially be chosen to give a peak to peak ripple current equal to roughly 30% of the maximum output current. The peak to peak inductor ripple current can be calculated by the equation:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT})D}{Lf_{SW}}$$

Rearranging this equation and solving for the inductance reveals that for this application (V_{IN} = 5V, V_{OUT} = 1.8V, f_{SW} = 500 kHz, I_{OUT} = 6A) the nominal inductance value is approximately 1.28 µH. A final inductance of 1.5 µH is selected to minimize the inductor size and dc resistance. This results in a peak-to-peak ripple current of 1.8A and 2.24A when the converter is operating from 5V and 3.3V input rails, respectively. Once an inductance value is calculated, an actual inductor needs to be selected based on a trade-off between physical size, efficiency, and current carrying capability. For this LM20k reference design, a TDK SPM6530T-1R5 inductor offers a good balance between efficiency (9.7 mΩ DCR), size, and saturation current rating (11.5A I_{SAT} rating). If the output voltage of the evaluation board is increased, there is a chance the device may hit current limit at 6A output. To avoid current limit with higher output voltages, the value of the inductor should be increased to reduce the ripple current.

OUTPUT CAPACITOR

The value of the output capacitor in a buck regulator influences the voltage ripple that will be present on the output voltage, as well as the large signal output voltage response to a load transient. Given the peak-to-peak inductor current ripple (ΔI_{P-P}) the output voltage ripple can be approximated by the equation:

$$\Delta V_{OUT} = \Delta I_{P-P} \times \sqrt{R_{ESR}^2 + \left(\frac{1}{8 \times f_{SW} \times C_{OUT}}\right)^2}$$

The variable R_{ESR} above refers to the ESR of the output capacitor. As can be seen in the above equation, the ripple voltage on the output can be divided into two parts, one of which is attributed to the AC ripple current flowing through the ESR of the output capacitor and another associated with the AC ripple current actually charging and discharging the output capacitor. The output capacitor also has an effect on the amount of droop that is seen on the output voltage in response to a load transient event.

For this reference design, a Murata 100 µF ceramic capacitor is selected for the output capacitor to provide good transient and DC performance in a relatively small package. From the technical specifications of this capacitor, the ESR is roughly 2 mΩ and the effective in-circuit capacitance is approximately 55 µF (reduced from 100 µF with the 1.8V DC bias). With these values, the peak to peak voltage ripple on the output when operating from a 5V input can be calculated at 9 mV.

C_{SS}

A soft-start capacitor can be used to control the startup time of the LM20k voltage regulator. The startup time of the regulator when using a soft-start capacitor can be estimated by the following equation:

$$t_{SS} = \frac{0.8V \times C_{SS}}{I_{SS}}$$

For the LM20k, I_{SS} is nominally 5 µA. For this reference design, the soft-start time has been designed to be 5 ms, resulting in a C_{SS} capacitor value of 33 nF.

C_{VCC}

The C_{VCC} capacitor is necessary to bypass an internal 2.7V subregulator. This capacitor should be sized equal to or greater than 1 µF but less than 10 µF. A value of 1 µF is sufficient for most applications.

C_{C1}

The capacitor C_{C1} is used to set the crossover frequency of the LM20k control loop. Since this board was optimized to work over the full input voltage, output voltage, and frequency

ranges, the value of C_{C1} was selected to be 1.5 nF. Once the operating conditions for the device are known, the transient response can be optimized by reducing the value of C_{C1} and calculating the value for R_{C1} as outlined in the next section.

R_{C1}

Once the value of C_{C1} is known, resistor R_{C1} is used to place a zero in the control loop to cancel the output filter pole. This resistor can be sized according to the equation:

$$R_{C1} = \left[\frac{C_{C1}}{C_{OUT}} \times \left[\frac{I_{OUT}}{V_{OUT}} + \frac{1 - D}{f_{SW} \times L} + \frac{10 \times D}{V_{IN}} \right] \right]^{-1}$$

For stability purposes the device should be compensated for the maximum output current expected in the application.

C_{C2}

A second compensation capacitor C_{C2} can be used in some designs to provide a high frequency pole, useful for cancelling a possible zero introduced by the ESR of the output capacitor. For the LM20k reference design module, the C_{C2} footprint is unpopulated, as the low ESR ceramic capacitor used on the output does not contribute a zero to the control loop before the crossover frequency. If the ceramic capacitor on the reference design board is replaced with a different capacitor having significant ESR, the required value of the capacitor C_{C2} can be estimated by the equation:

$$C_{C2} = \frac{C_{OUT} \times R_{ESR}}{R_{C1}}$$

R_T

The value for R_T will set the operating frequency of the device. For this reference design, a value of 100 kΩ was chosen which sets oscillator frequency to 500 kHz. The value of R_T can be adjusted to support operating frequencies from 250 kHz to 750 kHz by using the equation:

$$R_T = \left(\frac{78000}{f_{SW}} \right) - 55$$

where f_{SW} is the switching frequency in kHz and R_T is the frequency adjust resistor in kΩ.

R_{FB1} and R_{FB2}

The resistors labeled R_{FB1} and R_{FB2} create a voltage divider from V_{OUT} to the feedback pin that is used to set the output voltage of the regulator. Nominally, the output of the LM20k reference design module is set to 1.8V, giving resistor values of R_{FB1} = 15 kΩ and R_{FB2} = 12 kΩ. If a different output voltage is required, the value of R_{FB1} can be adjusted according to the equation:

$$R_{FB1} = \left(\frac{V_{OUT}}{0.8} - 1 \right) \times R_{FB2}$$

R_{FB2} does not need to be changed from its value of 12 kΩ.

TRIM RESISTOR

The output voltage can be varied by using the TRIM pin. The resistor between the feedback (FB) node and the TRIM pin (R_{TRIM}) determines the output voltage adjustable range. To increase the output voltage, a resistor needs to be attached between the TRIM pin and ground (R_{UP} in *Figure 2*). Conversely, to decrease the output voltage, a resistor needs to be attached between the TRIM pin and the VOUT pin (R_{DOWN} in *Figure 2*). The resistor values for a desired output voltage can be calculated by the equations listed in *Table 1*. A value of R_{TRIM} = 10 kΩ is recommended to adjust the output voltage from 1.2V to 3.0V while keeping an acceptable control loop compensation. With R_{TRIM} = 10 kΩ selected, an output voltage of 3.0V can be achieved simply by shorting the TRIM pin to ground, and an output voltage of 1.2V can be achieved by shorting TRIM to V_{OUT}. To keep the nominal output voltage of 1.8V, the TRIM pin should be left open.

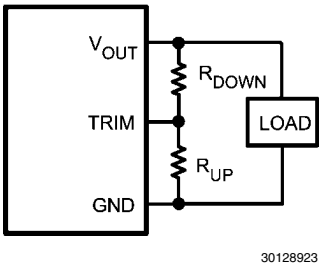
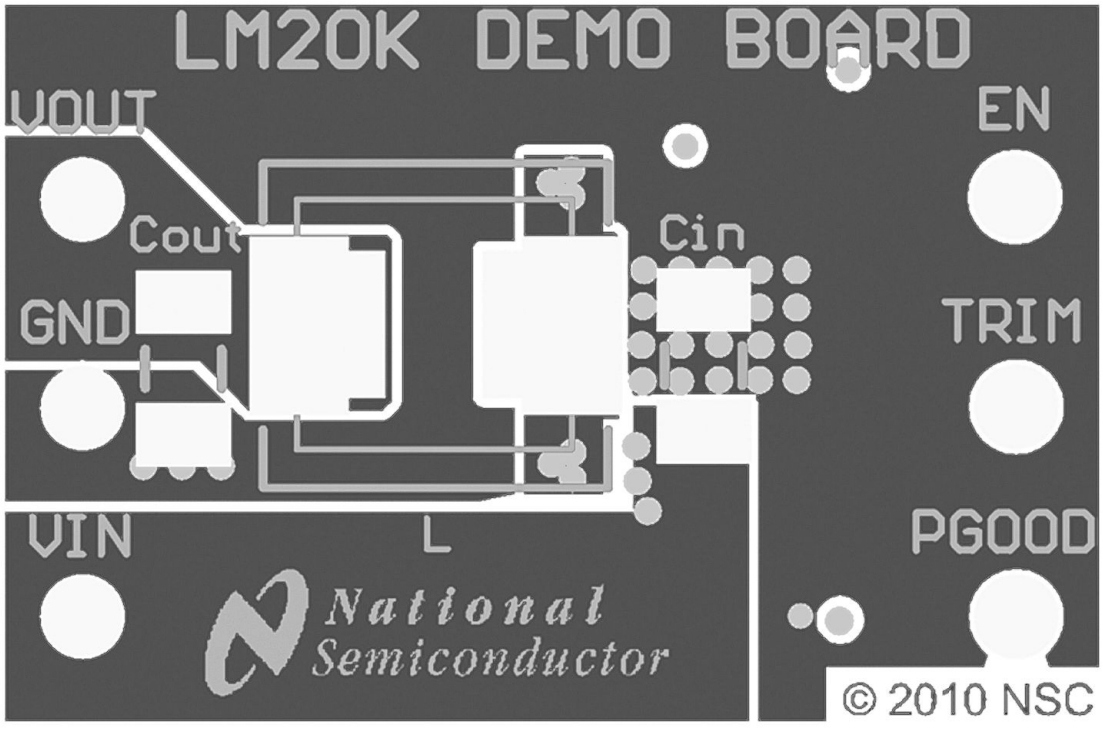


FIGURE 2.

TABLE 1.

Nominal Output Voltage	Trim Equations
1.8V	$R_{UP} = \frac{144}{12(V_{OUT} - 0.8) - 12} - 10$
	$R_{DOWN} = \frac{180(V_{OUT} - 0.8)}{12 - 12(V_{OUT} - 0.8)} - 10$

PCB Layout



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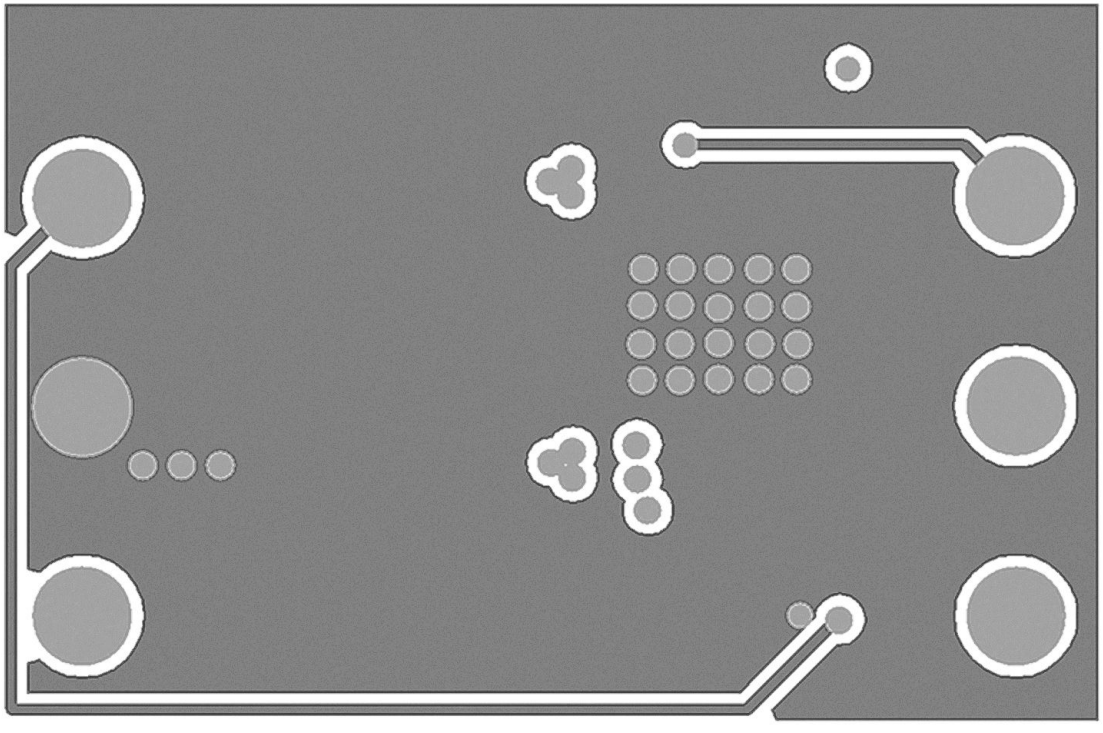
Top Layer



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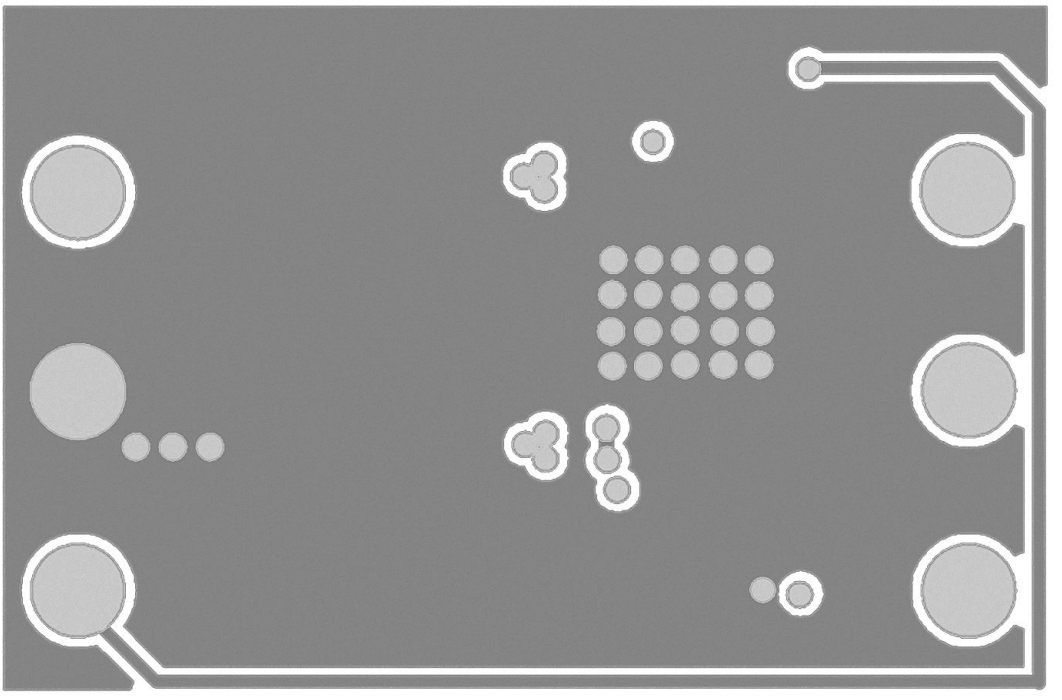
Midlayer 1



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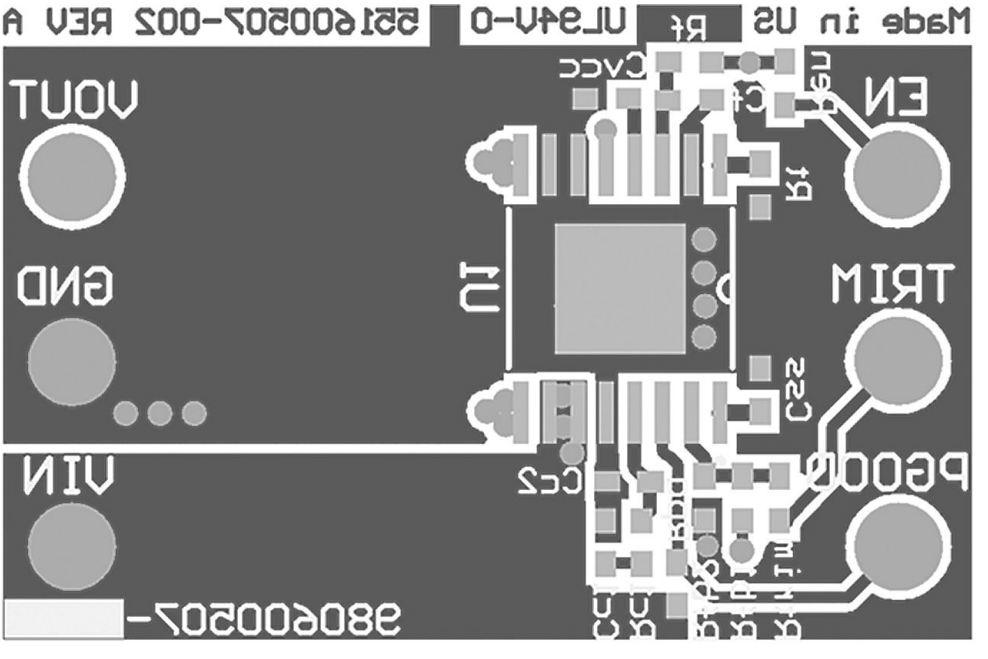

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Bottom Layer