# Voltage Doubler Design and Analysis

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## INTRODUCTION

Today's wireless applications demand lower operating voltages. A voltage doubler provides a means of obtaining a wider VCO tuning range at lower voltages. This paper discusses the considerations that need to be made when using a voltage doubler. Specific test results are shown for a CDMA application.

The LMX2350 provides an internal switched capacitor voltage doubler circuit that allows the RF charge pump to operate close to twice the RF $V_{CC}$ voltage. An external capacitor, $C_{ext}$, placed across the voltage doublers output, $V_P$, is charged up by the internal switched capacitor switched on and off at the rate of the RF crystal oscillator frequency. The minimum allowable voltage droop will determine the size of the external capacitor. The amount of current the voltage doubler can deliver and still maintain its voltage is considerably smaller than the instantaneous current demanded by the charge pump when it is on. Therefore, a large external capacitor is needed to reduce the voltage droop. The time it takes the voltage doubler to charge the external capacitor to twice $V_{CC}$ once the part is enabled is also set by the size of the external capacitor. Another consideration when using the voltage doubler is the average current required by the charge pump when the PLL is locked. This current will reduce the output voltage of the doubler.

**NOTE:** For the LMX2350/52/54 Frequency Synthesizer Series, the voltage output of the doubler cannot exceed the 5.5 volts, which is the maximum specification for the RF charge pump power supply, $V_P$.

## VOLTAGE DOUBLER CONCEPTS

The voltage doubler uses a switched capacitor to double the supply voltage, shown in *Figure 1*.

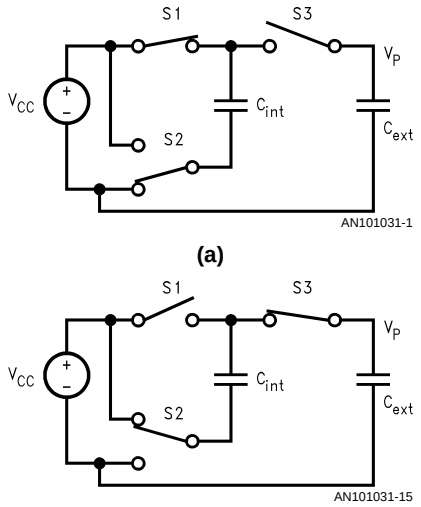



**FIGURE 1. Voltage Doubler Switched Capacitor Circuit**

During the first half of the oscillator cycle switch S1 is closed, S2 is down and S3 is open, as shown in *Figure 1a*. This allows the internal capacitor to charge up to $V_{CC}$. The second half of the oscillator cycle switch S1 is open, S2 is up, and S3 is closed, as shown in *Figure 1b*. This places the voltage on the internal capacitor in series with the supply voltage. Charge is redistributed to the external capacitor, $C_{ext}$. The internal switched capacitor can be ideally represented as a resistor and a voltage source as shown in *Figure 2*.



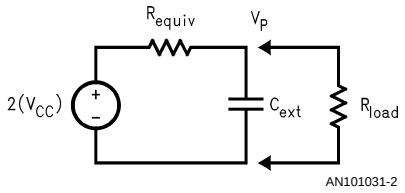



**FIGURE 2. Voltage Doubler Switched Capacitor Realization Equivalent**

$$R_{equiv} = \frac{1}{C_{int} \bullet F_{clock}} \quad (1)$$

$F_{clock}$ = RF Crystal Oscillator Input Frequency

## DESIGN CONSIDERATIONS

### Steady State Voltage Loss When in Lock

The steady state voltage loss is the difference between the ideal doubled voltage and the actual steady state $V_P$ voltage. The steady state voltage loss is set by three factors; charge pump current setting, phase detector frequency, and RF oscillator frequency. When the PLL is locked, the charge pump is on for a short period of time every phase detector cycle. Current is required during this on time to operate the charge pump. These bursts of current averaged over the entire phase detector period can be viewed as a constant load, as shown in *Figure 2*. This load will reduce the voltage doubler's output voltage, $V_P$. Higher charge pump current settings and higher phase detector frequencies will increase the average load current, decreasing the voltage doubler's output voltage, $V_P$. However, a higher RF Oscillator Frequency will reduce the switched capacitor equivalent resistance, increasing the voltage doubler's output voltage, $V_P$. *Figure 3* plots the LMX2350 steady state $V_P$ voltage versus phase detector frequency, $F_{pd}$, for three charge pump current settings when the RF Oscillator Frequency is 10 MHz and $V_{CC}$ set to 3.0V.

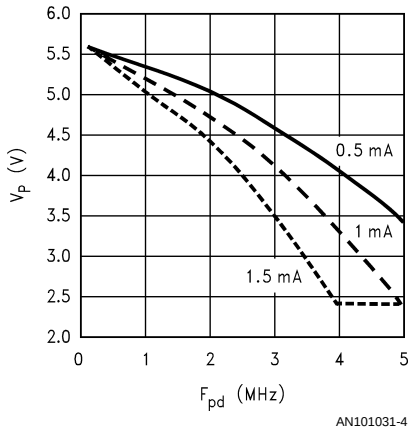



**FIGURE 3. Steady State $V_P$ vs. Fpd ($OSC_{in}$ = 10 MHz; $V_{CC}$ = 3.0V)**

*Equation (2)* can be used to linearly approximate the steady state voltage loss for the LMX2350.

$$V_{SS} = 0.3 - \frac{F_{pd}(MHz)[2 + 4Icp(mA)]}{OSC_{in}(MHz)} \quad (2)$$

### Dynamic $V_P$ Droop During Frequency Changes

When the PLL is programmed to switch frequencies, the loop voltage is forced to a new level corresponding to the new VCO frequency. Charge is either put into or removed from the loop filter depending on whether the loop voltage needs to be increased or decreased. Since the voltage doubler cannot source large amounts of current, the external capacitor needs to supply the current required to change the loop filter voltage. The external capacitor must be initially charged before the charge pump can transfer charge to the loop filter. The transfer of charge will cause the voltage on the external capacitor, $C_{ext}$, to decrease or droop. This voltage droop will reduce the effective upper limit of the VCO tuning range. Some charge is lost trying to change the loop filter voltage due to charge pump overhead current, which is current consumed by the charge pump circuitry. *Equation (3)* shows the charge transfer relation.

$$\text{Transfer Loss } C_{ext}\,\Delta V_P = Q_{Transfer} = C_{loop}\,\Delta V_{loop} \quad (3)$$

When current is demanded to change the loop voltage, some current is lost to overhead. The ratio of overhead current to the actual current delivered to the loop filter is referred to as the efficiency factor, Eff_Factor. The LMX2350 has sixteen charge pump current settings with each one having a different Eff_Factor. The Eff_Factor for the LMX2350 for each charge pump current setting is shown in *Figure 4*.

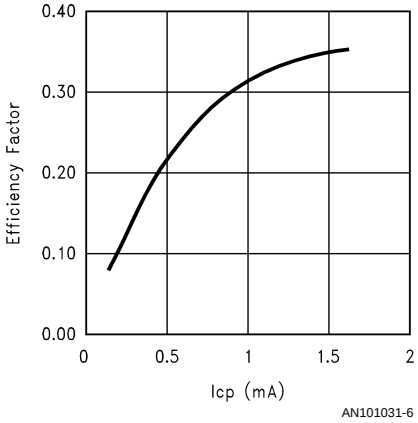



**FIGURE 4. LMX2350 Efficiency Factor vs. Icp**

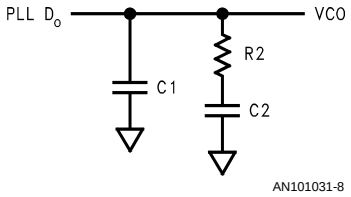
Cycle slipping will reduce the efficiency factor even further. Cycle slipping occurs when the VCO frequency does not change fast enough causing the two phase detector inputs to slip past each other. When this occurs the charge appears to be on 50% of the time.

The external capacitor, $C_{ext}$ connected to voltage doubler $V_P$ pin can be found using *Equation (4)*.

$$C_{ext} = \frac{\Delta V_{loop}}{\Delta V_P} C_{loop} \frac{1}{0.5 Eff\_Factor} \quad (4)$$

$V_{loop}$ is chosen to be the entire tuning range voltage.

The loop filter capacitance, $C_{loop}$, is found by adding C1 and C2 (assuming the internal VCO capacitance is much less than C1) as shown in *Figure 5*.




$C_{loop}$ = C1 + C2

**FIGURE 5. Loop Filter**

### $V_P$ Charge Time

The voltage doubler must be allowed to precharge before the charge pump is enabled. When using the LMX2350, the charge pump must be tri-stated by powering down the RF side via the internal register bit, to allow the external capacitor to precharge. The LMX2350's voltage doubler will be operational as long as the external RF enable pin is high, and the crystal oscillator input is present.

The voltage doubler must also be allowed to recover between frequency changes. As discussed in the previous section a frequency change will result in a $V_P$ voltage droop. The voltage doubler must recharge the external capacitor back to its steady state voltage before another frequency change can occur.

The amount of time it takes the voltage doubler to charge the external capicator can be determined using the simple RC time constant from *Figure 2*. Where C is the external capacitor and R is the switched capacitor equivalent resistance, found using *Equation (1)*. The LMX2350 has an internal capacitor of 36 pF (picofarads). *Equation (5)* calculates the time required for the external capacitor to charge to 98% of its maximum voltage.

$$t = 5\tau = 5R_{equiv}C_{ext} = \frac{5C_{ext}}{C_{int}F_{clock}} \qquad (5)$$

### SUMMARY

When low operating voltages are required, a voltage doubler can increase the VCO tuning range. There are three factors that will set the maximum tuning voltage. The first limiting factor is the steady state voltage loss resulting from some average load current when locked. *Equation (2)* is used to approximate the steady state voltage loss. The second limiting factor is dynamic $V_P$ droop voltage as a result of switching PLL frequencies. The third limiting factor for the VCO tuning range is the charge pump output voltage range, which is a fixed 0.5V below the charge pump supply voltage, $V_P$. The only limiting factor that can be set is the dynamic $V_P$ droop voltage. Once the dynamic $V_P$ droop voltage is determined, the external capacitor is calculated using *Equation (4)*. One last consideration when using a voltage doubler is to determine the charge time of the external capacitor as a result of completely powering down the RF PLL and charge time required to recover from a $V_P$ droop after changing frequencies. The charge time can be found using *Equation (5)*.

### EXAMPLE

**Voltage Doubler Design Parameters**

$V_{CC}$ = 3.0V

$C_{loop}$ = 11 nf

VCO Tuning Range = 0.5V to 4.0V

$OSC_x$ (RF Oscillator Frequency) = 14.4 MHz

$I_{cp}$ (Charge Pump Current) = 900 µA

$F_{pd}$ (Phase Detector Frequency) = 30 kHz

$\Delta V_P$ (Maximum Allowable Droop) = 1V

**I. Calculate Steady State $V_P$ Level**

$$V_{SS} = 0.3 - \frac{F_{pd}(MHz)[2 + 4Icp(mA)]}{OSC_{in}(MHz)}$$

$$V_{SS} = 0.3 - \frac{0.03 \times [2 + 4 \times 0.9]}{14.4} = 0.29V$$

**II. Calculate $C_{ext}$**

$$C_{ext} = \frac{\Delta V_{loop}}{\Delta V_P} C_{loop} \frac{1}{Eff\_Factor} 2$$

$$C_{ext} = \frac{4}{1} \times 11e^{-9} \times \frac{1}{0.3} \times 2 = 290e^{-9}F$$

**III. Determine $V_P$ Charge Time**

$$t = 5\tau = 5R_{equiv}C_{ext} = \frac{5C_{ext}}{C_{int}F_{clock}}$$

$$t = \frac{5 \times 290e^{-9}}{36e^{-12} \times 14.4e^{6}} = 2.8e^{-3}s$$

**Measured Results**

- Max. Tuning Voltage 6–0.3–0.8–0.5 = 4.4V
  (6 = 2x 3V; 0.3 = $V_{SS}$; 0.8 = max. droop during frequency changes, 0.5 = suggested fixed voltage below $V_P$)
- Switched Capacitor Settling Time ≈ 3 mS
- ≈ 30/1 Ratio between $C_{loop}$ and $C_{ext}$ 0.3 µF/11 nF

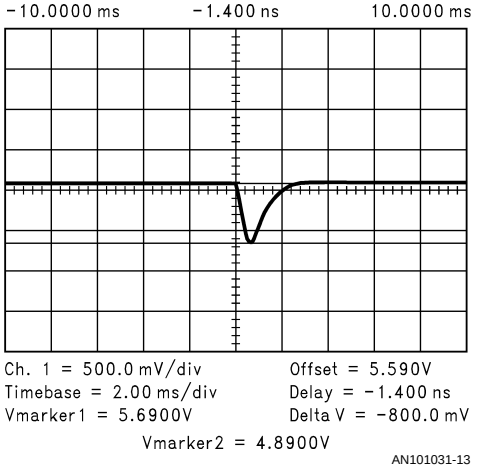



**FIGURE 6. Measured Voltage Droop**

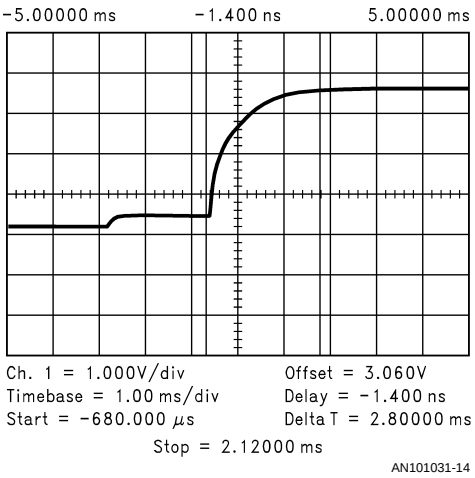



**FIGURE 7. Measured Initial $V_P$ Charge Time**



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