Using High Speed Differential Amplifiers to Drive Analog to Digital Converters

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Selecting The Best Differential Amplifier To Drive An Analog To Digital Converter

The right high speed differential amplifier will add flexibility to signal chains that include a high speed Analog to Digital Converter (ADC). A differential amplifier can provide signal conditioning such as single ended to differential conversion, impedance transformation, and gain or attenuation.

ADCs are normally fixed gain devices that provide best performance when driven with signals that are just below, but not above, full scale. Digitizing small signals that have an amplitude measured in single digit multiples of the Least Significant Bit (LSB) introduces distortion. Likewise, driving an ADC beyond full scale will cause distortion. An op amp can be used to scale the signal to the best amplitude range for the ADC. The CLC5526 is a variable gain differential amplifier designed to provide both gain and attenuation when driving a high speed ADC. When controlled by a micro-controller, 42 dB of increased dynamic range can be achieved. The LMH6550 offers low distortion, DC coupling, DC offset selection and fixed gain. Both of these amplifiers can provide low impedance, high compliance drive capability when matched with a high speed, CMOS analog to digital converter, such as the ADC12DL065.

When choosing which amplifier to use for driving an ADC it is very important to first define the system requirements. Some key parameters to consider are bandwidth, distortion, balance error, and settling time. Distortion will usually be the determining factor for wideband signals. On the other hand, for narrow band signals, bandwidth will drive the selection because distortion can be removed by the DSP. Narrow band signals are characterized by inter-modulation and harmonic distortion products that fall out of band, while in a wideband signal many products will fall in band. A more detailed selection criteria, based on the signal and ADC characteristics, will be described later.

First a quick review of some ADC basics. As hybrid devices, ADCs include both analog and digital circuits. The digital portion of the ADC works at a clocked sample rate (F_S) that is normally fixed for a given application. The sample rate determines a number of key operating characteristics as detailed in the following. When creating a digital representation of a signal, an ADC follows the Nyquist Sampling Theory. The Nyquist Theory states that a signal needs to be sampled at a rate that is at least twice the highest frequency contained in the signal. This defines a Nyquist band that is the sampling rate divided by 2 ($F_S/2$). In practise this results in the formation of “alias” signals. Alias signals are signals that appear to the ADC to be a different frequency than they really are. Alias signals may or may not be desirable, but they must be factored into the system design. For an illustration of aliasing refer to *Figure 1*, where a frequency domain graph shows sampling effects. Depending on the application, alias signals can be either noise or the desired signal. Analog filtering, as well as proper selection of sampling and signal frequencies, can eliminate distortion caused by aliasing.

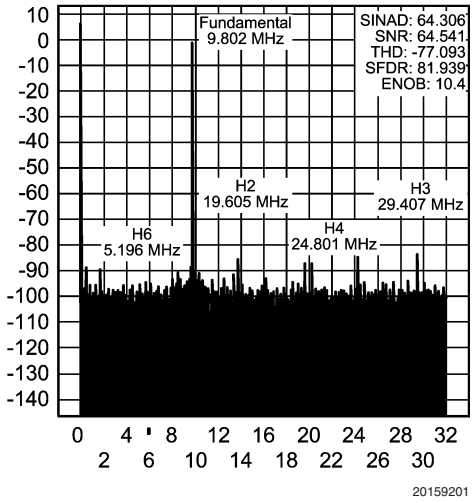


FIGURE 1. Nyquist Operation (Note how harmonic energy folds back into the Nyquist band) (LMH6550 driving ADC12L080, F_S = 64 MHz, Signal = 9.8 MHz)

Nyquist Operation

The classic and probably most familiar application of analog to digital converters is the Nyquist application. In this case the signal is fully contained between DC and half of the ADC sampling rate ($F_S/2$). The Nyquist theory sates that a signal must be digitized with an ADC that has a sampling rate of at least twice the highest frequency component of the sampled signal (note this does not apply to the carrier of a modulated signal, only the information bearing portion of the signal). For example, to digitize voice data for a phone conversation with desired data contained in the 300 to 3000 Hz range an ADC with a minimum of 6 kHz sampling rate could be used. In the United States, telephone conversations are digitized at an 8 kHz rate with a resolution of 8 bits. Although Nyquist operation is the least demanding scenario for the ADC, it makes the anti-alias filter very critical to system performance. Likewise the driving amplifier will be given very stringent criteria for Nyquist operation. The amplifier should have a 0.1 dB bandwidth of at least half of the sampling frequency. The amplifier and ADC should also have comparable distortion and noise performance up to half of the sampling frequency. If the amplifier is to be used as an active filter, then the amplifier –3 dB bandwidth should be close to two times the sampling frequency or more. In general for Nyquist operation, the amplifier and the ADC should have comparable specifications for all parameters at frequencies of $F_S/2$ and below. A fixed gain amplifier such as the LMH6550 is ideal for DC coupled signals or wide band signals under 50 MHz that require buffering, small amounts of fixed gain and exceptional signal purity. The LMH6550 can also eliminate the need for a transformer for single ended to differential conversion.

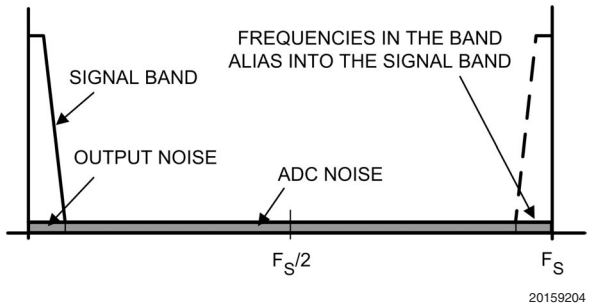


FIGURE 2. Over-Sampling (Sampling Frequency is ~6x Over Nyquist)

OVER-SAMPLING

Rapidly advancing ADC technology has given rise to a very powerful option for the signal chain designer. Modern ADCs are so fast that they can be clocked far faster than the signal bandwidth would require. This is called over-sampling. To operate in over-sampling mode the signal band is, by definition, far smaller than $F_S/2$. In order to quantify the degree of over-sampling divide, $F_S/2$ by the signal bandwidth. In *Figure 2* the degree of over-sampling is approximately six. The higher the degree of over-sampling, the lower the requirements are on the analog filter which precedes the ADC. Another key benefit is that a driving amplifier will need to match the ADC specifications only in the signal band.

One of the key benefits of over-sampling is the subsequent digital filtering. The entire zone between the upper frequency limit of the signal and $F_S/2$ is available for digital processing. Digital filtering has the advantages of being easily tuned, very accurate and very high order filters can be realized. This gives rise to a processing gain. Processing gain is the improvement in the signal-to-noise ratio obtained by digital signal processing in the DSP. Since nearly all of the noise outside the signal band can be removed by digital filtering, the processing gain is approximately equal to the degree of over-sampling. For example a system with signal bandwidth of 6 MHz and a sampling rate of 24 MHz would have a 2x over-sampling rate which would give up to a 6 dB gain in signal-to-noise.

One thing the DSP will not be able to remove is noise in the signal band. Careful selection of gain set and feedback resistors will help to keep the noise added by the amplifier to a minimum.

SUB-SAMPLING

Sub-sampling uses the sampling mechanism of the ADC to work like an analog mixer. Non-linear mixing is a very old technique made popular by the heterodyne or super-heterodyne receiver.

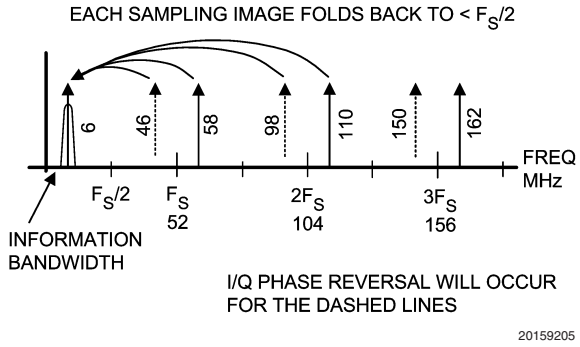


FIGURE 3. Sub-Sampling (Signal presented to the ADC front end at any of the arrows will alias to 6 MHz)

As shown in *Figure 3*, if the ADC front end has enough bandwidth, the ADC can be used to mix signals down from higher frequencies. In this example the sampling frequency is 52 MHz. An IF frequency of 150 MHz would mix down to 6 MHz. Even though the carrier frequency is reduced, the information bandwidth and content is entirely unchanged, EXCEPT, that the phase will be reversed (i.e. shifted 180 degrees – more specifically, the real and imaginary frequency components are swapped) for frequencies represented by dotted lines in *Figure 3*.

Sub-sampling is nearly always used in an over-sampled configuration, where the signal bandwidth is far less than $F_S/2$. With careful selection of IF frequency and sampling frequency, the DSP that follows the ADC can remove most of the distortion introduced by the analog signal chain, as well as, most of the distortion contributed by the ADC. This results in the same benefits described in the section on over-sampling. This is very important because at higher carrier frequencies a higher anti-alias filter Q is required for

Nyquist Operation (Continued)

the same amount of filtering with respect to $F_S/2$ and the signal bandwidth. Without over-sampling, sub-sampling would be impractical.

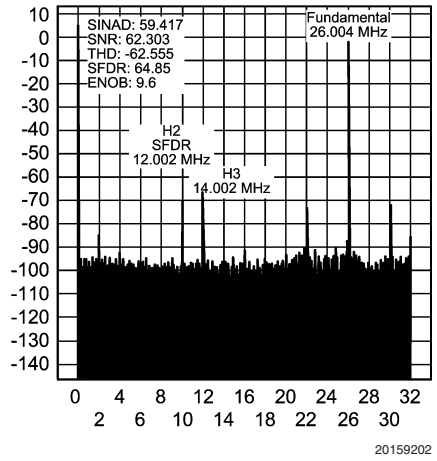


FIGURE 4. Sub-Sampling Operation near $F_S/2$ Sampling Frequency = 64 MHz, Signal = 38 MHz (6 MHz higher than $F_S/2$; 32 – 6 = 26 MHz)

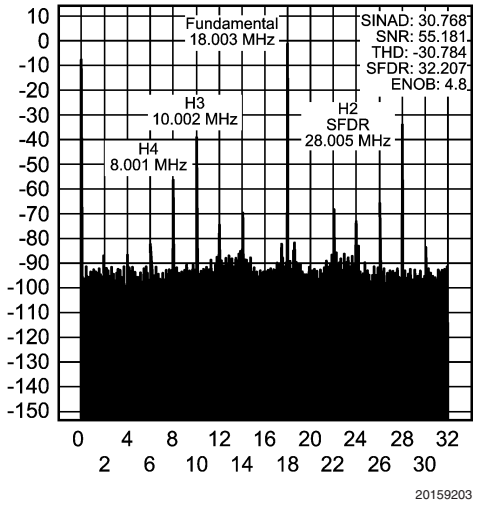


FIGURE 5. Sub-Sampling Operation Signal = 146 MHz, Sampling Frequency = 64 MHz, ($F_S/2$ * 4=128, 146 – 128 = 18 MHz) (LMH6550 Driving ADC12L080)

Looking at *Figure 5*, it would appear that the illustrated system would perform poorly with an SFDR of only 32 dB. However, there is a band of clear spectrum from 10 to 28 MHz with an SFDR of 65 dB, and a smaller band with SFDR of over 80 dB. For a GSM system, only 200 kHz of bandwidth is required. A simple two pole LC filter between the amplifier and the ADC would reduce the H2, H3 and noise contributed by a driving amplifier. Digital signal processing can remove much of the distortion.

Amplifier Specification, Key Parameter Tables

NYQUIST OPERATION – LOWPASS ANTI-ALIAS FILTER

Amplifier Specification	Amplifier Requirement
Bandwidth (0.1 dB)	Sampling frequency/2
H2 and H3	~20 * log(1/(2^(number of bits)))
Balance error	~ADC LSB at ½ sampling frequency
Settling time	~0.5 * 1/sampling frequency
Noise	~Noise floor of ADC to 6 dB better

OVER-SAMPLING OPERATION

Amplifier Specification	Amplifier Requirement
Bandwidth (0.1 dB)	Signal bandwidth (<< sampling frequency)
H2 and H3	Requirements relaxed by filtering provided they do not fall in band
Balance error	< ADC LSB at maximum signal bandwidth
Settling time	~0.5 * 1/signal bandwidth >> 1/ sampling frequency

SUB-SAMPLING OPERATION

Amplifier Specification	Amplifier Requirement
Bandwidth (3 dB)	>Signal bandwidth (>> sampling frequency)
H2 and H3	Requirements relaxed by filtering provided they do not fall in band
Balance error	Requirements relaxed by filtering
Noise	Requirements relaxed by filtering

Connecting The Amplifier To The ADC

Analog to digital converters often present challenging load conditions. They typically have high impedance inputs with large and often variable capacitive components. As well, there can be current spikes associated with switched capacitor or sample and hold circuits. This makes an ADC input a challenge to drive, and is where an amplifier can provide value. The output stage of a differential amplifier can help to

Connecting The Amplifier To The ADC (Continued)

smooth out current spikes as well as provide a low impedance, fast settling source for accurate sampling. *Figure 6* illustrates a typical circuit for driving an ADC. The two 56Ω resistors serve to isolate the capacitive loading of the ADC from the amplifier to ensure stability. In addition, the resistors form part of a low pass filter, which helps to provide anti-alias and noise reduction functions. The two 39 pF capacitors help to smooth the current spikes associated with the internal switching circuits of the ADC and also are a key component in the low pass filtering of the ADC input. In the circuit used to generate *Figure 4*, the cutoff frequency of the filter is 1/(2*π*56Ω *(39 pF + 16 pF)) ≅ 52 MHz (which is slightly less than the sampling frequency). Note that the ADC input capacitance must be factored into the frequency response of the input filter, and that fir a differential input, the effective input capacitance is doubled. Also, the input capacitance of many ADCs is a function of the ADC conversion cycle (sample vs. hold). *See the datasheet for your particular ADC for details.* In the example the sample capacitance was used.

With all high-speed circuits, board layout is critical. The amplifier and ADC should be located as close together as possible. Both the amplifier and the ADC require that the filter components be in close proximity. The amplifier needs to have minimal parasitic loading on the output traces and the ADC is sensitive to high frequency noise that may couple in on its input lines. In addition the ADC digital outputs should be well isolated from the ADC input as well as the amplifier inputs. The amplifier and the ADC input pins should not be placed over power or ground planes. Power supply bypass capacitors should be low ESR and placed within 2 mm of the associated pins. It is also a good idea to use multiple vias when they must be used.

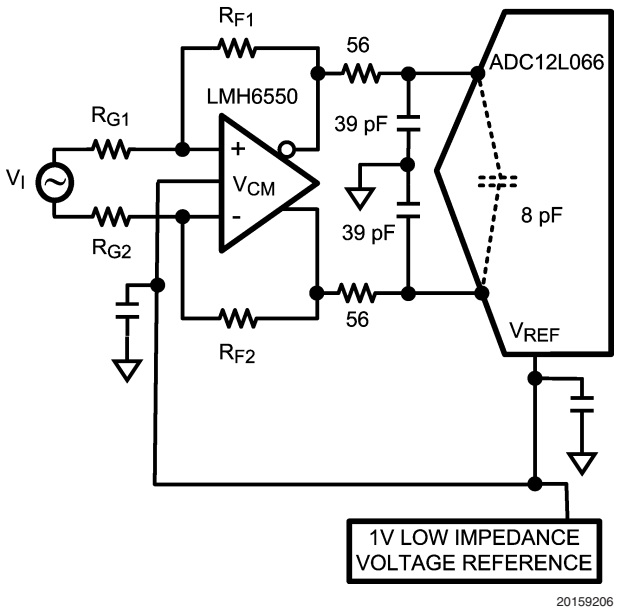


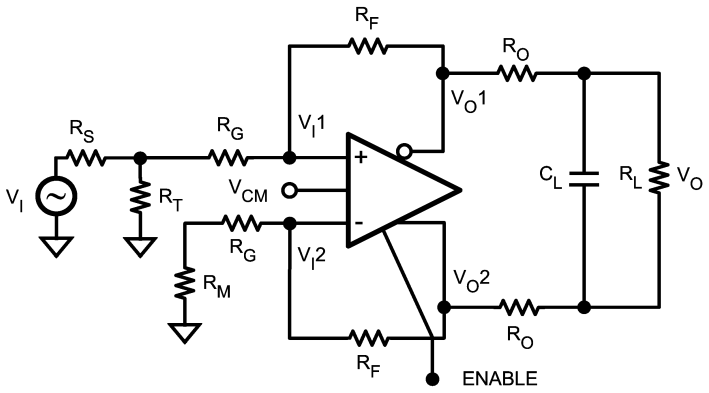
FIGURE 6. Driving an ADC (LMH6550 Driving an ADC12L066)

Common Mode Feedback

One of the key benefits of a common mode feedback circuit for a differential amplifier is the ability to set the precise level of the output common mode voltage. For most ADCs the common mode voltage must be set to a particular value to realize full dynamic range. Since a differential amplifier, by nature, only amplifies the difference of the inputs, the output common mode can be set independently with no impact on the gain or the differential output signal. Amplifiers such as the LMH6550 have a high impedance input for the output common voltage buffer (V_{OCM}). This allows the amplifier to use the reference voltage output of most ADCs with a buffered V_{REF}output. For ADCs without a buffered reference pin an external reference may be used for both devices.

The other benefit of a common mode feedback circuit is when an amplifier needs to create a fully differential signal from a single ended source. The common mode feedback circuit, in essence, creates the missing out of phase input signal. It also balances the two differential output stages, around the desired common mode point. This allows a very accurate differential signal to be created from a single ended source.

Common Mode Feedback (Continued)



$$*V_{CM} = \frac{V_O1 + V_O2}{2} \quad *\text{BY DESIGN}$$

$$V_{ICM} = V_{OCM} * \frac{(R_G + R_M)}{(R_G + R_M + R_F)} = \sim \frac{V_{OCM}}{1 + A_V} \quad \text{WHERE } R_M << R_G$$

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FIGURE 7. DC Operating Points

It is important to note that a common mode feedback circuit looks like a unity gain buffer with respect to the input pin of the buffer and the output common mode voltage operating point. The equation is V_{OCM} = (V+OUT + V-OUT)/2 , which is shorthand for saying that the outputs will have exactly equal magnitude and opposite phase with respect to the output common mode voltage (V_{OCM}). *Figure 7* shows a typical configuration for single supply operation and gives equations to calculate the effect of the common mode feedback network. In this example, V_{CM} is the input to the common mode feedback buffer. VOCM is the output common mode, or the output of the common mode feedback buffer. When using a differential amplifier with single supplies (0V and +5V, instead of ±5V for example) the input common mode operating point will end up being one of the key limitations to system design. Both gain and output common voltage settings will be limited in single supply operation.

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