National Semiconductor's Simple Switcher® Power Modules and EMI

National Semiconductor
Application Note 2052
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April 26, 2010

Power supply design, even the design of common DC to DC switching convertors can present a number of challenges; this is especially true with higher power designs. Beyond the functional issues, an engineer must make sure the design is robust, meets the required cost targets and thermal and space constraints all while staying on schedule. Additionally, and hopefully not as an afterthought, the design must produce sufficiently low Electromagnetic Interference (EMI) both for reasons of product compliance and system performance. However, a power supply's EMI level is one of the more difficult aspects of the design to accurately predict. Some might even argue that it's simply impossible and the best a designer can do is take sufficient care in the design especially in the layout.

While the principles discussed in this article apply more broadly to power design, we're going to focus on DC to DC convertor design given its broad application. It affects virtually every hardware engineer who at some point has to design a power convertor. In this article we'll consider two common trade-offs related to low EMI design; thermal performance and EMI and also solution size related to PCB layout and EMI. We'll use a simplified buck convertor as our example, shown in *Figure 1*.

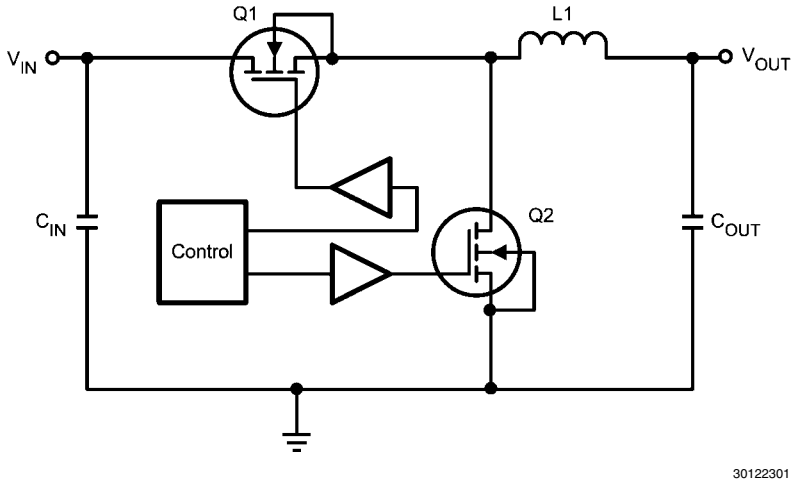

FIGURE 1.

Both radiated and conducted EMI are measured in the frequency domain and that is really nothing more than a Fourier series of a given waveform. We'll focus our attention on radiated EMI for this article. The dominant switching waveforms generating EMI in a synchronous buck convertor are generated by Q1 and Q2; namely the d_i/d_t flowing drain to source in each MOSFET during their respective on time. The current waveforms ($Q1_{on}$ & $Q2_{on}$), as shown in *Figure 2*, are not classically trapezoidal in shape, however, we can take a few liberties since the inductor current transitions are relatively slow allowing the application of *Equation 1* from Henry Ott's classic Noise Reduction Techniques in Electronic Systems. We see that the rise and fall time of a waveform like these directly affects the harmonic amplitude or the Fourier coefficient (I_n).

$$I_n = 2Id \text{ Sin } (n\pi d)/n\pi d \text{ x Sin } (n\pi t_r/T)/n\pi t_r/T \quad (1)$$

Where n is the harmonic number, T is the period, I is the p-p current amplitude of the waveform, d, the duty cycle and t_r is the shortest of either t_r or t_f.

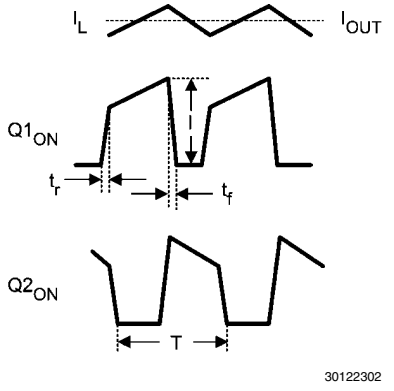

FIGURE 2.

In reality you will most likely have odd and even order harmonic emissions. A wave form must have a precise 50% duty cycle to generate only odd order harmonics. Real world waveforms rarely, if ever, have that kind of dutycycle precision.

The EMI amplitude of the harmonics series is affected by the turn-on and turn-off of Q1 and Q2. This can be seen in measuring the V_{DS} t_r and t_f across or d_i/d_t through Q1 and Q2. This

would imply that we could reduce the EMI levels by simply slowing down the turn-on and turn-off of Q1 and or Q2. This in fact is true and slowing down these switching times has a greater affect on harmonics above f = $1/\pi t_r$. The trade-off, however, is increased heat dissipation as the transition losses increase. Nonetheless, adding some control to these parameters is a good idea in order to strike a balance between EMI and thermal performance. This can be done by adding a small amount of resistance, typically < 5Ω, in series with the gate of Q1 and Q2 to control tr and tf. You can also add a "turnoff diode" in parallel with the gate resistor to independently control the t_r or t_f transitions, *Figure 3*. This effort is an iterative process and even the most seasoned power designers go through it. The end goal is to reduce the EMI level to an acceptable level by slowing down the transistors while at the same time keeping them cool enough to be reliable.

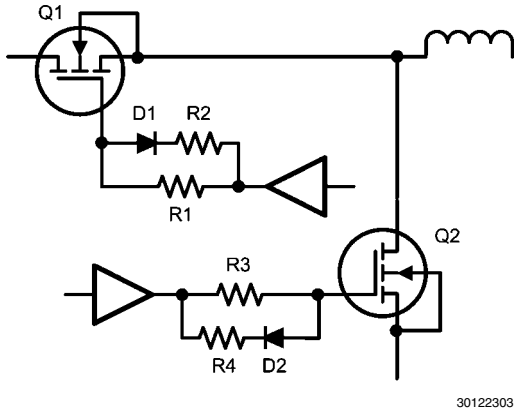

FIGURE 3.

The physical loop area of the switch nodes also plays a significant role in the resulting EMI levels. Typically a designer wants to make the design as compact as possible given that PCB real estate is rarely a luxury. However, many designers don't know which portion of the layout is EMI critical. Going back to our buck regulator example there are two loop nodes, (*Figure 4* & *Figure 5*) the size of which have a direct affect on EMI levels.

Ott's equation (*Equation 2*) for differential mode EMI level shows the direct and linear affect that loop area has on a circuit's EMI level.

$$E = 263 \times 10\text{-}16\ (f2AI)(1/r) \qquad (2)$$

The radiated field is proportional to the frequency (f) of the harmonic of interest in Hz, loop area (A) of the net in m2, the current (I) and the measured distance (r) in m.

This concept has application to all circuit designs employing trapezoidal waveforms, though we will limit our discussion here to power design. Let's consider the AC model, in *Figure 4*, for current flowing through the loop starting at the input capacitor then flowing through Q1 while it's on, through L1 into the output capacitor and returning to the input capacitor.

The second loop is formed when Q1 turns off and Q2 turns on. The energy stored in L1 then flows through the output capacitor and Q2 as seen in *Figure 5*. Control of these loop areas is essential to controlling EMI and begins with careful parts placement with forethought to the routing of your PCB traces. But, of course, there's a practical limit as to just how small a loop area can be obtained.

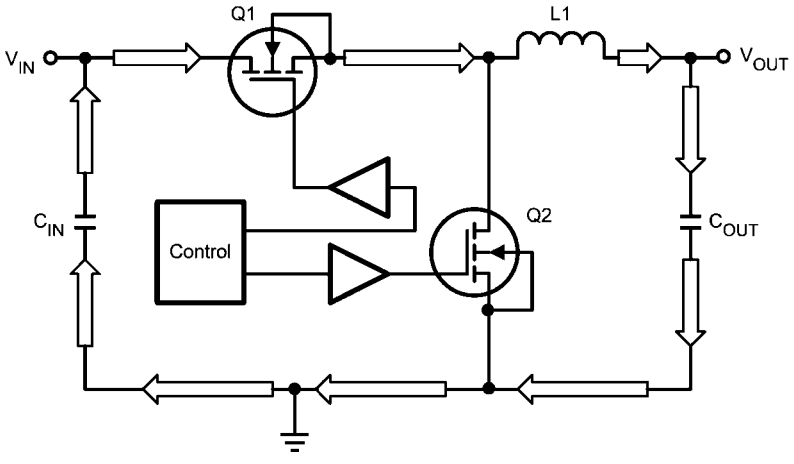

FIGURE 4.

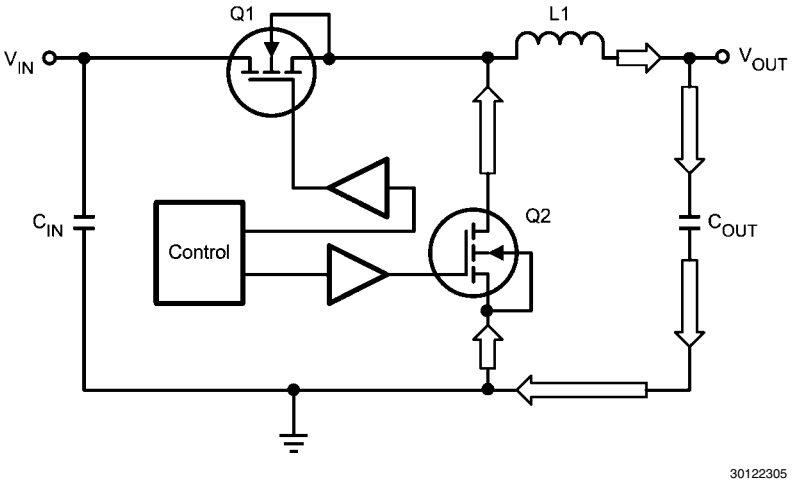

FIGURE 5.

From *Equation 2* we can see that reducing the loop area of a switch node can translate into large improvements in the measured EMI level. Reducing the loop area by a factor of 3 will result in an EMI reduction of 9.5dB, a factor of 10 results in 20dB of improvement. There are additional PCB layout guidelines for DC to DC convertors in application note AN-1229 available at www.national.com . It's best to start with the goal of minimizing the loop area of the two loop nodes noted in *Figure 4* & *Figure 5*. Begin with careful parts placement with an eye to routing copper. Avoid the temptation to use both sides of the board as vias add significant inductance and thus other problems.

Often overlooked is the importance of proper placement of the high frequency input and output capacitors. Some years ago the company I worked for transferred the design of our products to an off-shore manufacturer. As a result my role changed to largely that of a consultant which included helping the new power designer through the trade-offs mentioned here as well as a few more. This was an off-line switcher design with integrated lamp ballast and it was in this final power stage that he struggled to reduce the EMI. I simply moved a high frequency output capacitor closer to the output stage reducing the loop area by about half and we realized an EMI reduction of about 6dB. The designer, not really understanding the principles at work, called that capacitor the "magic cap," yet all that really happened was we shrunk the loop area of the switch nodes.

The obvious issue related to what we have discussed so far is that the cure may be worse than the illness. In other words the thermal problems resulting from slowing down the transition times in order to pass EMI could now be the big problem. One solution to controlling EMI as described is to use fully integrated power modules in place of traditional DC to DC convertors. Power modules are complete switching regulators with fully integrated power transistors and inductor and are as easy to design in as a linear regulator. The loop area of module's switch nodes is much smaller than a comparable discreet regulator or controller design. Power modules aren't new and have been around for some time. But until now, a couple of the things plaguing modules have been their inability to effectively remove heat from the package and the difficulty in reworking a module once it's mounted.

National Semiconductor's new SIMPLE SWITCHER® Power Modules provide the designer a low EMI alternative while also addressing traditional issues with power modules. This is accomplished in part by packages more often associated with power components than modules. As an example the LMZ10505, a 5A module with a Vin Max of 5V, comes in a 10mm x 10mm package with a relatively large 8.5 x 6.4mm thermal die attach pad from which the heat can be easily transferred to ground plane making the need for cooling airflow optional. Thermal and EMI problems no longer have to be the inherent trade-off in solving your power problem. So while the EMI solutions discussed in this article will work for any power design, it takes time to find the correct balance. Even seasoned power designers spend considerable time placing components, let alone routing traces for a power design and will never achieve the compact size afforded by these power modules. The advanced packaging techniques used on the SIMPLE SWITCHER® Power Modules allow for switch node loop areas that are far smaller than otherwise possible. The benefit found from decreased loop area, of course, scales beneficially as the output current increases.

National has also addressed the rework issue common in other power modules, by utilizing rework friendly packaging. Additionally, parts are pin compatible within a family; LMZ10503/04/05, LMZ12001/02/03 and LMZ14201/02/03 allowing the designer to replace parts as needed. The part numbers are intuitive with the last two digits denoting the rated output current and the two previous digits denoting the rated input voltage.

Notes

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