Optimizing Feedforward Compensation In Linear Regulators

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Introduction

All linear voltage regulators use a feedback loop which controls the amount of current sent to the load as required to hold the output voltage at the correct regulated value. The feedback loop is compensated to provide adequate phase margin at the frequency where the loop gain crosses unity (zero dB).

In cases where the output voltage is adjustable, and set by an external resistive divider, a compensation technique called *feedforward* can be employed which can increase phase margin by producing phase lead which cancels out some of the phase lag from the internal poles. It should be noted that not all linear regulators require feedforward compensation, but this application note explains the technique for those that will benefit from it (and most will).

Linear Regulator Loop Basics

All linear voltage regulators use a similar control topology (see *Figure 1*).

A pass transistor device is used to source current to the load. The error amplifier controls this current in response to the output's feedback voltage appearing at the junction of R1 and R2. The action of the loop is such to always force the voltage at the error amplifier's input terminals to be equal to the fixed reference voltage. In this way, the control loop holds the output at the nominal voltage, which is given by:

$$V_{OUT} = V_{REF} (1 + R1/R2)$$

Loop Compensation

The control loop is usually compensated locally at the error amplifier, and in some cases, also by using the ESR of the output capacitor to add some positive phase lead. In most "adjustable output" linear regulators (where the resistors R1 and R2 are external to the IC), a capacitor can be placed across R1 to add feedforward compensation which will also add phase lead.

R1, R2, and C_{FF} form a pole-zero pair, where the zero will always be at a lower frequency than the pole. The frequency of the pole-zero pair is given by:

$$F_{ZERO} = 1 / 2 \times \pi \times C_{FF} \times R1$$

$$F_{POLE} = 1 / 2 \times \pi \times C_{FF} \times (R1 // R2)$$

It should be noted that it is only the zero which adds beneficial phase lead, the pole adds phase lag which tends to cancel out the lead. To improve phase margin, the pole-zero pair must be positioned at the frequency where the zero adds maximum lead and the pole gives minimum phase lag at the unity gain frequency. The net positive phase lead obtained is the difference between these two values at the unity-gain point.

It follows from this that maximum benefit is derived when the pole-zero pair are far apart (which occurs when R1 >> R2). As R1 gets smaller and smaller, the pole frequency moves closer to the zero frequency, eventually canceling out when R1 = 0.

Therefore, the higher the ratio of R1/R2 is, the farther the pole and zero are separated and the more potential phase lead can be obtained. This means that feedforward compensation is more effective when the output voltage is set to higher ratios of the reference voltage (since it is the ratio of R1/R2 that is important, not the actual output voltage). A graphical illustration of this is shown in *Figure 2* which shows the maximum positive phase lead which can be obtained for selected ratios of R1/R2:

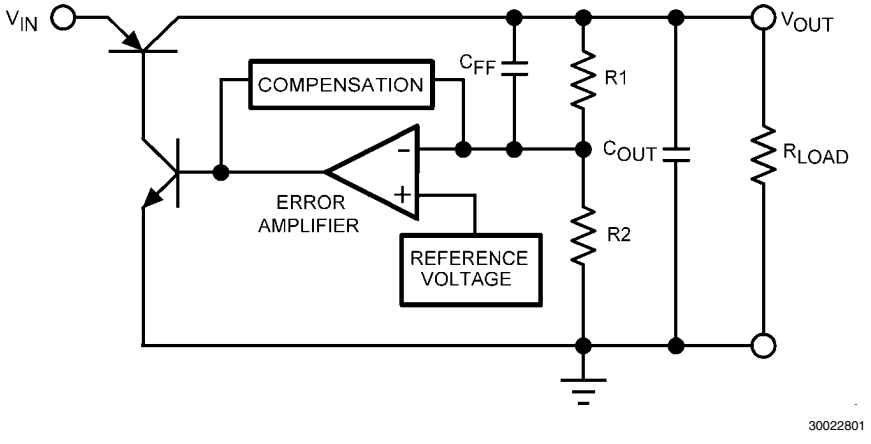

FIGURE 1. Basic Linear Regulator

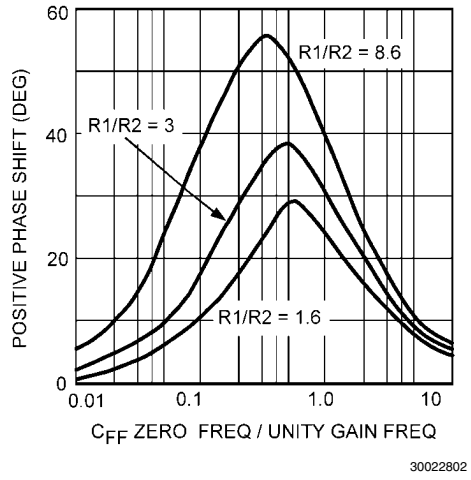

FIGURE 2. Feedforward Phase Lead For Various R1/R2 Ratios

What is important to note is that as the ratio of R1/R2 is reduced, not only does the maximum possible phase lead reduce, but the effective range over which it can be obtained also gets narrower. This points out an unavoidable fact: feedforward compensation works better at higher output voltages, and it's effect is limited at lower voltages. However, it can still improve stability and settling time even when the added phase margin is as little as 10 - 15 degrees.

The placement of the zero frequency with respect to the unity-gain frequency is what maximizes the phase lead provided by C_{FF}. As can be seen, the peak effect from C_{FF} is typically obtained when the zero is centered at approximately 0.3 to 0.6 times the unity-gain frequency.

As a ballpark figure, a good starting point for the feedforward zero frequency for most linear regulators is in the range of about 30kHz to 100kHz.

But, regulator bandwidths vary depending on process type and design topology. Also, many linear regulators have loop bandwidths which change with load current. Because of these reasons, best performance is obtained when C_{FF} is dialed in for the specific application by actual bench testing which allows fine tuning of the value of C_{FF} to maximize the amount of phase lead generated at the unity-gain frequency.

Optimizing Feedforward Compensation

The goal of adding feedforward compensation is to increase the phase margin, defined as the difference between the unity-gain phase shift and -180 degrees, which is the point where the loop becomes unstable. This means that a design with 20 degrees of phase margin has a total phase shift of -160 degrees at the unity gain frequency. The obvious way to know the amount of phase margin is to measure the loop gain/phase directly. One technique to do this is to break the loop and use signal injection to read the loop gain/phase as shown in *Figure 3*.

In the circuit shown, the feedback loop is broken at the top of R1. A ten Ohm resistor is inserted, which is used by the spectrum analyzer to force an AC signal into the loop. The amplitude of the signal is measured at the top and bottom of the resistor, and the ratio of the magnitudes defines the loop gain at that frequency. The spectrum analyzer also measures the phase shift between the two signals, which it uses to calculate the phase margin.

This method is often used, but it has some disadvantages: it is time consuming to set up, and it is often hard to get repeatable measurements because many variables affect the data (calibration of the instrument, frequency characteristics of the probes and isolation transformer). An indirect measurement called Load Step testing is much simpler, and gives very reliable data for optimizing compensation.

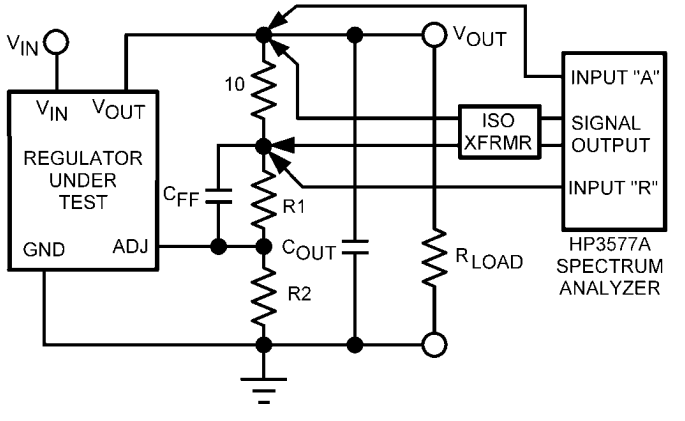

FIGURE 3. Loop Gain/Phase Measurement System

Load Step Testing

Load step testing is a method where the load current is abruptly changed from one level to another, which requires the control loop to correct for the change. Watching the output voltage behavior during a load step gives a very accurate indication of phase margin, and can be used to tune the compensation.

In general, the amount of ringing seen on the output after a load step will increase as phase margin is reduced. It follows that optimizing the compensation for minimum ringing and shortest "settling time" on the output will give best phase margin.

Since most regulators have increased bandwidth at higher values of load current, the load step test method most frequently used is to change the load current from minimum value to maximum (for the application) as quickly as possible. One way to do this is shown in *Figure 4*.

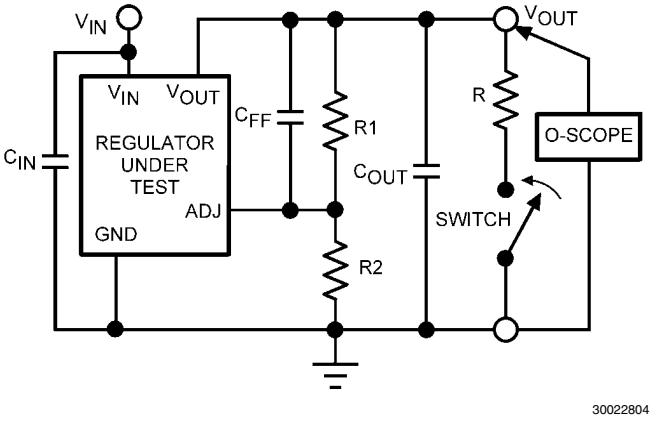

FIGURE 4. Load Step Test Circuit

Important to note for testing:

1. Select "R" for the maximum load current for the application.
2. C_{IN} must be a low ESR, good quality capacitor to prevent ringing of the V_{IN} source voltage which will be reflected to the output during the load step test and give false data. A Tantalum or Oscon electrolytic is a good choice, with a value of at least 47µF. For best results, parallel it with a good quality ceramic whose value is greater than 1µF to assure very low source impedance for testing.
3. The switch can be any mechanical contactor switch which can make a sharp, fast connection without bounce. Clip lead ends can be used.
4. An N-FET can be used for the switch, but typically does not give current rise times which are as fast as using mechanical contacts
5. The scope should be set on single-event trigger to sweep on the falling edge of the output voltage waveform. The typical time duration of such transients in linear regulators can range from a few microseconds to tens of microseconds. Most will not exceed 50 microseconds.

When the load current abruptly increases (the instant the switch is closed) the output voltage will fall, then the loop corrects and turns on the power device fully to force the output voltage back up to nominal. As the output voltage reaches the nominal value it will overshoot slightly and then settle out. A control loop with optimum compensation will show a transient response similar to *Figure 5*.

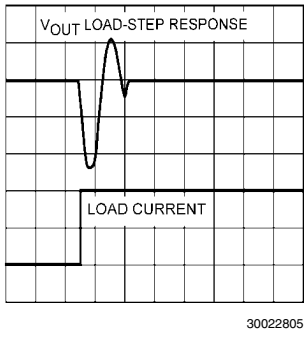

FIGURE 5. Optimum Output Voltage Transient Response

When phase margin is reduced, the output voltage will show increased ringing and an extended settling time as shown in *Figure 6*.

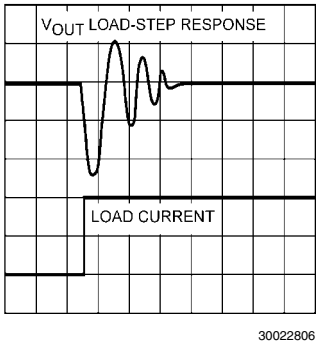

FIGURE 6. Sub-Optimum Output Voltage Transient Response

When optimizing the value of C_{FF}, it should be remembered that it has a limited effect on phase margin: not every regulator can have optimum transient response. In most cases, an output transient which extinguishes in less than three or four rings is acceptable. The best value of C_{FF} is the one that minimizes the amount of ringing, and gives the shortest settling time for V_{OUT}.

Notes

Notes

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