LP3884X-ADJ Evaluation Board

National Semiconductor Application Note 1457 Maurice Eaglin June 2006

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Introduction

The LP38841-ADJ and LP38842-ADJ are ultra low dropout linear regulators which provide adjustable output voltages and load currents up to 800 mA (LP38841) and 1.5A (LP38842). This document describes the evaluation board provided to demonstrate the performance of these parts.

Basic Application Circuit

The basic application circuit shown below reflects the electrical connections and component identifiers used on the evaluation board.



FIGURE 1. Basic Application Circuit Schematic

Capacitor C4 (Feedforward Compensation)

The feedforward capacitor C4 is used to provide increased phase margin. Any good quality X5R/X7R dielectric ceramic capacitor may be used. The value of capacitance for C4 depends on the value of R1. C4 may be calculated using the formula:

$$C4 = 1 / (2 X \pi X 70k X R1)$$

The value of C4 is calculated after R1 is selected to set the output voltage needed for the specific application.

Setting the Output Voltage

The first build of evaluation boards used R1/R2 values which set the output voltage to 1.2V. The nominal output voltage is easily changed by replacing R1. The formula which can be used to calculate the new value of R1 for a different output voltage is:

$$V_{OUT} = V_{ADJ} (R1/R2) + V_{ADJ}$$

Solved for R1:

$$R1 = (V_{OUT} - V_{ADJ}) / V_{ADJ} X R2$$

The evaluation board is shipped with a 5.62 $\mbox{k}\Omega$ resistor installed at R2.

Power Dissipation

Power dissipation must be limited so that the junction temperature does not exceed 125C. Power dissipation can be calculated using:

$$\begin{split} \mathsf{P}_{\mathsf{DISS}} = ((\mathsf{V}_{\mathsf{IN}} \text{ - } \mathsf{V}_{\mathsf{OUT}}) \mathbin{X} \mathsf{I}_{\mathsf{LOAD}}) + (\mathsf{V}_{\mathsf{IN}} \mathbin{X} \mathsf{I}_{\mathsf{Q}(\mathsf{V}_{\mathsf{IN}})}) + (\mathsf{V}_{\mathsf{BIAS}} \mathbin{X} \mathsf{I}_{\mathsf{Q}(\mathsf{V}_{\mathsf{BIAS}})}) \end{split}$$

In calculating junction temperature, a value of theta J-A (junction-to-ambient thermal resistance) of approximately 50C/W should be assumed for this board. Junction temperature (T_J) is calculated using:

$$T_J = P_{DISS} X \theta_{(J-A)} + T_{AMBIENT} = P_{DISS} X 50 + T_{AMBIENT}$$

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| Component List | |
|------------------------------|--|
| PCB | 551012613-001 Rev A |
| U1 | LP38842MR-ADJ |
| TP1, TP2, TP3, TP4, TP5, TP6 | test point terminal, NEWARK 97H6311 |
| VIN CONNECTOR | banana jack (RED): DIGI-KEY 108-0902-001 |
| VOUT CONNECTOR | banana jack (BLUE): DIGI-KEY 108-0910-001 |
| GROUND CONNECTOR | banana jack (BLACK): DIGI-KEY 108-0903-001 |
| S/D CONNECTOR | banana jack (YELLOW): DIGI-KEY 108-0907-001 |
| BIAS CONNECTOR | banana jack (GREEN): DIGI-KEY 108-0904-001 |
| R1 | resistor, 0805 case, 9.31 k Ω , 1% DIGI-KEY 311-(9.31K)CCT-ND |
| R2 | resistor, 0805 case, 5.62 k Ω , 1% DIGI-KEY 311-(5.62K)CCT-ND |
| R3 | R3: resistor, 0805 case, 51 k Ω , 5% DIGI-KEY 311-(51K)ACT-ND |
| C1 | ceramic capacitor, 0805 case, 0.1 μF , X5R/X7R dielectric: DIGI-KEY 478-3351-1-ND |
| C2 | ceramic capacitor, 10 µF, Taiyo-Yuden #LMK325BJ106MN |
| C3 | ceramic capacitor, 4.7 µF, Taiyo-Yuden # JMK316BJ475MD |
| C4 | ceramic capacitor 0805 case 220 pE X5B/X7B dielectric: DIGI-KEY 311-1123-1-ND |

PCB Layout Diagram(s)



FIGURE 2. Top View

LP3884X-ADJ Evaluation Board

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Notes

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