Replacing the CLC016 Reclocker with the LMH0026

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Introduction

The LMH0026 SD-SDI reclocker can replace the CLC016 reclocker in many applications. The LMH0026 and CLC016 are both reclockers designed to recover and retime data, primarily for the SMPTE 259M interface. Both reclockers are rated for industrial temperature range operation (-40°C to +85°C).

The LMH0026, the newer generation SDI reclocker, has advanced features and is pin compatible with the LMH0046 HD-SDI reclocker and the LMH0346 3G-SDI reclocker. This allows a forward migration path from SD to HD to 3G. The LMH0026 offers improved performance and extremely low output jitter (half the output jitter of the CLC016 at 270 Mbps). The LMH0026 also offers a lower supply voltage (3.3V), enabling system designers to migrate to lower-power designs. The LMH0026 provides a 37% power savings over the CLC016, with typical power of 330 mW in comparison with 525 mW for the CLC016.

Table 1 shows the key differences between the CLC016 and LMH0026.

TABLE 1. CLC016 and LMH0026 Key Differences

	CLC016	LMH0026
Power Supply (V_{CC})	5.0V	3.3V
Package	28-pin PLCC or TSSOP	20-pin e-TSSOP
Data Rates	40 to 400 Mbps	270 Mbps
Output Jitter	150 ps_{P-P}	74 ps_{P-P}
ESD Rating	≥±2 kV HBM	≥±7 kV HBM
Input Interface	2.5V to 5.0V common mode	1.2V to 3.3V common mode
Output Structure	Open collector, requires external 75Ω pullups to 5V	CML with internal 50Ω pullups (to 3.3V)
Loop Filter	Three Components: 0.1 µF capacitor, 82 pF capacitor, 500Ω resistor	Single 56 nF capacitor
Rate Selection	Four selectable rates, auto or manual rate select	Single 270 Mbps rate operation, automatically bypasses other rates
Other Features	Carrier detect	Bypass/$\overline{\text{Auto Bypass}}$, choice of 2nd reclocked data output or clock

How To Replace the CLC016 with the LMH0026

Replacing the CLC016 with the LMH0026 requires a few simple steps. The device packages and pinouts are quite different so this change requires a new PCB layout. To replace the CLC016 with the LMH0026, follow these steps:

1. Change the power supply from 5V to 3.3V.
2. Replace the input termination with a single 100Ω differential termination, located close to the LMH0026 input pins. Check the output common mode voltage of the driving device to determine if it is compatible with the LMH0026 input common mode range—if not, add AC coupling capacitors in series with the input, prior to the 100Ω termination.
3. Removed the 75Ω pullups on the output and replace with a 100Ω differential termination located at the input of the next stage. The outputs may also be AC coupled, but no pullups are required.
4. Change the loop filter circuit to a single 56 nF capacitor between LF1 and LF2.
5. Add a 27 MHz crystal or suitable external clock reference. Connect the crystal between the XTAL IN/EXT CLK and XTAL OUT pins along with the 39 pF capacitors as shown in the typical application in the datasheet, or simply connect the 27 MHz external clock to the XTAL IN/EXT CLK pin.

Figure 1 shows the typical application for the CLC016, and *Figure 2* shows the typical application for the LMH0026.

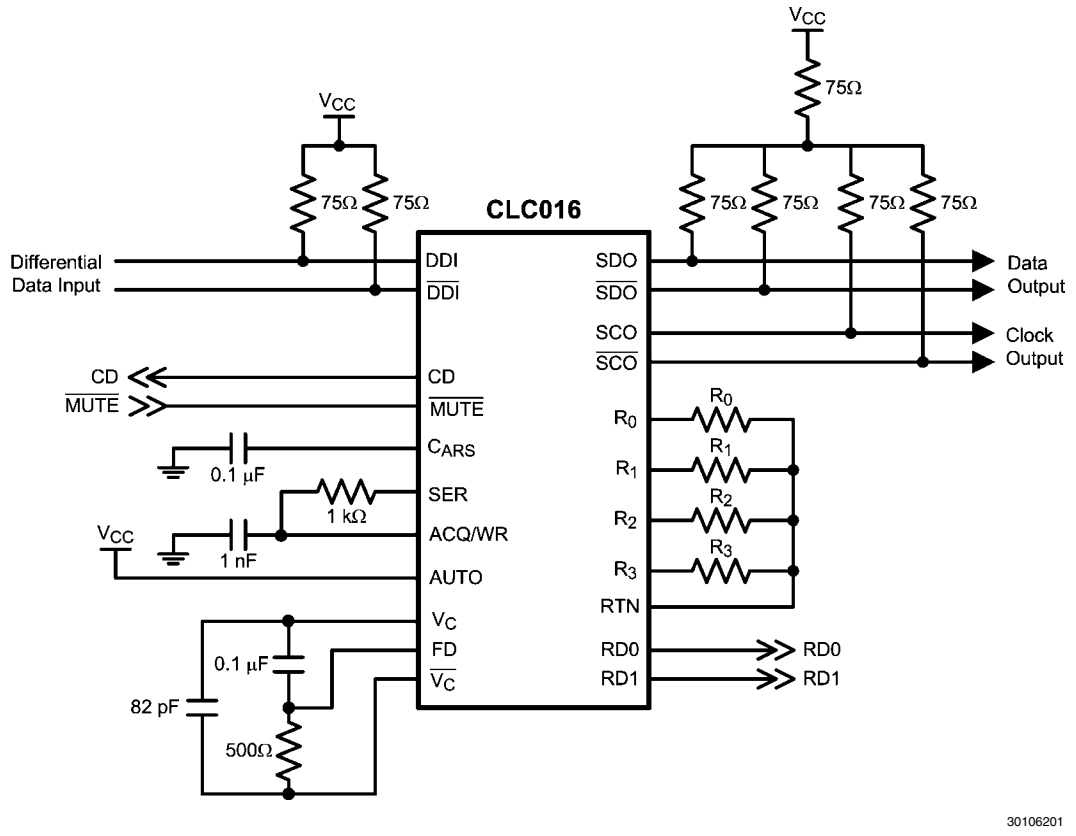

FIGURE 1. CLC016 Typical Application

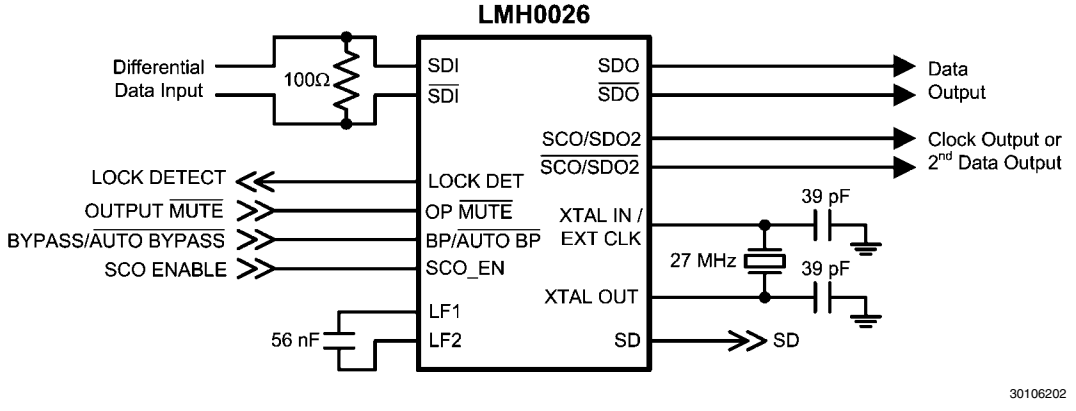

FIGURE 2. LMH0026 Typical Application

INPUT INTERFACE

The input common mode voltage range of the CLC016 is between 2.5V and V_{CC} (5V), and the minimum differential input amplitude is 200 mV. When the CLC016 input is driven by an equalizer such as the CLC014 (with its open collector output), the CLC016 input interface will typically consist of 75Ω pullups to V_{CC}, as shown in *Figure 1*.

The LMH0026 input interface is similar to that of the CLC016, but better suited for interfacing to the 3.3V and lower supply voltages of current generation devices. The input common mode voltage range of the LMH0026 is from 1.2V to V_{CC} (3.3V), with the same minimum differential input amplitude as the CLC016. This input common mode voltage range allows DC coupling to many 3.3V and 2.5V devices.

OUTPUT INTERFACE

The CLC016 outputs are open collector and require 75Ω pullups to 5V to generate an output voltage. This structure has some limitations when interfacing to non-5V systems. The CLC016 outputs are essentially cut off if the SDO output voltage drops below V_{CC}-1.6V (typically 3.4V), so this prevents DC-coupling to other 3.3V devices.

The LMH0026 provides much more flexibility. The LMH0026 outputs are CML with internal 50Ω pullups to 3.3V. They may be DC coupled to many more types of inputs, including the LMH0001 cable driver. Typically only a far-end differential termination (a simple resistor) is required. If the LMH0026 output common mode voltage is not compatible with the input common mode voltage of the receiving device, the outputs may be AC coupled. The outputs do not require pullups to V_{CC}.

LOOP FILTER

The CLC016 external loop filter circuit typically consists of a 1.0 µF capacitor, an 82 pF capacitor, and a 500Ω resistor. These components define the overall jitter transfer function and control the acquisition performance of the PLL, and may be changed to affect these parameters. For the LMH0026, the external loop filter should consist of a single 56 nF capacitor only. The LMH0026 loop filter was designed and optimized for a 56 nF capacitor and it should not be changed.

RATE SELECTION

The CLC016 can be configured to recognize up to four different data rates (between 40 Mbps and 400 Mbps) using external resistors, and can further be set to automatically detect between these four rates or manually configured for the desired rate. The LMH0026 supports a single 270 Mbps data rate, and bypasses other data rates up to 1.5 Gbps. The LMH0026 also requires an external 27 MHz reference clock (crystal or suitable external reference) which is not necessary for the CLC016, but this allows for its superior performance: the LMH0026 has typical output jitter of 0.02 UI at 270 Mbps (with 0.2 UI input jitter) vs. typical output jitter of 0.04 UI at 270 Mbps for the CLC016.

OTHER FEATURES

The CLC016 includes an input Carrier Detect (CD) signal to indicate the presence of transitions at the input. In typical CLC016 applications, CD is tied to MUTE to latch the output when no input signal is present. The LMH0026 does not provide an input carrier detector, but it does provide a robust LOCK DETECT signal to indicate that data is being received and the PLL is locked. LOCK DETECT may be connected to OUTPUT $\overline{\text{MUTE}}$ to mute the data and clock outputs when no valid data is being received.

The LMH0026 includes advanced features not present in the CLC016. The LMH0026 includes a BYPASS/$\overline{\text{AUTO BYPASS}}$ function which can be used to either force the reclocker to output all data without reclocking it, or automatically bypass only unsupported data rates while reclocking 270 Mbps data. The LMH0026 also provides the option of either a second reclocked data output or the serial data rate clock (the CLC016 only provides the clock and has no option for a second data output).

LMH0026 Enhancements over the CLC016

The LMH0026 is a solid upgrade and good replacement for the CLC016. It is designed in a newer, more advanced process. The LMH0026 offers lower power, lower jitter, better ESD protection, a more flexible output interface, and new features such as a reclocker bypass and a second reclocked data output. The LMH0026's smaller, space-saving package allows for more compact designs. The PCB layout is simpler as the LMH0026 requires less PCB components overall than the CLC016. In addition, the LMH0026's pin compatibility with HD-SDI and 3G-SDI equalizers offers an easy upgrade path and allows future-proof designs.

Notes

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