# LM5072 Evaluation Board

National Semiconductor
Application Note 1455
Youhao Xi
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## Introduction

The LM5072 evaluation board is designed to provide a low cost, fully IEEE 802.3af compliant Power over Ethernet (PoE) power supply, capable of operating with both PoE and auxiliary (AUX) power sources. The evaluation board features the LM5072 PoE Powered Device (PD) interface and controller integrated circuit (IC) configured in the versatile flyback topology.

## Features of the LM5072 Evaluation Board:

- Single Isolated 3.3V output (see Figure 1)
- Dual Isolated 5V and 3.3V outputs supported (see Figure 15)
- Non-Isolated outputs supported (see Figure 16)
- Maximum output current 3A
- Input voltage range for maximum output current (as configured):
  - With the installed wide-voltage-range EP13 transformer
    - PoE input voltage range: 38 to 60V
    - FAUX input voltage range: 24 to 60V
    - RAUX input voltage range: 16 to 60V
  - With the optional, efficiency-optimized EP13 transformer
    - PoE input voltage range: 38 to 60V
    - FAUX input voltage range: 24 to 60V
    - RAUX input voltage range: 24 to 60V
- Measured maximum efficiency:
  - With the installed wide-voltage-range EP13 transformer
    - DC to DC converter efficiency: 81% at 3A
    - Overall efficiency (including diode bridge): 78.5% at 3A
  - With the optional, efficiency-optimized EP13 transformer
    - DC to DC converter efficiency: 84% at 3A
    - Overall efficiency (including diode bridge): 81.5% at 3A
- Board Size: 2.75 x 2.00 x 0.66 inches
- Operating frequency: 250 kHz
- PoE input under-voltage lockout (UVLO) release: 39V nominal
- PoE input UVLO hysteresis: 7V nominal

This application note focuses on the evaluation board. Please refer to the datasheet for detailed information about the complete functions and features of the LM5072 IC.

## A Note about Input Potentials

The LM5072 is designed for PoE applications that are typically -48V systems, in which the notations GND and -48V normally refer to the high and low input potentials, respectively. However, for easy readability, the LM5072 datasheet was written in the positive voltage convention with positive input potentials referenced to the VEE pin of the LM5072. Therefore, when testing the evaluation board with a bench power supply, the negative terminal of the power supply is equivalent to the PoE system's -48V potential, and the positive terminal is equivalent to the PoE system ground. To prevent confusion between the datasheet and this application note, the same positive voltage convention is used herein.

## A Note About the Maximum Power Capability

While the LM5072 provides a fully IEEE 802.3af compliant PD solution, it is also capable of supporting higher power level applications with an input current up to 700 mA. However, this evaluation board is designed for IEEE 802.3af compliant PD power levels less than 12.95W. This power limitation is mainly due to the use of appropriately rated devices like the power transformer and power switch MOSFET, which do not support higher power levels. It should be noted that when using the LM5072 at elevated power levels, the thermal environment must be carefully considered.

No power conversion is 100% efficient. It should be noted that conversion efficiency lowers the amount of power that can be delivered to the load to levels significantly below 12.95W. For example, 75% efficiency limits the power delivered to 9.7W. Conversion efficiency must also be taken into account when calculating board input current.

Finally, when configured for front auxiliary operation, the maximum power deliverable may be limited by the hot swap MOSFET's DC current limit function. This is especially true at lower input voltages. The current limit can be adjusted via a single resistor on the DCCL pin.

## Schematic of the Evaluation Board

*Figure 1* shows the schematic of the LM5072 evaluation board. See the Appendix for the Bill of Materials (BOM).



## Schematic of the Evaluation Board (Continued)

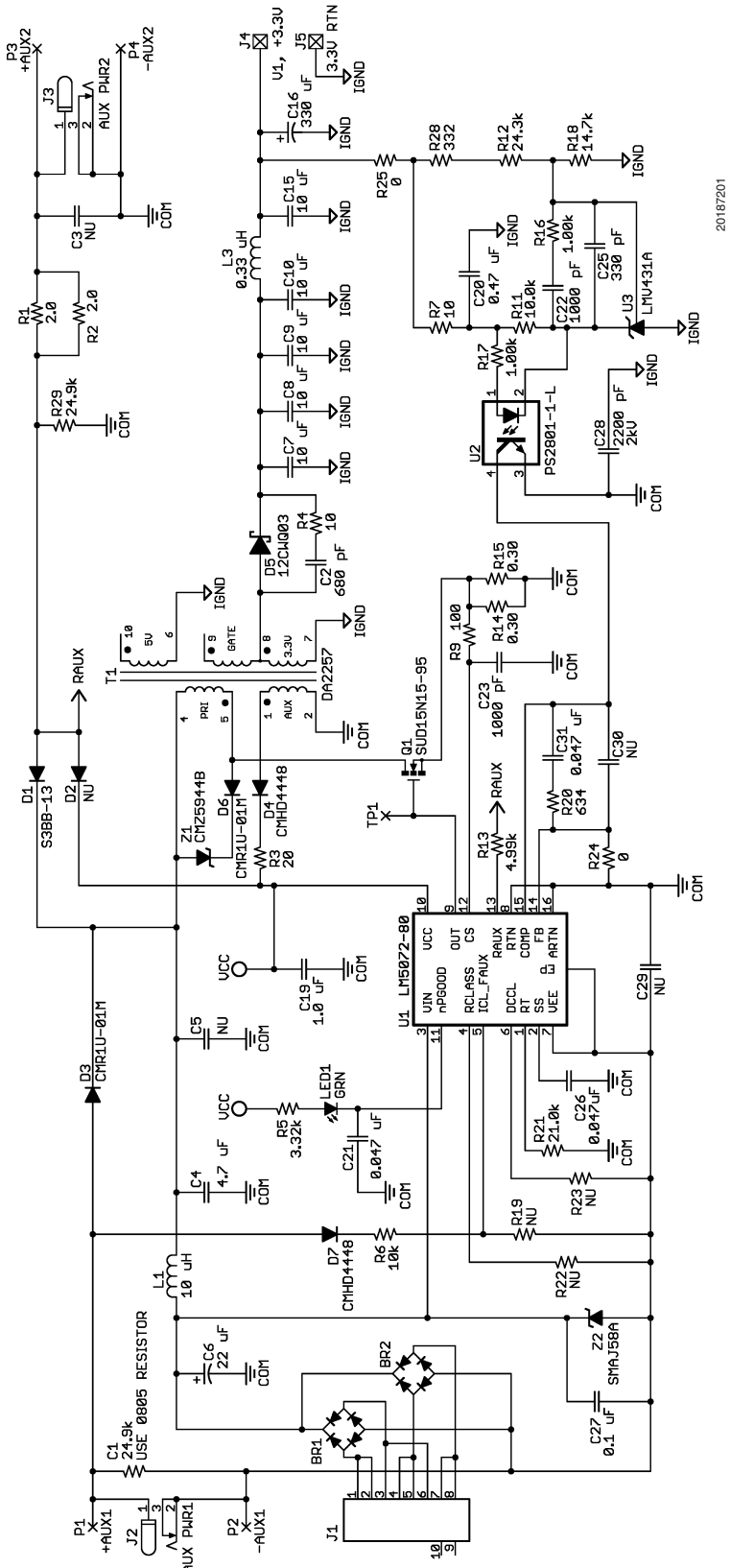



**FIGURE 1. Schematic of the LM5072 Evaluation Board**

## Connection and Proper Test Methods

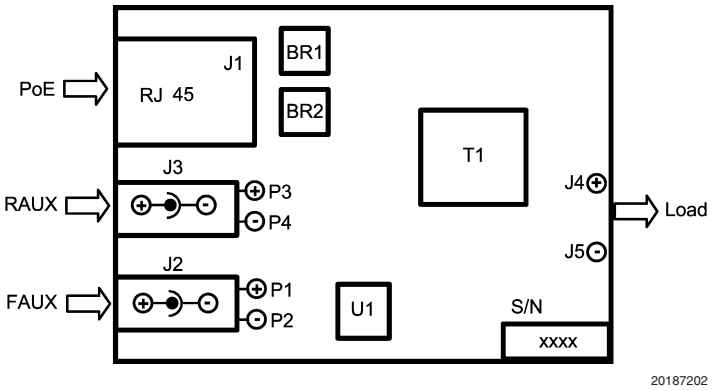



**FIGURE 2. LM5072 Evaluation Board Connections**

*Figure 2* shows the connections for the LM5072 evaluation board.

The LM5072 evaluation board has the following four ports for connections.

- J1, the RJ45 connector for PoE input
- J2, a PJ102A power jack, for Front Auxiliary (FAUX) input (also accessible with posts P1 and P2 located immediately behind the jack)
- J3, the other PJ102A power jack, for Rear Auxiliary (RAUX) input (also accessible with posts P3 and P4 immediately behind the jack)
- The 3.3V output port accessible with posts J4 and J5

For the PoE input, two diode bridges (BR1 and BR2) steer the current to the positive and negative supply pins of the LM5072. For both FAUX and RAUX inputs, the higher potential input voltages should feed into the center pins of the PJ102A jacks, or to P1 and P3, respectively. It should be pointed out that P2 and P4, the returns for the FAUX and RAUX inputs, should not be interchanged because they do not represent the same potential in the circuit. The RAUX pin is not reverse protected, and an additional reverse blocking diode will be required for complete RAUX input reverse protection.

For the output connection, the load can be either a passive resistor or active electronic load. Attention should be paid to the output polarity when connecting an electronic load. Use of additional filter capacitors greater than 20 µF total across the output port is not recommended unless the feedback loop compensation is adjusted accordingly.

Sufficiently large wire such as AWG #18 or thicker is required when connecting the source supply and load. Also, monitor the current into and out of the circuit board. Monitor the voltages directly at the board terminals, as resistive voltage drops along the connecting wires may decrease measurement accuracy. Never rely on the bench supply's voltmeter or ammeter if accurate efficiency measurements are desired.

When measuring the dc-dc converter efficiency, the converter input voltage should be measured across C4, as this is the input to the converter stage. When measuring the evaluation board overall efficiency (which is more relevant), both input and output voltages should be read from the terminals of the evaluation board.

## Source Power

To fully test the LM5072 evaluation board, a DC power supply capable of at least 60V and 1A is required for the PoE input. For the auxiliary source power, either FAUX or RAUX, use a DC power supply capable of 3A. Use the output over-voltage and over-current limit features of the bench power supplies to protect the board against damage by errant connections.

## Loading / Current Limiting Behavior

A resistive load is optimal, but an appropriate electronic load specified for operation down to 2.0V is acceptable. The maximum load current is 3.3A. Exceeding this current at low input voltage may cause oscillatory behavior as the part will go into current limit mode. Current limit mode is triggered whenever the average current through the PoE connector exceeds 440 mA (default nominal). The current limit can be programmed to any desired level up to 800 mA by selecting a resistor value for R23 (see the LM5072 datasheet for further details). If current limit is triggered, the switching regulator is automatically disabled by discharging the soft-start capacitor C26 through the SS pin. The module is then allowed to restart, but the unit will operate in an automatic re-try (hiccup) mode as long as the over-current condition remains. Switching regulator shut down during a fault condition such as current limit can be delayed by adding additional filtering capacitance to the nPGOOD pin.

## Power Up

It is suggested to apply PoE power first. During the first power up, the load should be kept reasonably low. Check the supply current during signature and classification modes before applying full power. During signature mode, the module should have the I-V characteristics of a 25 kΩ resistor in series with two diodes. During classification mode, current draw should be about 700µA at 16V; the RCLASS pin is left open, defaulting to class 0. If the proper response is not observed during both signature and classification modes, check the connections closely. If no current is flowing it is likely that the set of conductors feeding PoE power have been incorrectly installed.

Once the proper setup has been established, full power can be applied. A voltmeter across the output terminals J4

## Power Up (Continued)

(+3.3V) and J5 (3.3V RTN), will allow direct measurement of the 3.3V output line. If the 3.3V output voltage is not observed within a few seconds, turn the power supply off and review connections.

A final check of efficiency is the best way to confirm that the unit is operating properly. Efficiency significantly lower than 80% at full load indicates a problem.

After proper PoE operation is verified, the user may apply auxiliary power to the FAUX or RAUX inputs. It is recommended that the application of the auxiliary power follow the same precautions as those taken when applying PoE. If no output voltage is observed, it is likely that the auxiliary power feed polarity is reversed. After successful operation is observed in both FAUX and RAUX modes, full power testing can begin.

## PD Interface Operating Modes

When connecting into the PoE system, the evaluation board's Powered Device interface will go through the following operating modes in sequence: PD signature detection, power level classification (optional), and application of full power. Refer to the LM5072 datasheet and IEEE 802.3af for detailed information about these operating modes.

## Signature Detection

The 25 kΩ PD signature resistor is integrated into the LM5072 IC. The PD signature capacitor is implemented with a 100 nF capacitor at C27 or C29, depending on the auxiliary input configuration.

It should be noted that when either FAUX or RAUX power is applied first, it will not allow the Power Sourcing Equipment (PSE) to identify the PD as a valid device because the auxiliary voltage will cause the current steering diode bridges to be reverse biased during detection mode. This prevents the PSE from applying power, so the evaluation board will only draw current from the auxiliary source.

## Classification

PD classification is implemented with R22. The evaluation board is set to the default Class 0 by leaving the RCLASS pin open (R22 position not populated). To activate a specific class instead of Class 0, install R22 according to the following table.

| Class | $P_{MIN}$ | $P_{MAX}$ | $I_{CLASS}$(MIN) | $I_{CLASS}$(MAX) | R22 Selection |
|---|---|---|---|---|---|
| 0 | 0.44W | 12.95W | 0mA | 4mA | Open |
| 1 | 0.44W | 3.84W | 9mA | 12mA | 130Ω |
| 2 | 3.84W | 6.49W | 17mA | 20mA | 71.5Ω |
| 3 | 6.49W | 12.95W | 26mA | 30mA | 46.4Ω |
| 4 | Reserved | Reserved | 36mA | 44mA | 31.6Ω |

## Input UVLO and UVLO Hysteresis

The input Under Voltage Lock-Out (UVLO) is an integrated function of the LM5072. The UVLO release threshold is set to approximately 38.5V (at the pins of the IC) and the UVLO hysteresis is approximately 7V.

## Inrush and DC Current Limit Programming

The LM5072 allows the user to independently program the inrush and DC current limits of the internal Hot Swap MOSFET. The evaluation board sets the inrush limit to the default 150 mA by leaving R19 unpopulated, and the DC current limit to the default 440 mA by leaving the DCCL pin open (R23 not populated). In applications where it is desirable to adjust these values, install R19 and R23, respectively, according to the recommendations in the LM5072 datasheet. Please note that by leaving the DCCL pin open, the default 440 mA DC current limit will be elevated to 550 mA during FAUX operation. When R23 is used to program the DC current limit, it applies to both PoE and FAUX power modes, and it should be considered a "firm limit", i.e. independent of operating mode.

## FAUX Power Option

For the FAUX power option, the ICL_FAUX pin of the LM5072 senses the FAUX input voltage through D7 and R6. When the current flowing into the ICL_FAUX pin is greater than 50 µA at 8.5V nominal, it will establish a state at the ICL_FAUX pin that forces UVLO release in order to allow operation at an auxiliary input voltage as low as 18V (17V seen by the VIN pin of the LM5072 IC). One should not try to use the ICL_FAUX as a stable, accurate UVLO threshold, the front auxiliary supply should pull the pin up well past the voltage and current thresholds.

It should be pointed out that the minimum operative FAUX input voltage for the maximum output current is 24V. This is mainly limited by the default 540 mA FAUX input DC current limit of the LM5072's internal hot swap MOSFET. By lowering the FAUX input voltage, the input current will exceed the said limit unless the output current is reduced accordingly.

If the FAUX power option is not used in a new design, delete C1, D3, D7, R6, and J2 from the circuit to reduce the BOM cost.

## RAUX Power Option

For the rear auxiliary power option, the RAUX pin of the LM5072 senses the RAUX input voltage through R13. When the current flowing into the RAUX pin is greater than 20 µA at 2.5V nominal, it will establish a state at the RAUX pin that forces switching regulator controller operation at input voltages as low as 10V (9V seen by the pins of the LM5072 IC). When the current flowing into the RAUX pin is greater than 250 µA at 6V nominal, which is the preset configuration of the evaluation board, auxiliary dominance is selected. During auxiliary dominance, the RAUX power source will always supply the current to the PD regardless if PoE power is present or not. This is accomplished by forcing a shut down of the hot swap MOSFET. If the PSE has implemented DC Maintain Power Signature, it will remove the 48V supply thus freeing up power to be allocated to other ports. If only AC Maintain Power Signature is implemented, the PSE may or may not remove power. Note that auxiliary non-dominance does not imply PoE dominance. PoE dominance is very difficult to achieve without additional circuitry. Contact National Semiconductor for a schematic of a robust PoE dominant solution.

Because the LM5072's input hot swap feature is not applicable to the RAUX input, two 2Ω resistors (R1 and R2) in parallel are used to achieve transient protection. Unlimited inrush currents can wear on board traces, connector contacts, and various board components, as well as create dangerous transient voltages. Nevertheless, these two resistors will cause power loss in the RAUX power mode, and they also reduce the effective RAUX input voltage level sensed by the VIN pin of the LM5072. The resistors should be made as large as is practical for the application. But, with a low RAUX input voltage (<16V), R1 and R2 may need to be reduced to a lower value.

During RAUX operation, the hot swap MOSFET is turned off. Consequently, the substrate of the IC no longer has a low impedance path to power return. It is advised that the user remove C27 and populate C29. A capacitor across the hot swap MOSFET will act as both the signature capacitor and a high frequency short for any substrate noise.

If the RAUX power option is not used in a new design, delete C3, D1, D2, R1, R2, R13, R29 and J3 from the circuit to lower the BOM cost.

## Auxiliary Dominant in RAUX Power Option

The evaluation board is populated for auxiliary dominance in the RAUX power option. This is achieved by selecting 4.99 kΩ for R13. In applications where auxiliary dominance is not desirable, change the installed R13 to a higher value. Please refer to the LM5072 datasheet for assistance in selecting this value.

## Auxiliary Input "OR-ing" Diode Selection

Special attention should be paid to the selection of D1 and D3. They need not be high speed diodes because there is no switching action during operation associated with these components, but they should be low reverse leakage current devices. Otherwise, the leakage current during operation may create a false signal at the ICL_FAUX pin, the RAUX pin, or both, as if the circuit is powered from the FAUX or RAUX source. Leakage current into the ICL_FAUX pin may also corrupt inrush current programming, if implemented. Most diode and transistor datasheets provide information on the maximum leakage current at both 25˚C and 125˚C, although the data for the intermediate temperatures are not often supplied. It can be approximated that the leakage current doubles for every 10˚C rise in temperature.

The junction temperature of these devices should not reach 125˚C because the only dissipation inside these devices is caused by the leakage current. Therefore, it is not necessary to select the devices based on the maximum leakage current specified at 125˚C. The evaluation board design considered 55˚C as the maximum junction temperature of these devices, which is acceptable for most PoE applications. Simple circuit adjustments can be made if higher leakage currents are expected.

Resistors R29 and C1 (note that a resistor is installed at the C1 loacation on the evaluation board to achieve the function similar to R29's) are both 24.9 kΩ, providing paths for the leakage currents of D1 and D3, respectively. These two resistors are meant to sink all of the leakage current from the

## Auxiliary Input "OR-ing" Diode Selection (Continued)

diodes and prevent false states at the ICL_FAUX and RAUX pins. Please see the LM5072 datasheet for more details about the selection of these two resistors.

## Flyback Converter Topology

The dc-dc converter stage of the LM5072 evaluation board features the flyback topology, which employs the minimum number of power components to implement an isolated power supply at the lowest possible cost.

A unique characteristic of the flyback topology is its power transformer. Unlike an ordinary power transformer that simultaneously transfers the power from the primary to the secondary, the flyback transformer first stores the energy in the transformer core while the main switch is turned on, then releases the stored energy to the load during the rest of the cycle. When the stored energy is not completely released before the main switch is turned on again, it is said that the flyback converter operates in continuous conduction mode (CCM). Otherwise, it is in discontinuous conduction mode (DCM).

Major advantages of CCM over DCM include (i) lower ripple current and ripple voltage, requiring smaller input and output filter capacitors; and (ii) lower RMS current, thus reducing the conduction losses. To keep the flyback converter in CCM at light load, the transformer's primary inductance should be designed as large as is practical.

Major drawbacks of CCM, as compared to DCM, are (i) the presence of the right-half-plane zero, which may limit the achievable bandwidth of the feedback loop, and (ii) the need for slope compensation to stabilize the feedback loop at duty cycles greater than 50%.

The flyback topology can have multiple secondary windings for several isolated outputs. One or more of these secondary channels are normally utilized internally by the converter itself to provide necessary bias voltages for the controller.

The evaluation board uses a small power transformer having a primary inductance of 32 µH. This is a compromise made to allow the small transformer to operate over a wide input voltage range from 13V to 60V. However, with this transformer, the flyback converter runs in CCM at full load for input voltages lower than 42V, and in DCM for higher input voltages or light loads. The LM5072's built-in slope compensation helps stabilize the feedback loop when the duty cycle exceeds 50% during low input voltage operation.

A transformer winding is used to provide the bias voltage ($V_{CC}$) to the LM5072 IC. Although the LM5072 controller includes an internal startup regulator which can support the bias requirement indefinitely, the transformer winding produces an output about 2V higher than the startup regulator output, thus shutting off the startup regulator and reducing the power dissipation inside the IC. Given the low current limit value (15 mA nominal) of the high voltage startup regulator, the $V_{CC}$ line is not meant to be a linear regulator for external loads.

## Factors Limiting the Minimum Operating Input Voltage

The LM5072 supports operation with low voltage auxiliary power sources. The minimum FAUX voltage is 24V for the maximum output current. It can be reduced to 18V if the output current is reduced to 2A. The voltage drop caused by the FAUX input OR-ing diode D3 reduces the VIN pin potential to 17V. This is because at lower FAUX input voltages the maximum power that can be delivered to the load will be greatly reduced by the hot swap MOSFET's current limit function. This is one of the drawbacks of FAUX operation, though DC current limit can be adjusted by adding / changing the value of the DCCL resistor.

The minimum RAUX voltage of the evaluation board is 16V (voltage drops caused by the inrush limit resistors R1 and R2 and the RAUX input OR-ing diode D1 reduce the VIN pin potential to about 15V), although the LM5072 can function with a minimum of 9V seen at VIN. The 13V RAUX operating voltage limit is mainly determined by three factors; the value of the RAUX inrush current limit resistor R1 and R2, the flyback power transformer design, the values of the current sense resistors R14 and R15, and mainly the dropout of the startup regulator.

The installed R1 and R2 are 2Ω resistors. Under full load conditions, these two resistors significantly reduce the effective RAUX voltage seen by the DC-DC converter stage. In order to operate the evaluation board at a lower input voltage, it is required to reduce R1 and R2 to 1Ω or lower values.

The installed EP13 type power transformer (DA2257-AL or DCT13EP-U12S005) is a low cost, area efficient solution to operate with a wide auxiliary input voltage range. However, the small cross-sectional area of the EP13 magnetic core also limits the maximum flux it can support. To use such a small transformer from 16V to 60V input under the full load condition, a compromise between the minimum operating input voltage and maximum inductance of the transformer must be made such that the peak current at 16V input will not cause the peak flux density to exceed 3000 Gauss (saturation). A drawback of this low cost solution is that the RMS current flowing through the dc-dc converter stage is increased and the efficiency of the dc-dc converter suffers by about 3%.

Replacing the installed transformer with the optional power transformer DA2383-AL from Coilcraft improves the efficiency, but the minimum operating input voltage will be limited to 24V. To use this optional transformer for lower input voltage, the load level should be scaled down accordingly, as shown in Figure 3.

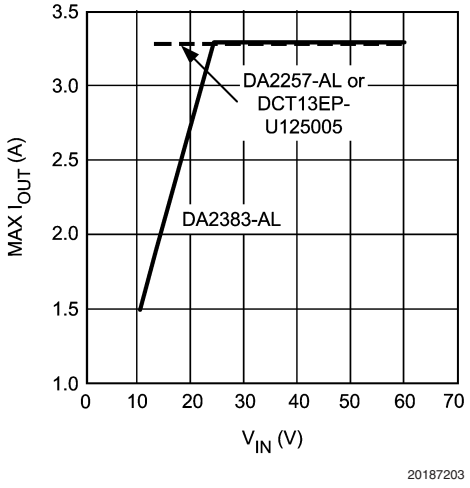



**FIGURE 3. Maximum Load Current vs. Minimum Input Voltage as Limited by Different EP13 Type Power Transformers**

## Factors Limiting the Minimum Operating Input Voltage (Continued)

To optimize efficiency over the maximum input voltage range of 10.5V to 60V (9V min seen at the VIN pin, after R1 and R2 are replaced with 1Ω), a larger magnetic core like the EFD20 should be used. The EFD20 core has adequate cross-sectional area to handle the peak currents observed with a 10.5V input.

The effects of the current sense resistors R14 and R15 also limit the minimum RAUX input operating voltage. The LM5072's internal slope compensation stabilizes the feedback loop of the dc-dc converter when the duty cycle exceeds 50% for input voltages lower than 22V. However, the relative magnitude of the slope compensation is inversely proportional to the values of R14 and R15. The maximum values of R14 and R15 are governed by the following relation:

$$\frac{R14 \times R15}{R14 + R15} < \frac{1.8 \times D_{max}}{2 \times D_{max} - 1} \times \frac{f_{SW} \times L_m}{k_t \times (V_O + V_F)} \times 10^{-4}$$

where

$D_{max}$ is the duty cycle at the minimum AUXILIARY input voltage;

$f_{sw}$ the switching frequency, in kHz

$L_m$ the flyback transformer primary inductance, in µH

$k_t$ the transformer's primary to secondary turns ratio

$V_o$ the output voltage, in volts

$V_F$ the forward drop of the output diode D5, in volts

Selecting 0.30Ω for both R14 and R15 will allow a minimum operating voltage of 16V. For lower RAUX input voltages, Dmax is greater and hence R14 and R15 must be reduced accordingly. However, smaller resistors increase the effect of internal slope compensation. Increasing the slope compensating makes the feedback loop appear more like voltage mode than current mode. This in turn requires the use of a low ESR capacitor for C16, rather than the low cost capacitor initially installed on the evaluation board.

In summary, the 16V minimum operating RAUX input voltage of the evaluation board is limited by the low cost solution, and also by the dropout of the startup regulator. In order to use the evaluation board with a lower RAUX source, the power transformer T1, the output capacitor C16, R14, and R15 should be modified, in addition to the installation of D2.

D2 should be installed whenever the voltage at the VIN pin is less than 15V. This ensures the $V_{CC}$ regulator has enough voltage to start given its relatively high drop out requirement. One must also be careful not to violate the VCC pin's absolute maximum voltage rating under this configuration. Accordingly, a 15V nominal auxiliary supply may be difficult to design for, as it will require the installation of D2 and violate the pin's absolute maximum rating. Additional circuitry may be required, or the selection of a different auxiliary input voltage.

## Performance Characteristics

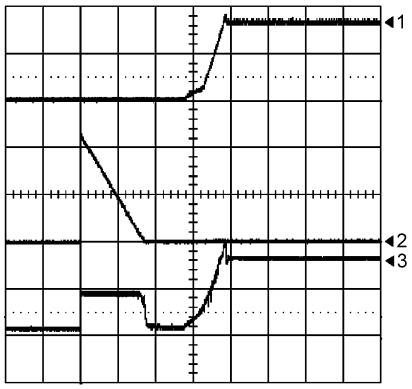
### PoE INPUT POWER UP SEQUENCE

The high level of integration designed into the LM5072 allows all power sequencing communications to occur within the IC. Very little system management design is required by the user. The power up sequence is as follows. Note that the RTN pin (IC pin 8) is isolated from the +3.3V RTN output pin of the board:

1. Before power up, all nodes in the non-isolated section of the power supply remain at high potential until UVLO is released and the drain of the internal hot swap MOSFET is pulled down to VEE (IC pin 7).
2. The $V_{CC}$ regulator powers up during the inrush sequence. During $V_{CC}$ regulator startup, it draws current on the order of 20mA, but this will likely not be noticed by the user. Once the RTN pin of the IC drops below 1.5V (referenced to VEE), and the gate of the hot swap MOSFET rises, power good is asserted by pulling the nPGOOD pin low.
3. Once power good has been asserted, the SS (Soft-Start) pin is released. The SS pin will rise at a rate equal to the SS current source, typically 10µA, divided by the SS pin capacitance, C26.
4. As the switching regulator achieves regulation, the auxiliary winding will raise the $V_{CC}$ voltage to about 11V, thus shutting down the internal regulator and increasing efficiency.

Figure 4 shows the voltage at the RTN pin (referenced to VEE), output voltage $V_{OUT}$ and input current during a normal startup sequence. The RTN voltage gradually drops as the input current charges the input capacitors. When the charging process is completed, the RTN voltage drops to below 1.5V, followed by the soft start of the converter.

Figure 5 shows the $V_{CC}$ voltage during startup. The $V_{CC}$ of about 8V is first produced by the internal startup regulator. When the output regulation is established, $V_{CC}$ is elevated to about 11V through cross-regulation.




Horizontal Resolution: 5 ms/Div.

Trace 1: VOUT, 2V/Div.

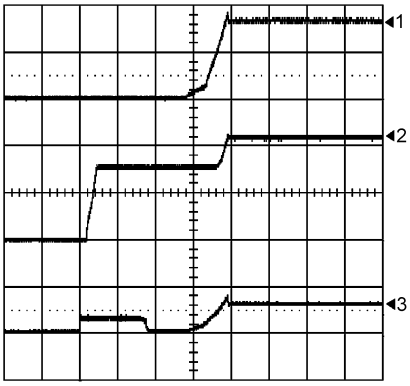
Trace 2: RTN pin (referenced to VEE), 20V/Div.

Trace 3: Input Current, 200 mA/Div.

**FIGURE 4. Normal PoE input Startup Sequence**

## Performance Characteristics

(Continued)

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Horizontal Resolution: 5 ms/Div.

Trace 1: VOUT, cross-regulating VCC after output regulation is established. 2V/Div.

Trace 2: VCC, first regulated by startup regulator at 7.6V, then elevated by auxiliary winding to 11V. 2V/Div.

Trace 3: Input Current, 0.5A/Div.

**FIGURE 5. VCC During Startup**

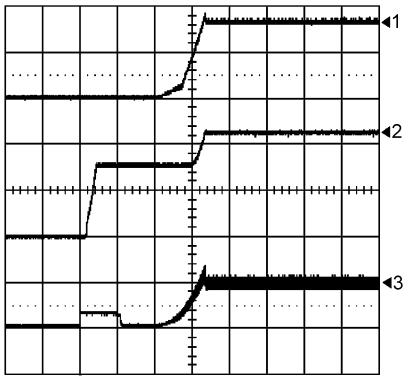
### AUXILIARY INPUT POWER UP SEQUENCE

The FAUX input power up sequence is similar to that of the PoE input, with the exception that the 38V UVLO release threshold is overridden when the ICL_FAUX pin is pulled up.

The RAUX input power up sequence is simpler:

1. Auxiliary application quickly charges the input capacitors. There should not be any overshoot observed as the series resistors should limit the inrush.
2. When the $V_{CC}$ regulator establishes 7.6V, soft start of the PWM controller begins.
3. As the switching regulator achieves regulation, the auxiliary winding will raise the $V_{CC}$ voltage to about 10V, thus shutting down the internal regulator and increasing efficiency.

Figures 6 and 7 shows the FAUX and RAUX input power up sequence, respectively.

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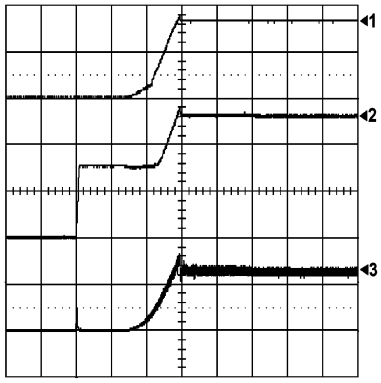
Horizontal Resolution: 5 ms/Div.

Trace 1: VOUT, 2V/Div.

Trace 2: VCC, 5V/Div.

Trace 3: Input Current, 0.5A/Div.

**FIGURE 6. Normal FAUX input Startup Sequence**

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Horizontal Resolution: 5 ms/Div.

Trace 1: VOUT, 2V/Div.

Trace 2: VCC, 5V/Div.

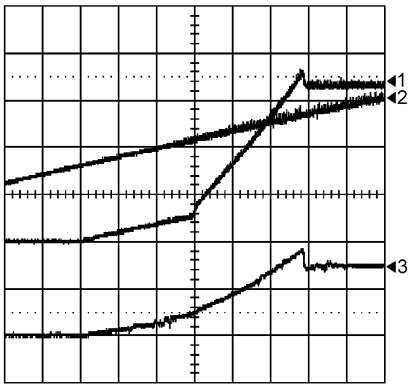
Trace 3: Input Current, 0.5A/Div.

**FIGURE 7. Normal RAUX input Startup Sequence**

Figure 8 shows the normal 3.3V output voltage startup, along with the SS pin for reference.

## Performance Characteristics

(Continued)




Horizontal Resolution: 1 ms/Div.

Trace 1: VOUT, 1V/Div.

Trace 2: SS pin voltage (referenced to RTN), 1V/Div

Trace 3: Input current (AC coupled), 200 mA/Div

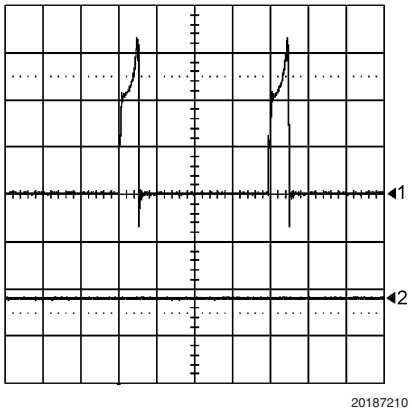
**FIGURE 8. Output Voltage Vout (+3.3V) Soft-start Detail**

**OUTPUT DEAD SHORT FAULT RESPONSE**

The evaluation board survives the output dead short condition by running into a re-try mode (hiccup). Applying a dead short to the +3.3V line causes a number of protection mechanisms to occur sequentially. They are:

1. The feedback signal increases the duty cycle in an attempt to maintain the output voltage. This initiates cycle-by-cycle over-current limiting which turns off the main switch when the current sense (CS) pin exceeds the current limit threshold.
2. The current in the internal hot swap MOSFET rises until it is current limited around 440 mA. Some overshoot in the current will be observed, as it takes time for the current limit amplifier to react and change the operating mode of the MOSFET.
3. Because linear current limit is accomplished by driving the MOSET into the saturation region, the drain voltage (RTN pin) rises. When it reaches 2.5V with respect to VEE, power good is de-asserted and the nPGOOD pin rises in voltage.
4. The de-assertion of power good causes the discharge of the softstart capacitor, which disables all switching action in the dc-dc converter.
5. Once the switching stops, the current in the internal MOSFET will decrease and the drain voltage will fall back below 1.5V with respect to VEE. When power good is re-asserted, the dc-dc converter will automatically restart with a new softstart sequence.

Figure 9 shows the cycle-by-cycle peak current limit providing the over-current protection under output short-circuit condition. The short-circuit condition causes a large over current such that it intends to saturate the power transformer. Consequently, a large peak current of about 4.33A is produced in the primary circuit. This large peak current causes the current-sense voltage at CS pin to exceed the peak limit threshold (>0.5V). Therefore the PWM duty cycle is cut short, leading to a limited input current (the average current of the current pulses) at about 0.34A.




Horizontal Resolution: 1 µs/Div.

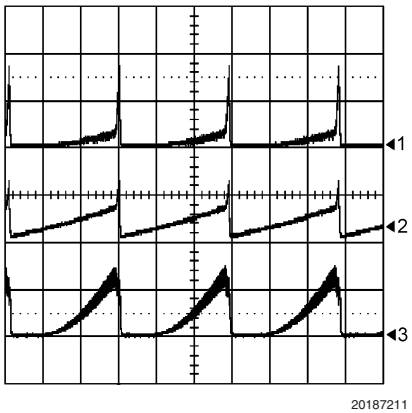
Trace 1: Voltage at the CS pin, 200 mV/Div.

Trace 2: Input Current, 0.5A/Div.

Vin=48V. Iin=0.34A

**FIGURE 9. Cycle-by-Cycle Peak Current Limit Protection Under Output Short-Circuit Condition**

Figure 10 shows the over-current protection by the hot swap MOSFET's dc current limit under the output short circuit condition. The circuit operates in the FAUX power configuration, and the FAUX input voltage is set to 24V. The input current will exceed the 440 mA DC current limit of the hot swap MOSFET, and causes the voltage at the RTN pin to rise rapidly. It also discharges the soft start capacitor C26 connected to the SS pin, and the circuit enters the automatic retry mode until the over-current condition is removed. The voltage at the SS pin is observed to rise quickly as the LM5072 reacts to the fault. This is because the internal soft-start circuitry is referenced to RTN, while all scope measurements are referenced to VEE.




Horizontal Resolution: 5 ms/Div.

Trace 1: RTN pin voltage (referenced to VEE), 2V/Div.

Trace 2: Softstart pin (referenced to VEE), 5V/Div.

Trace 3: Input current, 0.5A/Div.

FAUX input=24V

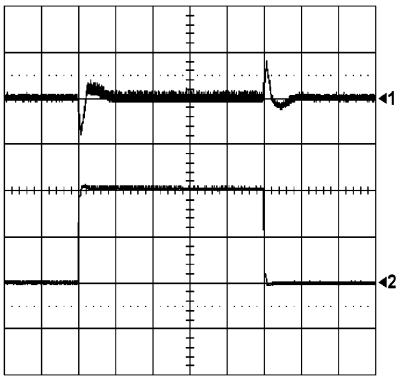
**FIGURE 10. Shorted Output Fault Condition / Automatic Re-try**

## Performance Characteristics

(Continued)

**STEP RESPONSE**

Figure 11 shows the step load response at Vin = 48V.




20187212

Horizontal Resolution: 0.2 ms/Div.

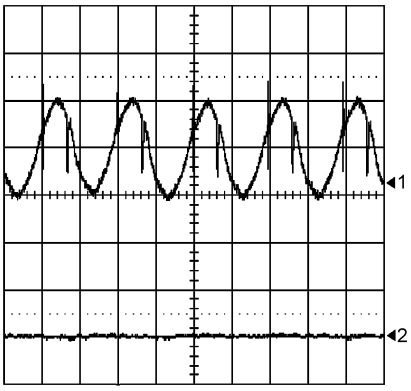
Trace 1: Output voltage (AC coupled), 200 mV/Div.

Trace 2: Output current (DC coupled), 0.5 A/Div.

**FIGURE 11. Regulator Response to Step Load**

**RIPPLE VOLTAGE/CURRENT**

Figure 12 shows the output ripple voltage and input ripple current for 48V input voltage and 3.3A output. The input ripple current is reduced to less than 5 mA pk-pk by the input filter inductor.




20187213

Horizontal Resolution: 0.2 ms/Div.

Trace 1: Output voltage (AC coupled), 20 mV/Div.

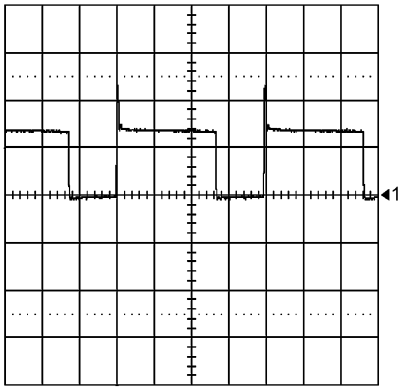
Trace 2: Input current (AC coupled), 50 mA/Div.

Vin=48V, Iout=3.3A

**FIGURE 12. Ripple Currents and Voltages**

**FLYBACK TRANSFORMER WAVEFORMS**

Figures 13 and 14 show typical flyback transformer waveforms: the drain to source voltage of the main switch Q1 and the reverse voltage of the rectifier diode D5, respectively, at 48V input voltage and 3.3A output.



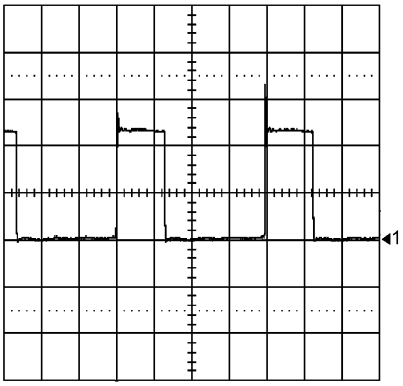

20187214

Horizontal Resolution: 1 µs/Div.

Trace 1: Drain to source voltge of main switch Q1, 50V/Div.

Vin=48V, Iout=3.3A

**FIGURE 13. Flyback Transformer Waveforms**




20187215

Horizontal Resolution: 1 µs/Div.

Trace 1: Reverse voltage across output rectifier diode D5, 5V/Div.

Vin=48V, Iout=3.3A

**FIGURE 14. Flyback Transformer Waveforms**

## Reconfiguration of the Evaluation Board for 3.3V And 5V Dual Outputs

The standard evaluation circuit can be easily reconfigured into a 2A 3.3V and 0.6A 5.5V dual output power supply. To reconfigure the board for dual output, populate the components for the 5.5V output rail as shown in Figure 15. These components are listed in the additional BOM list in the Appendix.

## Reconfiguration of the Evaluation Board for Non-Isolated Output

For applications where output isolation is not required, the non-isolated version of the evaluation board can be used to reduce the BOM cost. Reconfiguration of the circuit board to the non-isolated version can be accomplished in the following four steps:

1. Delete the unused parts from the circuit board as well as the BOM: C20, C22, C25, C28, R7, R11, R16, R17, R24, U2 and U3.
2. Connect test points P5 and P6 with a bus wire of AWG 26.
3. Short C28 pads by installing a 0Ω resistor of R2010 size, or by soldering a piece of AWG 26 bus wire.
4. Change C30 to 3.3 nF, C31 to 1.0 nF and R20 to 10 kΩ.

Figure 16 shows the schematic for non-isolated circuit with a single 3.3V output. Similar changes also apply to the dual output version.

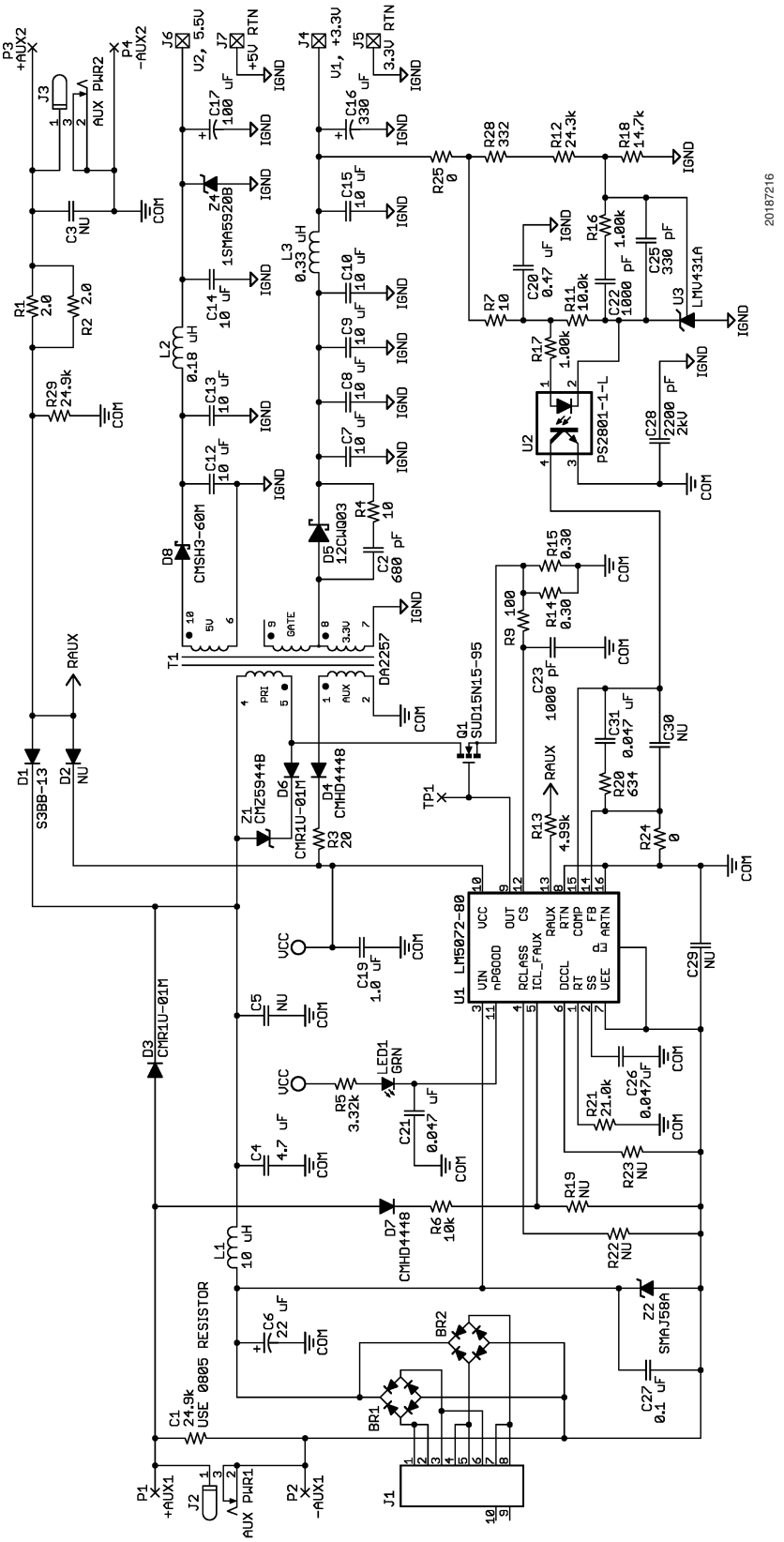



**FIGURE 15. The Schematic for Dual Outputs**

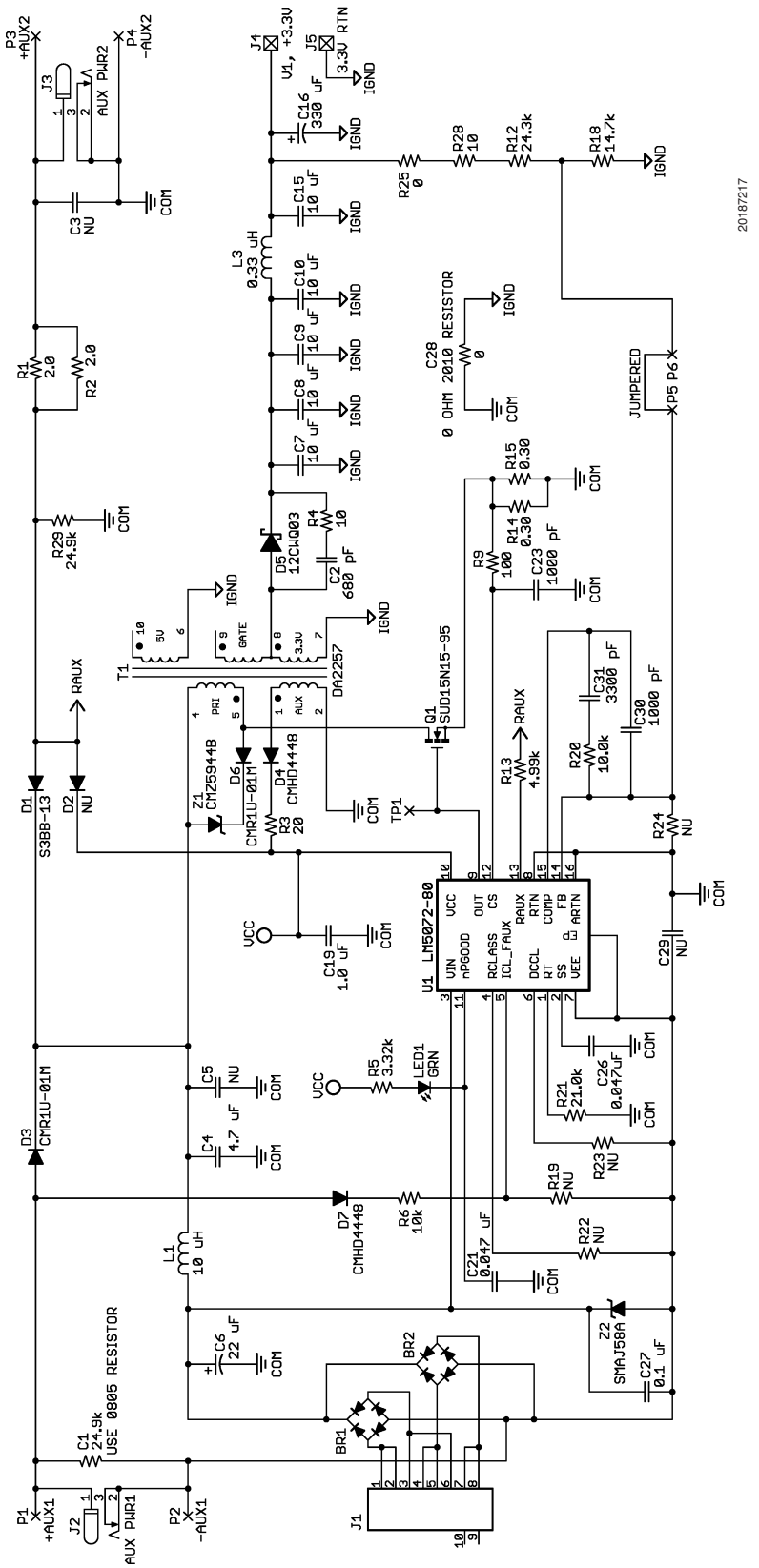



**FIGURE 16. The Schematic for Non-Isolated Output**

## A Note For Using The Efficiency Optimized EP13 Power Transformer DA2383

Please note that the DA2383 is a single output transformer. When using a DA2383 to obtain better efficiency (See Figure 3 for the applicable load and AUX input voltage levels), also remember to connect D5's cathode to DA2383's pin 9 with a short jumper wire. This is because the secondary winding of DA2382 uses Pins 6 through 9 of the transformer bobbin, unlike DA2257 that only uses of Pins 7 and 8 for the secondary winding. The maximum converter stage efficiency at 3.3A will be expected to be greater than 84%.

## Appendix: LM5072 Evaluation Board Bill of Materials

| ITEM | PART NUMBER | DESCRIPTION | VALUE |
|---|---|---|---|
| BR1 | CBRHD-01 | DIODE BRIDGE, SMDIP, CENTRAL | 0.5A, 100V |
| BR2 | CBRHD-01 | DIODE BRIDGE, SMDIP, CENTRAL | 0.5A, 100V |
| C1 | CRCW08052492F | RESISTOR | 24.9K |
| C2 | C0805C681F5GAC | CAPACITOR, CER, CC0805, KEMET | 680p, 50V |
| C3 | NU | | |
| C4 | C5750X7R2A475M | CAPACITOR, CER, CC2220, TDK | 4.7µF, 100V |
| C5 | NU | | |
| C6 | EEV-HA2A220P | CAPACITOR, AL ELEC, PANASONIC | 22µF, 100V |
| C7 | C3216X5R0J106M | CAPACITOR, CER, CC1206, TDK | 10µF, 6.3V |
| C8 | C3216X5R0J106M | CAPACITOR, CER, CC1206, TDK | 10µF, 6.3V |
| C9 | C3216X5R0J106M | CAPACITOR, CER, CC1206, TDK | 10µF, 6.3V |
| C10 | C3216X5R0J106M | CAPACITOR, CER, CC1206, TDK | 10µF, 6.3V |
| C15 | C3216X5R0J106M | CAPACITOR, CER, CC1206, TDK | 10µF, 6.3V |
| C16 | EMVY6R3ADA331MF80G | CAPACITOR, AL ELEC, CHEMI-ON | 330µF, 6.3V |
| C19 | C2012X5R1C105K | CAPACITOR, CER, CC0805, TDK | 1.0µF, 16V |
| C20 | C2012X5R1C474K | CAPACITOR, CER, CC0805, TDK | 0.47µF, 16V |
| C21 | C0805C473K5RAC | CAPACITOR, CER, CC0805, KEMET | 47nF, 50V |
| C22 | C0805C102K5RAC | CAPACITOR, CER, CC0805, KEMET | 1nF, 50V |
| C23 | C0805C102K5RAC | CAPACITOR, CER, CC0805, KEMET | 1nF, 50V |
| C25 | C0805C331K5RAC | CAPACITOR, CER, CC0805, KEMET | 330pF, 50V |
| C26 | C0805C473K5RAC | CAPACITOR, CER, CC0805, KEMET | 47nF, 50V |
| C27 | C3216X7R2A104K | CAPACITOR, CER, CC1206, TDK | 100nF, 100V |
| C28 | C4532X7R3D222K | CAPACITOR, CER, CC1812, TDK | 2.2nF, 2 kV |
| C31 | C0805C473K5RAC | CAPACITOR, CER, CC0805, KEMET | 47nF, 50V |
| D1 | S3BB-13 | DIODE, SMB, DIODE INC | 3A, 100V |
| D2 | NU | | |
| D3 | CMR1U-01M | DIODE, SMA, CENTRAL | 1A, 100V |
| D4 | CMHD4448 | DIODE, SOD123, CENTRAL | 125mA, 75V |
| D5 | 12CWQ03FN | SCHOTTKY, TO252, IR | 12A, 30V |
| D6 | CMR1U-01M | DIODE, SMA, CENTRAL | 1A, 100V |
| D7 | CMHD4448 | DIODE, SOD123, CENTRAL | 125mA, 75V |
| J1 | RJ-45-8N-B | RJ-45 CONNECTOR | |
| J2 | PJ-102A | POWER JACK | |
| J3 | PJ-102A | POWER JACK | |
| J4 | 3104-2-00-01-00-00-080 | POST, MILL MAX | |
| J5 | 3104-2-00-01-00-00-080 | POST, MILL MAX | |
| L1 | DO3308P-103MLD | SM INDUCTOR, COILCRAFT | 10µH |
| L3 | DO1813P-331HC | SM INDUCTOR, COILCRAFT | 0.33µH |
| LED1 | SSL-LXA228GC-TR11 | LED,GREEN, LUMEX | |
| P1 | 5012K-ND | TEST POINT, KEYSTONE | |
| P2 | 5012K-ND | TEST POINT, KEYSTONE | |
| P3 | 5012K-ND | TEST POINT, KEYSTONE | |
| P4 | 5012K-ND | TEST POINT, KEYSTONE | |

## Appendix: LM5072 Evaluation Board Bill of Materials (Continued)

| ITEM | PART NUMBER | DESCRIPTION | VALUE |
|---|---|---|---|
| Q1 | SUD15N15-95 | MOSFET, N-CH, TO252, VISHAY | 150V, 15A |
| R1 | CRCW2512200J | RESISTOR | 2Ω, 1W |
| R2 | CRCW2512200J | RESISTOR | 2Ω, 1W |
| R3 | CRCW080520R0F | RESISTOR | 20Ω |
| R4 | CRCW120610R0F | RESISTOR | 10Ω |
| R5 | CRCW08053321F | RESISTOR | 3.3kΩ |
| R6 | CRCW08051002F | RESISTOR | 10kΩ |
| R7 | CRCW080510R0F | RESISTOR | 10Ω |
| R9 | CRCW08051000F | RESISTOR | 100Ω |
| R11 | CRCW08051002F | RESISTOR | 10kΩ |
| R12 | CRCW08052432F | RESISTOR | 24.3kΩ |
| R13 | CRCW08054991F | RESISTOR | 4.9kΩ |
| R14 | CRCW12060R301F | RESISTOR | 0.301Ω |
| R15 | CRCW12060R301F | RESISTOR | 0.301Ω |
| R16 | CRCW08051001F | RESISTOR | 1kΩ |
| R17 | CRCW08051001F | RESISTOR | 1kΩ |
| R18 | CRCW08051472F | RESISTOR | 14.7kΩ |
| R19 | NU | | |
| R20 | CRCW08056340F | RESISTOR | 634Ω |
| R21 | CRCW08052102F | RESISTOR | 21.0kΩ |
| R22 | NU | | |
| R23 | NU | | |
| R24 | CRCW08050R0J | RESISTOR | 0Ω |
| R25 | CRCW08050R0J | RESISTOR | 0Ω |
| R28 | CRCW08053320F | RESISTOR | 332Ω |
| R29 | CRCW08052492F | RESISTOR | 24.9kΩ |
| T1A | DA2257-AL | XFMR, FLYBACK, COILCRAFT | 32µH |
| T1B | DCT13EP-U12S005 | XFMR, FLYBACK, TDK | 32µH |
| U1 | LM5072-80 | POE PI AND PWM CTRL, NATIONAL | LM5072-80 |
| U2A | PS2801-1-L | OPTO-COUPLER, NEC | PS2801 |
| U2B | PC3H7D | OPTO-COUPLER, SHARP | PC3H7D |
| U3 | LMV431A | REFERENCE, SOT23-3, NATIONAL | LMV431A |
| Z1 | CMZ5944B | Zener, 60V, CENTRAL | CMZ5938B |
| Z2 | SMAJ58A | TVS, 58V, DIODE INC | SMAJ58A |

## Additional BOM to Add An 1A, 5.5V Output Rail

| ITEM | PART NUMBER | DESCRIPTION | VALUE |
|---|---|---|---|
| C12 | C3216X5R1A106M | CAPACITOR, CER, CC1206, TDK | 10µF, 10V |
| C13 | C3216X5R1A106M | CAPACITOR, CER, CC1206, TDK | 10µF, 10V |
| C14 | C3216X5R1A106M | CAPACITOR, CER, CC1206, TDK | 10µF, 10V |
| C17 | EMVY100ADA101MF55G | CAPACITOR, AL ELEC, CHEMI-ON | 100µF, 10V |
| D8 | CMSH2-60 | DIODE, SMA, CENTRAL | 2A, 60V |
| J6 | 3104-2-00-01-00-00-080 | POST, MILL MAX | |
| J7 | 3104-2-00-01-00-00-080 | POST, MILL MAX | |
| L2 | DO1813P-181MLD | SM INDUCTOR, COILCRAFT | 0.18µH |
| Z4 | CMZ5920B | ZENER, SMA, CENTRAL | 6.2V |

**Note:** The total load of the dual outputs should be limited below 10W maximum.



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