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PROM Power-Down Circuits

description

Inexpensive bipolar PROMs can be used in high performance, low power applications if powered down when they are not being accessed. Since the access time of the circuit of Figure 1 is less than 80 nanoseconds, the power saving can be greater than 10 to 1 if cycled every microsecond. Longer cycle times, or decoding of the power switching to multiple packages, can yield even more impressive ratios.

Bipolar PROMs with on-chip power-down have power-up to power-down ratios of 3:1. Using the PROM power-down technique illustrated in Figure 1, ratios considerably higher than 3:1 can be obtained. National's PROMs perform well in this application. With power removed, the Tri-State® parts revert quickly to the third (open high Z) state. Because there are no clamp diodes from the outputs to V_{CC}, the powered down device presents only leakage to the output bus.

PROMs do not need to be continuously powered in many applications. Often data is required from a PROM on system power up or for a small percentage of a system cycle. Turning the PROM off when it is not needed saves power and the access time is increased by only the delay of the power down circuit.

The basic power down circuit is illustrated in Figure 2. A TTL level input signal drives the TTL logic input of the power down circuit. The logic input is drawn as a noninverting buffer; however, circuit operation is not limited to noninverting buffers. Logic Table 1 illustrates several logic implementations of both inverting and noninverting inputs with different speed-power tradeoffs.

Circuit operation is as follows. When the logic input to R_2 goes low, base drive is supplied to the PNP switch, turning the switch on. C_1 is a speed-up capacitor which decreases the switching time of the PNP switch. In applications where high speed is not important C_1 is not necessary. When the PNP saturating switch is on V_{CC} (+5 V) is applied to the PROM. The time delay from power up command to power up on the PROM ranges from about 10 ns to 100 ns, depending upon the PNP switch and the TTL logic driving the switch.

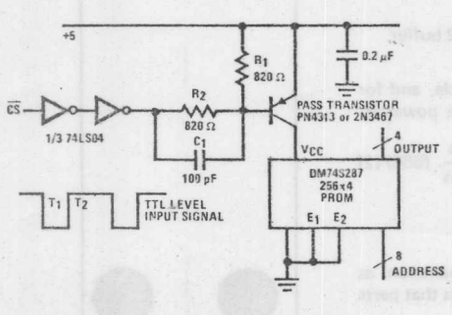


Figure 1. PROM Power Down Circuit

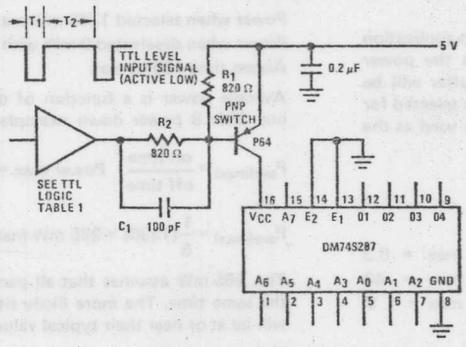


Figure 2. PROM Power Down Circuit

DA-B20M126/Printed in U.S.A.

logic table

TTL LOGIC	
CS — 74S00 74LS00	• Fast • Active High Selects 74S00 Speed 74LS00 Speed and Low Power
$\overline{CS}$ — 74S04 74LS04	• Fast • Active Low Selects 74S04 Speed Only 74LS04 Speed and Low Power
$\overline{CS}$ — MM74C902	• Very Low Power • Active Low Selects Buffers can be connected in parallel for additional current
1-10 DECODER, 4, 10 — MM74C42	• Very Low Power • Memory Expansion • No Resistors Required R_1 and R_2, Figure 2, not required

design example

Design a minimum power memory that has a 200 ns access time, a 1000 ns cycle time, and a 256x8 memory.

Two DM74S287 PROMs will be used for the 256x8 memory. DM74S287s have a ±5% power supply tolerance. Since there will be about a 0.2 V drop across the PNP switch we need to ensure that the V_{CC} requirement of the PROM is met.

Since speed is not of prime importance in this application we will select "slow" low power parts in the power down circuit. The 74C902 noninverting buffer will be used as the logic input device. This device is selected for its low power. 2N3467 PNP switch will be used as the pass transistor.

From the data sheets:

2N3467 PNP Saturating Switch

$V_{CE(SAT)}$	I_C = 150 mA	typ = 0.165	max	= 0.3
h_{fe}	I_C = 150 mA	typ = 120	min	= 40
$V_{BE(SAT)}$	I_C = 150 mA	typ = 0.8	max	= 1 V

DM74S287 PROM

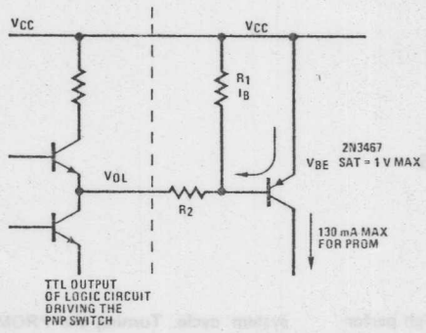
I_{CC} = 80 mA typ, 130 mA max

74C902 Buffer

I_{CC} = 15 μA max

We are now ready to calculate the value of resistor R_2. Resistor R_2 is used to limit the base drive current of the PNP 2N3467 transistor. The value of R_2 is calculated from the voltage across R_2 and the base current required to supply the I_{CC} current required for the PROM.

Resistor calculation:



$$I_B = \frac{130\text{ mA} = I_{CC}}{h_{fe} = 40} = 3.25\text{ mA}$$

min

Base current calculation:

$$R_2 = \frac{V_{CC} - (V_{BE(SAT)} + V_{OL(MAX)})}{I_B + \frac{V_{BE(SAT)}}{R_1 = 820}}$$

$$R_2 = \frac{5 - (1 + 0.5)\text{ V}}{(3.25 + 1.0)\text{ mA}}$$

$$R_2 = \frac{3.5\text{ V}}{4.25\text{ mA}} = 823\ \Omega$$

R_2 = 820 Ω, rounding to the nearest standard value.

R_1 is chosen to be equal to the R_2 to simplify the parts list and this allows resistor packs (8 identical resistors in a 16-pin package) to be used when appropriate.

Figure 3A is the final circuit for the 256 x 8 memory.

Performance of the 256x8 power down memory is:

Power when selected 1345 mW max
Power when deselected 0 mW with 74C902 buffer
Access time 180 ns max

Average power is a function of duty cycle, and for our 256x8 power down example average power is:

$$P_{ave(max)} = \frac{\text{on time}}{\text{off time}}.\quad \text{Power max} = \frac{200\text{ ns}}{1000\text{ ns}}.\ (665)\ (2)$$

$$P_{ave(max)} = \frac{1}{5}(1330) = 265\text{ mW max}$$

The 265 mW assumes that all parts are maximum at the same time. The more likely situation is that parts will be at or near their typical value.

For our example:

$$P_{ave(typ)} = \frac{1}{5}(830) = 166\text{ mW ave}_{typ}$$

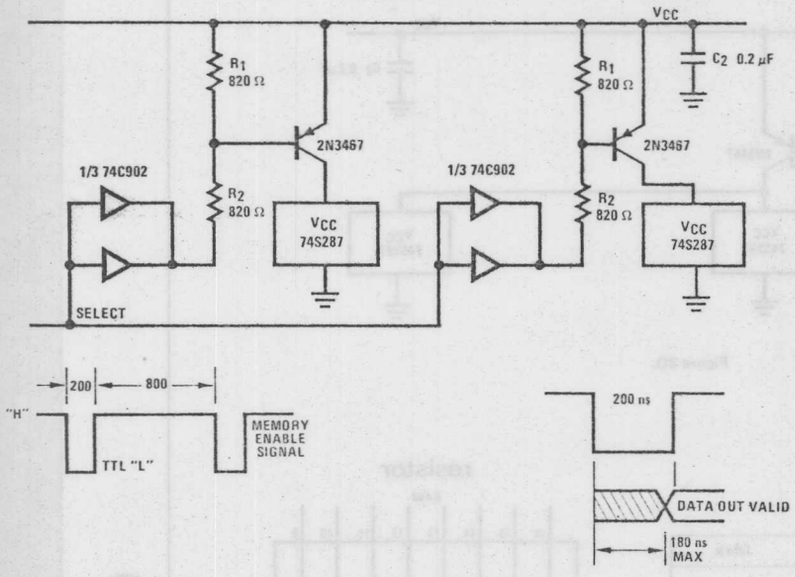


Figure 3A. 256x8 Power Down Memory

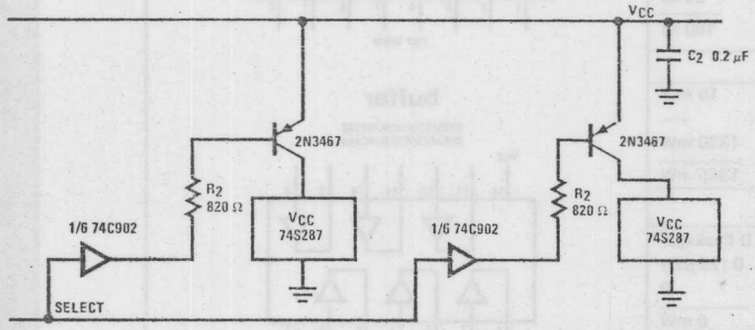


Figure 3B.

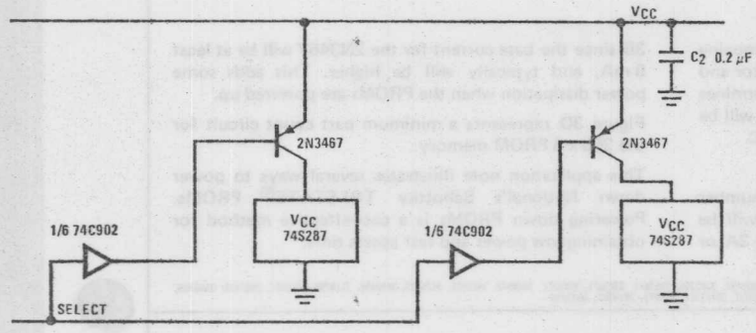


Figure 3C.

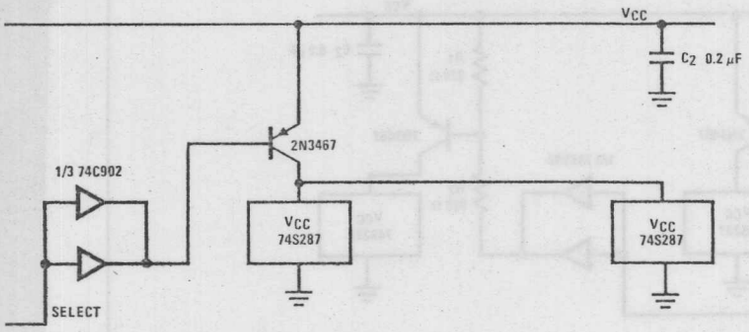
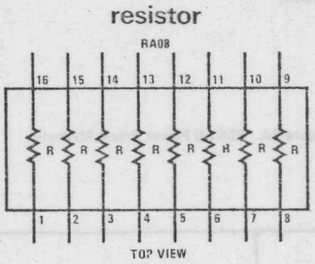


Figure 3D.

performance table

	Typ	Max
Access Time Max		
74C902 Buffer	54 ns	90 ns
2N3467 PNP Switch	20 ns	40 ns
74S287 PROM	35 ns	50 ns
	109 ns	180 ns
Power Selected		
I_B 2N3467		15 mW
74C902		—
74S287 at 5 V, 6.65 mW each		1330 mW
		1345 mW
Power Unselected		
I_B 2N3467		0 (leakage)
74C902		0 (75 μW)
74S287		0
		0 mW

resistor



buffer

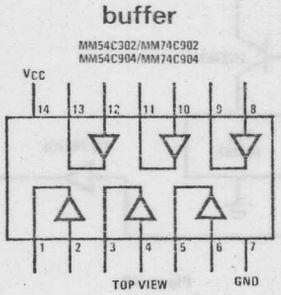


Figure 3B illustrates a circuit simplification of removing R_1 (the I_{b2} resistor). Eliminating R_1 saves a resistor and the power dissipated by the resistor. R_2 still determines the base drive current which is V/R. This circuit will be slightly slower than the circuits in figures 3A or 3C.

Figure 3C illustrates a further reduction in the number of resistors. Neither R_1 nor R_2 is used. Speed will be good and power will be higher than in figures 3A or 3B since the base current for the 2N3467 will be at least 9 mA, and typically will be higher. This adds some power dissipation when the PROMs are powered up.

Figure 3D represents a minimum part count circuit for the 256 x 8 PROM memory.

This application note illustrates several ways to power down National's Schottky TRI-STATE® PROMs. Powering down PROMs is a cost-effective method for obtaining low power and fast access time.

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

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