LMH6533 Four Channel Laser Diode Driver

National Semiconductor
Application Note 1333
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Circuit Description

GENERAL

The LMH™6533 is a 4-channel-input, dual-output laser driver. The dual outputs are meant to drive two different laser diodes, one for CD reading and writing and one for DVD reading and writing. The part has an oscillator that can be set for both amplitude and frequency. The oscillator has two different sets of amplitude and frequency setting resistors, one for the A (CD) output and one for the B (DVD) output channel. The part operates off 5V and can deliver 500 mA of current.

INPUTS

Current-Setting Inputs

The four input channels are transconductance-type inputs. This means the output current the channel contributes is proportional to the current (not voltage) sourced into the input pin. That is why these pins are designated by the letter "I" to indicate the current input nature of the pin. The read channel current-setting pin is "IR", the Channel 2 current-setting pin is "I2" and so on. Using a transconductance-type input eliminates the high-impedance inputs associated with a voltage input amplifier. The lower input impedances of the input nodes lowers the susceptibility of the part to EMI/RFI pickup much in the same way industrial plants use a 4 to 20 mA current loop for sensing and process control. The Read and Channel 3 and 4 current-setting inputs have a gain of 150. Sourcing 1 mA into the pin will give 150 mA from the output. The maximum output current these inputs can set is 150 mA for each of the channels. The Channel 2 input (I2) has a current gain of 300. The maximum output current this input can set is 300 mA. 1 mA into this pin will result in 300 mA output current. The total allowable output current from all the channels operating together is 500 mA.

The current-setting inputs have a voltage compliance to the input current. The voltage at the input will change from about 0.12V with 0.2 mA going into the pin to 0.6V with 1.1 mA going into the pin.

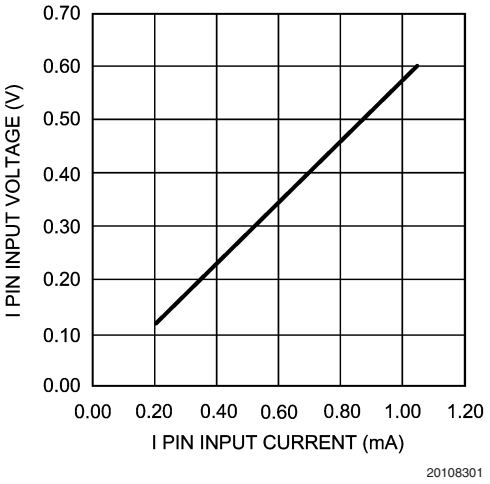

FIGURE 1. INPUT CURRENT VOLTAGE COMPLIANCE

A reasonable maximum voltage for this pin to achieve full channel output is about 0.65V. This means that if the pin is connected to a DAC through a resistor then the maximum voltage that can be generated across the resistor is V_{CC} - 0.65V = 4.35V. In order to generate the 1 mA input current to this pin, the resistor must be less then 4.35 kΩ. In view of supply voltage variations, DAC inaccuracy and worse-case laser driver parameters, a 3.0k resistor is the largest value recommended. This allows the DAC to sweep through the most counts and then set the current output of the device. A resistor as low as 1k can be used but the DAC will be at 1.65V output to give full channel current. DAC settings above 1.65V will not have any effect as the LMH6531 will be saturated and in the full output state for that channel.

Circuit Description (Continued)

CHANNEL ENABLE INPUTS

Each of the four channels have enable inputs that allow the channel to be turned on or off. The read channel enable (ENR) is a single-ended TTL/CMOS compatible input. A single-ended signal is adequate for this channel because the read channel is generally enabled the entire time the drive is reading or writing. This is because even during writing the drive always reverts to read mode between write pulse. This is so the drive can still read the wobbled groove track on the disk and servo the OPU (Optical Pickup Unit) to keep the laser focused and aimed at the proper point on the disk. The three write/erase channels need to be operated much faster as the drive performs writes so these channel enables are LVDS (Low Voltage Differential Signal) inputs. Each channel has two inputs, such as EN2 and EN2B. The inputs need only change a small voltage, about 200 mV or so, but in opposite direction, in order to enable or disable the channel. The inputs should be biased at 1.2V common-mode voltage. A high level would be 1.3V and a low level would be 1.1V. The small swing and differential nature of these inputs allows very fast digital signaling. The EN2 input is the same phase as the output; when it is high the output is high. The EN2B input is the opposite. The LVDS inputs for the three write/erase channels have a 100Ω termination resistor built into the chip. This provides the LVDS termination without the need for external components, simplifying layout and assembly.

CONTROL INPUTS

There are two control inputs (except the oscillator enable which is covered in the next section). There are the global chip Enable and output select pin SELB. Bringing the Enable pin high (TTL/CMOS levels) will enable the part. The supply current will go from about 8 µA to around 40 mA. The SELB pin controls which output pin is active. When it is high (TTL/CMOS levels) the “B” (DVD) output is active. Changing this pin also changes the oscillator frequency and amplitude based on the setting resistors described in the next section.

OSCILLATOR INPUTS

The oscillator section has five inputs. One input (ENOSC) enables and disables the oscillator. Bringing this input high (TTL/CMOS levels) will enable the oscillator. The other four inputs set the oscillator frequency and amplitude for the A and B outputs. R_{FA} and R_{FB} pins set the oscillator frequency for the A and B outputs respectively. The R_{AA} and R_{AB} pins set the oscillator amplitude for the A and B channels respectively. These four inputs work by having current drawn out of the pin by a setting resistor or potentiometer. The greater the current drawn from the pin the higher the frequency or the larger the amplitude. This implies that the smaller the resistor (or potentiometer setting) hooked to the pin, the higher the frequency or amplitude. There are two charts in the Typical Performance Characteristics section that relate the setting resistor value to the resultant frequency or amplitude.

OUTPUTS

The outputs can source up to 500 mA. The output pins have been designed to have minimal series inductance in order to minimize current overshoot on fast pulses. The outputs have a saturation voltage of about 1.3V. The following Table below show the typical output saturation voltages into a 10Ω and a 5Ω load at various supply voltages.

TABLE 1. OUTPUT SATURATION

Supply Voltage (V)	Maximum Output (mA) 10Ω	Saturation Voltage (V)
4.5V	375	0.75
5.0V	415	0.85
5.5V	450	1.0
Supply Voltage (V)	**Maximum Output (A) 5Ω**	**Saturation Voltage (V)**
4.5V	646	1.07
5.0V	727	1.22
5.5V	788	1.33

As can be seen, even with a 4.5V supply voltage the part can deliver 375 mA while the saturated output is at 3.75V. This insures that the part can adequately drive laser diodes with as much as 3V of forward voltage. When using a 5Ω load the part can deliver 788 mA while the saturated output voltage is at 3.95V. This includes a supply voltage loss of 0.23V caused by the high output current through the supply lines.

Application Hints

SUPPLY SEQUENCING

As the LMH6533 is fabricated in the VIP10C process, latch-up concerns are minimal. Be aware that applying a low impedance input to the part when it has no supply voltage will forward bias the ESD diode on the input pin and then source power into the V_{CC} pin. If the potential exists for sustained operation with active inputs and no supply voltage, all the active inputs should have series resistors to limit the current into the input pins to levels below a few milliamperes.

DECOUPLING

The LMH6533 has very high output currents that change radically in less then a nanosecond. This makes decoupling especially important. Good, low impedance, ceramic capacitors should be located as close as possible to the supply pins. The LMH6533 needs two decoupling capacitors, one for the analog power and ground (V_{CCA}, GNDA) and one for the power side supply and ground ($3xV_{CC}$ and GNDB). The high level of output current dictates that the power side decoupling capacitor should be 0.1 µF at the minimum. Larger values may improve rise times depending on the layout and trace impedances of the connections. The capacitors should have direct connections across the supply pins on the top layer, preferably with small copper-pour planes. These planes can connect to a bottom side ground and/or power planes with vias but there should be a topside low impedance path with no vias if possible.

OVERSHOOT

As the LMH6533 has extraordinarily fast rise times of around a nanosecond, any inductance in the output path will cause overshoot. This includes the inductance in the laser diode itself, as well as any trace inductance. A snubber network is recommended to reduce overshoot where needed. Typical

Application Hints (Continued)

values are 15Ω and 150 pF. The actual values required depend on the laser diode used and the circuit layout . They should be determined empirically.

Thermal

GENERAL

The LMH6533 is a very high current output device. This means that the device must have adequate heat-sinking to prevent the die from reaching its absolute maximum rating of 150˚C. The primary way heat is removed from the LMH6533 is through the Die Attach Pad, the large center pad on the underside of the device. Heat is also carried out of the die through the bond wires to the traces. The outputs and the V_{CC} pads of the device have double bond wires so that they will conduct about twice as much heat to the pad. In any event, the heat transferred out by the bond wires is far less than that which can be conducted out of the die attach pad. Heat can also be removed from the top of the part but the plastic encapsulation has thermal conductivity 450 times worse then copper. This means a heat sink on top of the part is less effective than the same copper area on the circuit board that is thermally attached to the die attach pad.

PCB HEAT SINKS

In order to remove the heat from the die attach pads there must be a good thermal path to large copper pours on the circuit board. If the part is mounted on a dual-layer board the simplest method is to use six or eight vias under the die attach pad to connect the pad thermally (as well as electrically, of course) to the underside of the circuit board. The vias can then attach to a copper pour that is as large as possible. Since the LMH6533 uses the VIP10C dielectrically isolated process there is a thin layer of glass (dielectric) in the middle of the die that electrically isolates all the chip circuitry from the underside of the die. This means the die attach pad could, if needed, be connected to a node other than the system ground. Usually, however, the pad will be attached to a ground plane on the underside of the board. On such a two-sided board the heat can be conducted through vias to the underside of the board. Please see application note AN-1187 for guidelines about these vias and LLP packaging in general.

DERATING

It is essential to keep the LMH6533 die under 150˚C. This means that if there is inadequate heat sinking the part may overheat at maximum load while at maximum operating ambient of 85˚C. How much power (current) the part can deliver to the load at elevated ambient temperatures is purely dependent on the amount of heat sinking the part is provided with. There is a convenient way to determine if the die is overheated by using an ESD diode. The forward voltage of a diode operating at a given current has a very linear relationship to temperature. The following chart shows this relationship measured for two different currents. One current is +100 µA and the other is −100 µA. This gives two curves showing the relation between the forward voltage vs. the temperature.

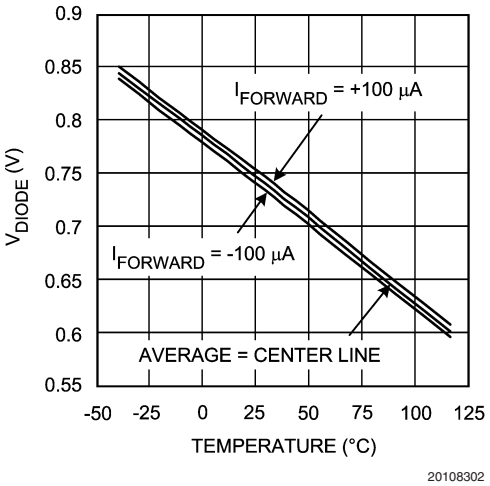

FIGURE 2. Diode Voltage Characterization

This relationship was measured while the part was turned off so that no other current has to be taken into account. For calculation of the right die temperature the absolute values of both diode forward voltages must added and divided by two. This gives a fairly good result for the die temperature. It is not possible to measure between both pins of the temperature diode. Pin 3 of the package of the LMH6533 is directly connected to the ESD diodes and the other connection is established by connecting the diodes to the ground pin. Between this diode connection and the ground pin of the package exists a small resistance. But if high currents are flowing through the part the measured voltage at pin 3 is a little bit lifted due to these currents which will cause a wrong temperature measurement.

Thermal (Continued)

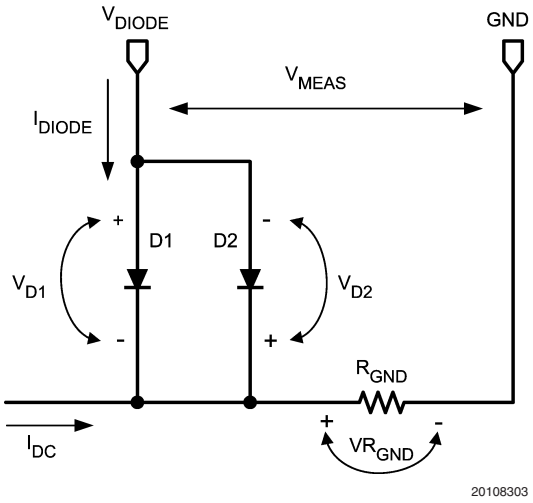

FIGURE 3. Temperature Diodes Input Circuity

While using two measurements with two different polarized currents, it is possible to eliminate the influence of the high DC current. The expression for V_{MEAS} with +100 µA is:

$V_{MEAS+} = (I_D*R_D)+(I_D+I_{DC})*R_{GND}$

The same expression for the opposite current is:

$V_{MEAS-} = (-I_D*R_D)+(-I_D+I_{DC})*R_{GND}$

After reworking this formula it is:

$V_{MEAS+} = I_D*(R_D+R_{GND})+I_{DC}*R_{GND}$ and

$V_{MEAS-} = -I_D*(R_D+R_{GND})+I_{DC}*R_{GND}$

After simplifying this formula it is:

$V_{MEAS+} = I_D*R_X+I_{DC}*R_{GND}$ where $R_X = R_D+R_{GND}$

$V_{MEAS-} = -I_D*R_X+I_{DC}*R_{GND} - V_{MEAS} = 2I_D*R_X$

It can be seen now that the measured voltage depends only on I_D and the two the resistors, and there is no dependency any more of the DC current through the device. After dividing this result by 2, it is possible to read in the curve the actual die temperature. This is possible because the R_{GND} shows over temperature a low variation compared to the variation of the ESD diode. Above this the contribution of the R_{GND} to the total measured voltage is very low.

Layout

INPUTS

The most critical inputs are the LVDS inputs. These should be routed together and enclose a minimum loop area. As the differential impedance is 100Ω the single-ended impedance of each LVDS input should be 50Ω to ground. For the motherboard and the flex circuits with ground planes (dual layer) the correct width of the traces can be calculated using Transmission Line Rapidesigner, which is available from the National Semiconductor's Interface Products Group.

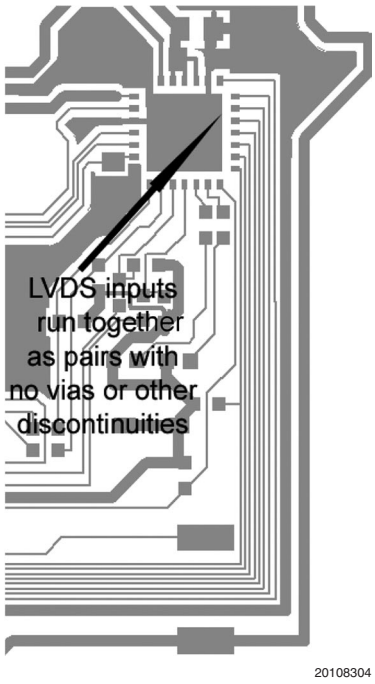

FIGURE 4. LVDS Inputs

Application Note AN-905 details the use of this paper slider-ule nomograph. For a DVD drive main-board the Rapide-signer shows that to get a 50Ω trace on an FR4 circuit board (dielectric constant of 4.3) with the ground plane 20 mils below the signal lines, the trace width needs to be 36 mils. For flex circuits the dielectric constant of the insulation must be used as well as the distance between layers. If the two LVDS input traces run close to each other this will effect the characteristic impedance. It is recommended that the imped-ance be checked with a TDR (Time Domain Reflectometer). Be aware that differential inputs do not return the signal current though the other line. The return current is provided by the ground plane. This is why running LVDS signals on single-sided flex circuits can be tricky. There should be a return path for the input current that is parallel to and close to each input line. The characteristic impedance of the lines should be evaluated with a TDR to insure that it is as close as possible to 100Ω with no discontinuities that would cause reflections and ultimately, write errors. The Read Enable and Enable inputs are slower and much less critical. The Oscil-lator Enable input is toggled in concert with the write pulse so special attention should be given to this signal to insure it is routed cleanly. It may be desirable to put a termination resistor close to the LMH6533 for the Enable Oscillator line to achieve the best turn-on and turn-off performance of the oscillator.

Layout (Continued)

OUTPUTS

In order to achieve the fastest output rise times the layout of the output lines should be short and tight. It is intended that the Output B trace be routed under the decoupling capacitor and that the ground return for the laser be closely coupled to the output and terminate at the ground side of the decoupling capacitor.

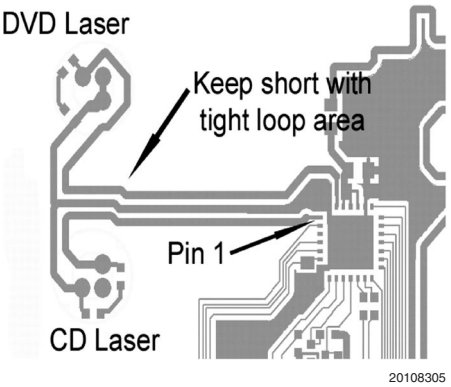

FIGURE 5. Laser Connections

The capacitance on the output lines should also be reduced as much as possible. This implies removing any ground plane from under the output lines that is not used to return the laser current. As always the loop area of the laser current should be minimized and it is necessary to think in three dimensions, paying attention to the distance between the layers as well as the proximity of the output and return traces on the same layer.

DECOUPLING CAPACITORS

As mentioned before, the decoupling capacitors are critical to the performance of the part. The output section stated that the power-side decoupling capacitor should be as close as possible to the V_{CC} and GND pins and that the B output should pass under the decoupling capacitor. Similarly the analog-side decoupling capacitor should be as close as possible to the $V_{CC}A$ and GNDA pins. The figure below shows a layout where the analog (V_{CCA} and GNDA) decoupling capacitor C_1 is placed next to pins 6 and 7. (Note the layout is rotated 90 degrees from the last figure.) The ground extends into a plane that should connect to the oscillator amplitude and current setting resistors. C_2 is the power-side decoupling capacitor and it has been placed as close to the V_{CC} and GNDB pins as possible while straddling the B output trace. This layout has also provided for a second power decoupling capacitor C_3 that connects from V_{CC} to a different GND copper pour. It must be noted that the two ground planes extending from C_2 and C_3 must be tied together. This will be shown in the thermal section. Bear in mind that the closeness of the parts to the LMH6533 may be dictated by manufacturing rework considerations, such as that the LMH6533 can be de-soldered with a hot-air rework station without the need of removing the capacitors. The relevant manufacturing organization provides guidelines for this minimum spacing.

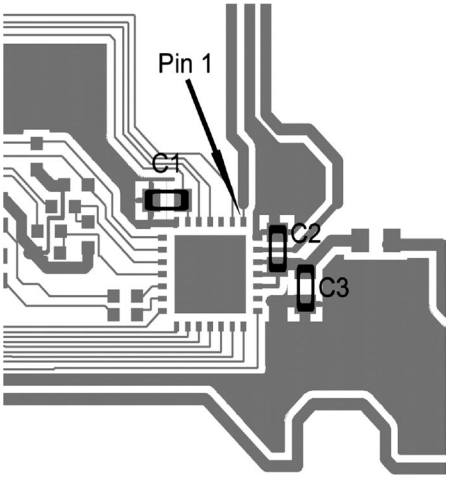

FIGURE 6. Decoupling Capacitors

OSCILLATOR RESISTORS

The resistors and/or potentiometers used to set the oscillator frequency or amplitude should be as close to the part as possible. The low current in these parts makes 0402 and even 0201 size resistors practicable. If the grounds are split when using a single-sided flex circuit, it is essential that these resistors and potentiometers share the same ground as the GNDA pin and the decoupling capacitor.

THERMAL

As mentioned previously, the primary way to get heat out of the LLP package is with the large Die Attach Pad at the center of the LMH6533 underside. On two-layer circuits this can be done with vias. On single-sided circuits the pad should connect with a copper pour to either the GND pin or, if a better thermal path can be achieved, with the V_{CC} pins. Be aware that the unused pins on the part can also be used to connect a copper pour area to the Die Attach Pad. *Figure 7* (with the same orientation as the first layout example) shows the unused pin being used to provide a thermal path to the copper pour heat sinks. In this layout the analog ground has been separated from the power ground so that pin 7 is not connected to the Die Attach Pad even though it would help remove heat from the part. The layout of *Figure 7*

Layout (Continued)

is based on a single-sided circuit board. If a dual-sided circuit board was used there would also be vias on the Die Attach Pad that would conduct heat to a copper plane on the underside of the board.

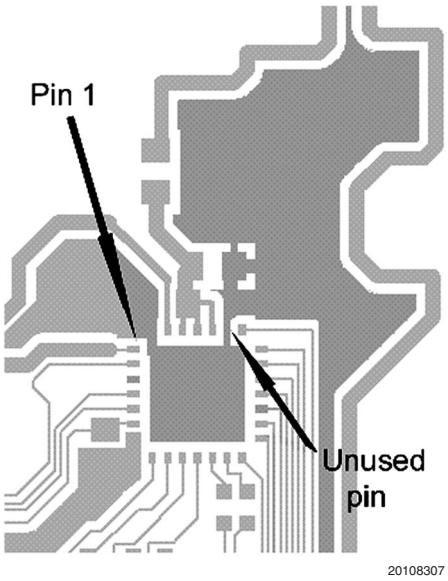

FIGURE 7. Heat Sinking

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