DP83640 Synchronous Ethernet Mode: Achieving Sub-nanosecond Accuracy in PTP Applications

National Semiconductor
Application Note 1730
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1.0 Introduction

Synchronous Ethernet at 100 Mb/s, a feature unique to the National Semiconductor DP83640, enables very accurate synchronization between IEEE 1588 Precision Time Protocol (PTP) systems connected via Ethernet. Using this feature, it is possible to maintain sub-nanosecond master to slave synchronization precision in PTP applications operating within required network topological constraints. It is also possible to generate a slave node clock output which is locked and aligned to the Master PTP clock.

This application note first provides a summary of empirical results found when master to slave node synchronization is measured with Synchronous Ethernet mode enabled. Background information is then provided describing the operation of and topological constraints associated with Synchronous Ethernet mode. Typical applications are then described, followed by empirical data which clearly demonstrates the accuracy potential of using Synchronous Ethernet mode.

This application note is applicable to the following products:

DP83640

2.0 Measuring Synchronization

Synchronization accuracy can be defined as the instantaneous time difference between a master clock counter and a corresponding synchronized slave clock counter. Accuracy is determined by measuring the time difference between a master signal which is triggered at a specific time, and a corresponding slave signal which is triggered at the same time using the slave's local synchronized clock counter. Usually, in the context of PTP discussions, these triggered signals occur at 1 second intervals, and are referred to as Pulse Per Second, or PPS, signals.

Depending on the accuracy of the master to slave synchronization, it is also possible to directly measure the phase relationship between outputs from the Master and Slave PTP clocks which control the PTP counters.

In doing such a measurement repeatedly over extended periods, statistical data is gathered which provides a mean, a standard deviation, and a maximum time or "Peak-to-Peak" difference between master and slave clock or PPS signals.

When a slave device is connected to and synchronized with a master device, a fixed phase relationship is established between the master and the slave PTP clocks. This fixed phase relationship is measured as the mean of the statistical data accumulated over time. The extent that this phase relationship can vary is constrained by the resolution of the internal PTP counter. In the DP838640T device, the internal PTP counter (or digital clock) updates in 8 ns increments at a rate of 125 MHz. Thus, the fixed phase relationship, or mean, established between a master and slave device can vary from +8 to -8 ns. Additional variation may also result from any asymmetry in the physical bidirectional path between the master PTP clock and the slave PTP clock.

The mean remains fixed for as long as a synchronization connection is maintained. However, when this connection is broken and then re-established, a new fixed mean is established within the constraints of the sampling clock.

For the purpose of this document, the term "Precision" is used to describe the standard deviation measured between a master and a slave signal corresponding to a fixed mean while synchronization is established.

3.0 Results Summary

In point-to-point connected PTP systems configured for Synchronous Ethernet operation, tests conducted over extended periods under nominal conditions show master clock to slave clock synchronization can achieve a precision of less than 100 ps with a peak-to-peak measurement of less than 1 ns. These results are roughly 100 times more accurate than similar tests performed with Synchronous Ethernet mode disabled.

Empirical data also demonstrates the ability to produce a slave clock of up to 125 MHz which is locked and aligned to a network connected PTP master clock. Even higher frequency locked clocks are attainable using an external precision clocking device, such as the NSC LMK3000 family of devices.

It is also noteworthy to mention that with Synchronous Ethernet mode enabled, the effects of any local slave reference clock instability are eliminated, since the slave PTP clock is locked to the master clock.

4.0 Background

The IEEE 1588 Precision Time Protocol provides networked, packet-based synchronization between master and slave systems. When implemented as a purely software-oriented process, systems typically achieve synchronization precision on the order of milliseconds.

By including the hardware-oriented advantages provided by the DP83640 in a PTP-enabled point-to-point connection, it is possible to achieve precision of under 10 ns.

Additionally, by enabling Synchronous Ethernet mode, it is possible to achieve sub-nanosecond precision in point-to-point connections.

In order to utilize Synchronous Ethernet mode, a network system must meet certain topological constraints. To help explain these constraints, some key terms, the internal clocking architecture of the device, and the network topology requirements are described below.

4.1 KEY TERMS

Master Node: A master node is a Precision Time Protocol (PTP) enabled network node which contains or propagates a Master PTP clock signal and Master PTP counter data.

Slave Node: A slave node is a PTP-enabled network node which contains a Slave PTP clock and counter. A slave node is usually connected to a master node via a network connection. PTP is used to synchronize the slave PTP clock and counter to a master PTP clock and counter.

PTP Clock: A PTP clock is the source of an output clock signal which is locked to a PTP counter. In the DP83640, the local PTP clock operates at 250 MHz, and can be configured

to control the CLK_OUT signal. This PTP CLK_OUT signal is programmable to frequencies which are integral divisions of the 250 MHz PTP clock in the range of 2 and 255 (125 MHz to 0.98 MHz).

PTP Counter: A PTP counter contains time information, and is locked to the PTP clock. In a master node, the PTP counter is the source of data used in the Precision Time Protocol for the purpose of synchronizing counters in PTP slave nodes. The PTP counter is incremented every 8 ns.

Local Reference Clock: A local reference clock is used for generating network traffic. The local reference clock is embedded into the transmit network packet traffic and is recovered from the network packet traffic at the receiver node. All Ethernet Physical Layer devices use local reference clock sources. Internally, the local reference clock in the DP83640 operates at 125 MHz.

4.2 KEY CONFIGURATION REQUIREMENTS

For a network node to function as a PTP slave device, the node must be attached to a partner (node, switch, or repeater) which provides access to a Master PTP clock, and the PTP protocol must be enabled and active.

In addition, the partner must have its local reference clock frequency locked to the PTP master clock. If PTP clock phase alignment between the master and slave is also desired, the PTP master clock must be phase-aligned with the master PTP counter. (For information on phase aligning the output clock in the DP83640, see application note AN—1729 – "DP83640 IEEE 1588 PTP Synchronized Clock Output".)

It is also important to note that Synchronous Ethernet mode should only be enabled in a device which is utilized as a slave PTP clock node. Enabling Synchronous Ethernet mode in a master node will produce undesired results.

4.3 ENABLING SYNCHRONOUS ETHERNET MODE

Synchronous Ethernet mode must be enabled in nodes which are designated as slave nodes only. Synchronous Ethernet mode is enabled by simply setting the SYNC_ENET_EN bit of the PHYCR2 Extended Page 0 register to 1 (Reg 0x1C:13 = 1).

4.4 DP83640 CLOCKING ARCHITECTURE

The DP83640 has several internal clocks, including the local reference clock, an Ethernet receive clock, and a PTP clock signal source. An internal PTP digital counter is also included, as well as logic which controls the rate (frequency) of both the digital counter and the PTP clock. (See *Figure 1*.)

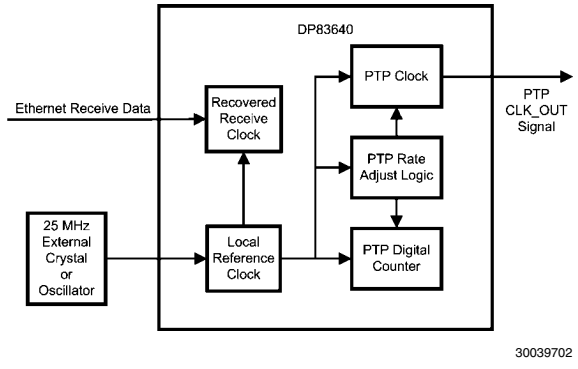

FIGURE 1. DP83640 Internal Clocks with Synchronous Ethernet Mode Disabled

An external crystal or oscillator provides the stimulus for the local reference clock. The local reference clock acts as the central source for all clocking in the device. The Receive Clock is recovered from the received Ethernet packet data stream and is locked to the Transmit Clock in the partner.

In normal operation, IEEE 1588 PTP packets are utilized to match the PTP clock and counter in the slave device to the PTP clock and counter in the master device. This matching is accomplished by controlling the rate adjust logic.

When Synchronous Ethernet mode is enabled, control of the PTP clock, digital counter, and PTP rate adjust logic is switched from the local reference clock to the recovered receive clock (see *Figure 2*). This has the effect of locking the PTP clock and counter of the slave system to the PTP clock and counter of the master system. Consequently, synchronization accuracy is increased dramatically (see *Figure 3*).

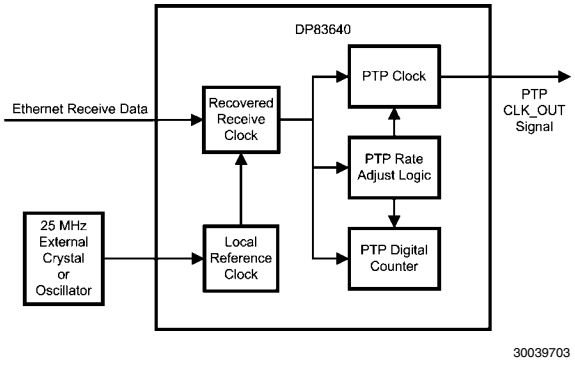

FIGURE 2. DP83640 Internal Clocks with Synchronous Ethernet Mode Enabled

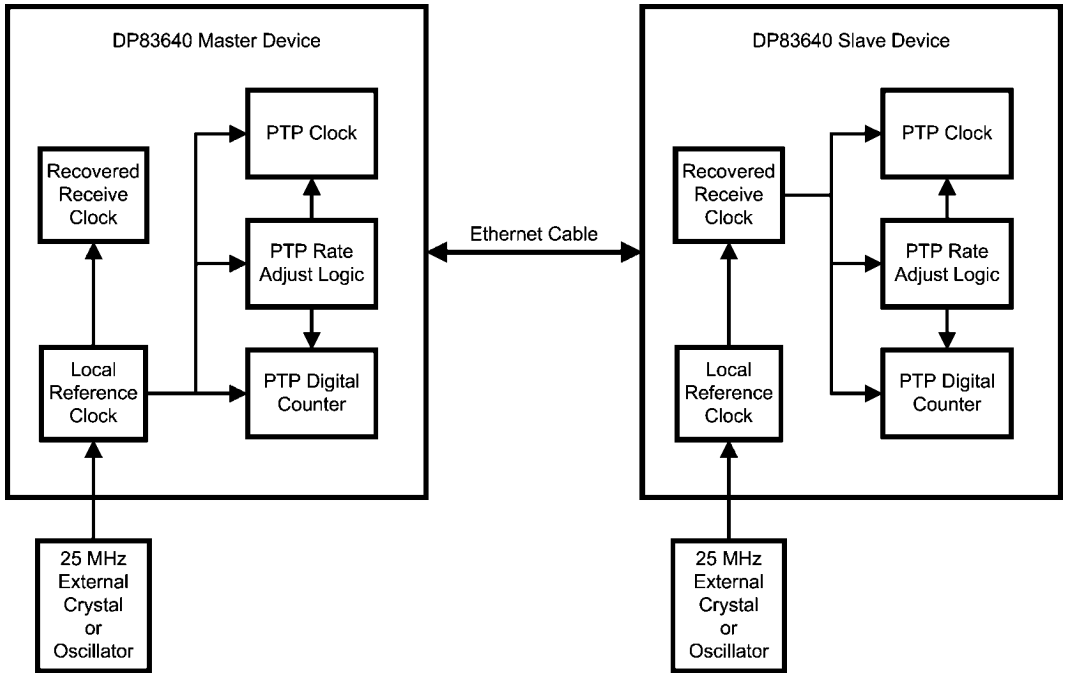

FIGURE 3. DP83640 with Synchronous Ethernet Mode Enabled in a Point to Point Network Topology

4.5 SYSTEM TOPOLOGY CONSIDERATIONS

As mentioned earlier, for Synchronous Ethernet mode to function, the master node reference clock must be locked to the master PTP clock. This is the default configuration when the DP83640 local reference clock is used by the PTP digital counter and PTP clock. If an external PTP clock source is used in a master system, an external PLL can be used to lock the reference clock source to the external PTP clock.

Note that it is not necessary for a master PTP clock node to utilize a DP83640 device for Synchronous Ethernet mode to function in attached DP83640 slave nodes. Phase locking an external PTP clock to the reference clock input of any Ethernet Physical Layer Interface (Phy) device will suffice.

It is possible to synchronize multiple slave devices to a single master clock if a hub or switch architecture is utilized that synchronizes all Ethernet channels to the master PTP clock. See *Figure 4*.

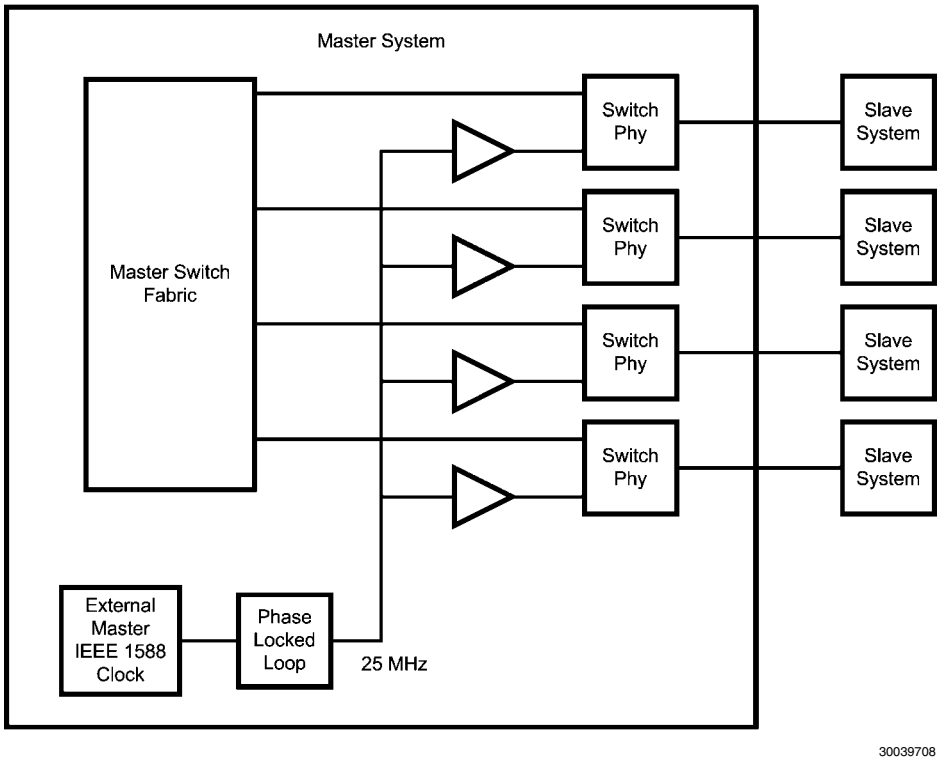

FIGURE 4. Distributed Master Clock Switch Topology

Similarly, it is possible to propagate Synchronous Ethernet mode operation through a switch tree in which each slave switch node synchronizes itself to a master network source connection. (See *Figure 5*.)

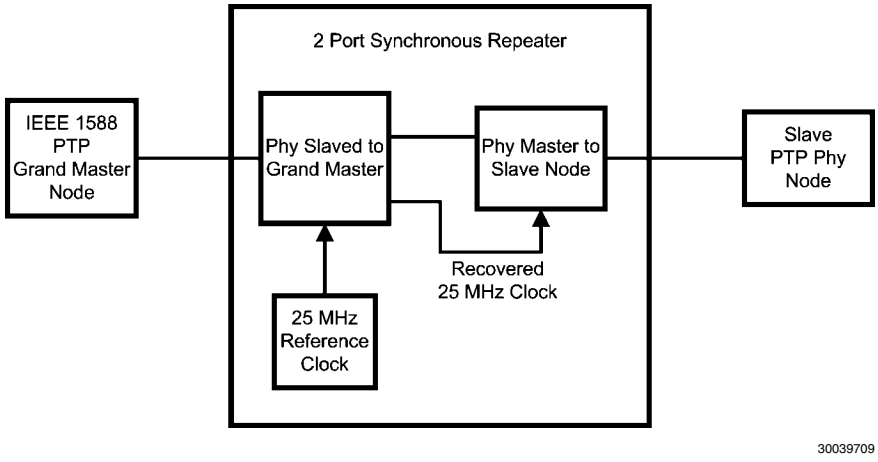

FIGURE 5. 2 Port Synchronous Repeater System

5.0 Typical Applications

A typical application for Synchronous Ethernet mode is instrumentation that requires very precise data logging. Using the distributed node example of *Figure 4*, a master system may trigger a stimulus, such as an energy burst, and each slave node may represent a precision instrument or sensor used to measure the effects of the stimulus at precise times.

Additionally, it may be desirable for an application to propagate a locked clock across several instruments within a local network. Given 1 ns peak-to-peak precision, with Synchronous Ethernet mode enabled, it is possible to trigger multiple instruments to sample data synchronously using 125 MHz output clocks. A greater variety of frequency options become available by using the output clock of the device to control an external PLL clock source, such as a National Semiconductor LMK3000 series device.

Finally, since the frequency of the master clock is delivered through the network, the stability of the local oscillator is not a significant source of error when Synchronous Ethernet

mode is enabled. The stability of a slave node is directly dependent upon the stability of its corresponding PTP connected master node. Therefore, special environmental controls are not necessary to maintain synchronization precision. The slave node will achieve the same level of precision with a standard 25 MHz crystal as it would with a high-stability OCXO.

6.0 Synchronization Measurement Setup

As mentioned earlier, synchronization accuracy can be measured by using an oscilloscope to compare the delay between an output signal from a master clock source or node to the corresponding synchronized signal from a slave node. Typically, master and slave output signals are connected to inputs on a scope. The master signal is used to trigger the scope, and the slave signal time is measured against the master trigger signal.

With some oscilloscopes it is possible to enable a histogram function. By accumulating a large sample of slave node output signals, statistical information about the relative synchronization of a slave node to a master mode can be established.

In IEEE 1588 applications, synchronization is typically measured by connecting a pulse per second (PPS) trigger output from a master device and a corresponding PPS signal from a slave device.

Using the DP83640, it is possible to measure synchronization using either output triggers (including a periodic PPS output trigger), or using the actual PTP clock signal, which can be programmed to output on the CLK_OUT pin (pin 24) of the device. See *Figure 6*.

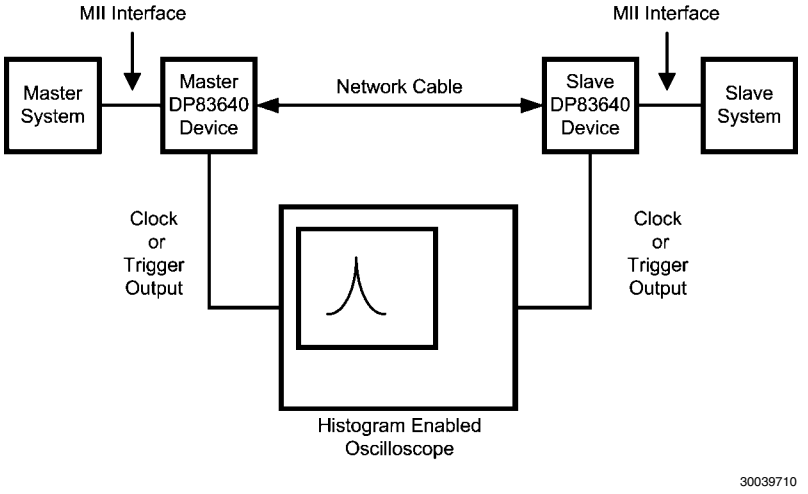

FIGURE 6. Synchronization Measurement Setup

For the purpose of this application note, measurements were taken using two DP83640 Demo Cards used as Master and Slave devices, connected together using a 1 meter cable. Master devices used OCXO 25 MHz reference clock sources. Slave devices used both OCXOs and crystals, to illustrate the immunity that Synchronous Ethernet mode affords against local temperature / frequency instability. Measurements were taken under nominal conditions, using 3.3 V VCC in 25 °C room temperature conditions. Measurements were taken using a Tektronix 784C Oscilloscope.

7.0 Measurement Results

Table 1 summarizes the long term (several hours) accumulation of synchronization data under nominal conditions. The statistical data represents the time measured between a master oscilloscope trigger signal and corresponding slave signal over an extended period. The associated histogram for each line in the data table is also represented in an attached scope plots.

Test Number 1 in *Table 1* (*Figure 7*) presents synchronization data taken with Synchronous Ethernet mode disabled for comparison purposes. This data was taken with both master and slave devices utilizing very stable OCXO reference clock sources. It can be seen that the standard deviation of the distribution of captured slave clocks when measured against a master clock is about 5 ns, with a maximum peak-to-peak measurement of about 48 ns.

Test Number 2 (*Figure 8*) presents data taken in the same configuration with Synchronous Ethernet mode disabled, but using a crystal as a slave reference clock source for comparison. It can be seen that the standard deviation almost doubles to about 9.5 ns, with a maximum peak-to-peak measurement of about 119 ns. With a maximum peak-to-peak measurement greater than 100 ns, it is impossible to obtain a stable 10 MHz signal histogram trace, so 1 MHz clock output signals were used instead.

To contrast, Test Number 3 (*Figure 9*) shows a standard deviation of about 80 ps with Synchronous Ethernet mode enabled, and a peak-to-peak measurement of about 900 ps. This is more than 50 times more precise than the corresponding data with Synchronous Ethernet mode disabled (Test Number 1, *Figure 7*).

Test Number 4 (*Figure 10*) shows data from the same configuration with Synchronous Ethernet mode enabled, but again using a crystal as a slave reference clock source for comparison. With a standard deviation of about 77 ps and a peak-to-peak measurement of about 700 ps, the immunity to local clock instability that Synchronous Ethernet mode provides is clearly illustrated. This is roughly 100 times more precise than comparable data with Synchronous Ethernet mode disabled.

Test Number 5 (*Figure 11*) is useful for comparing data representing the synchronization of a 10 MHz CLK_OUT signal to the synchronization of a Pulse Per Second trigger output. The data shows that while the standard deviation is comparable to similar 10 MHz CLK_OUT data (Test number 3,) the peak-to-peak measurement of the data doubles to about 2 ns.

Finally, Test Number 6 (*Figure 12*) shows that 125 MHz master to slave clock output performance is comparable to the 10 MHz clock output performance, with a standard deviation of about 79 ps and a maximum spread of about 760 ps.

TABLE 1. Synchronization Output Test Results

Test Number	Synch Ethernet Enabled	Master Reference Clock	Slave Reference Clock	Measured Output	Mean	Standard Deviation	Peak-to-Peak	Reference Figure
1	No	OCXO	OCXO	10 MHz CLK_OUT	-2.148 ns	5.237 ns	48.3 ns	*Figure 7*
2	No	OCXO	Crystal	1 MHz CLK_OUT	-543 ps	9.537 ns	119.25 ns	*Figure 8*
3	Yes	OCXO	OCXO	10 MHz CLK_OUT	319 ps	80.6 ps	900 ps	*Figure 9*
4	Yes	OCXO	Crystal	10 MHz CLK_OUT	784 ps	77.5 ps	700 ps	*Figure 10*
5	Yes	OCXO	OCXO	1 Pulse Per Second Trigger Out	1.005 ns	82.8 ps	2.02 ns	*Figure 11*
6	Yes	OCXO	OCXO	125 MHz CLK_OUT	667 ps	78.7 ps	760 ps	*Figure 12*

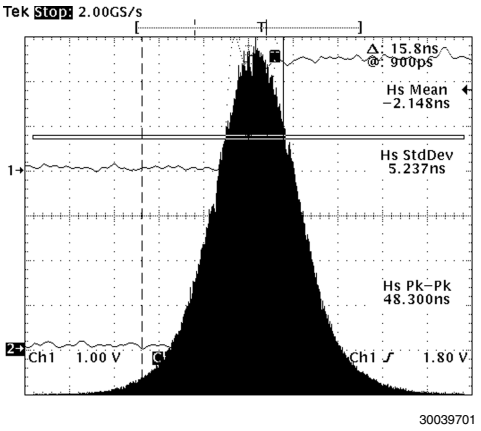

FIGURE 7. Master to Slave 10 MHz CLK_OUT Synchronization with Synchronous Ethernet Mode Disabled

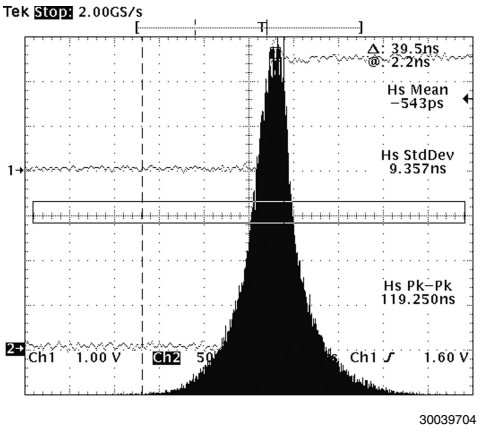

FIGURE 8. Master to Slave 1 MHz CLK_OUT Synchronization with Synchronous Ethernet Mode Disabled and Crystal Slave Reference Clock

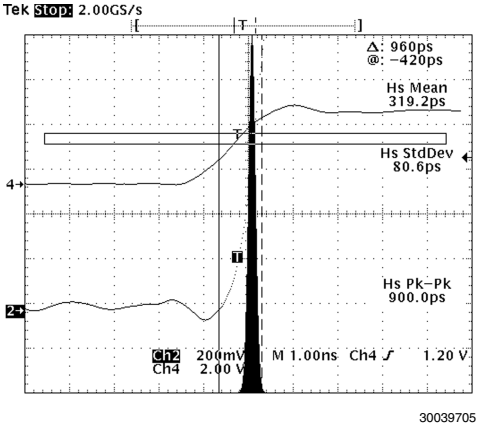

FIGURE 9. Master to Slave 10 MHz CLK_OUT Synchronization with Synchronous Ethernet Mode Enabled

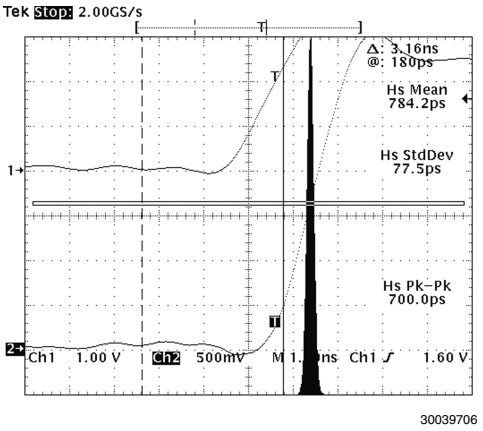

FIGURE 10. Master to Slave 10 MHz CLK_OUT Synchronization with Synchronous Mode Enabled and Crystal Slave Reference Clock

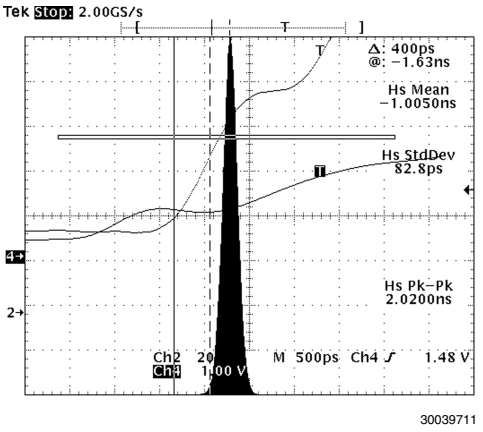

FIGURE 11. Master to Slave Synchronization Pulse Per Second Trigger Output with Synchronous Ethernet Mode Enabled

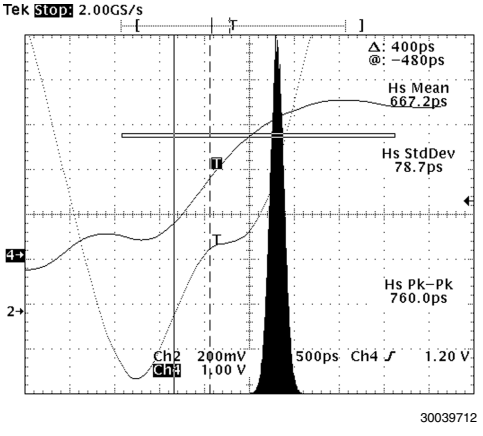

FIGURE 12. Master to Slave Synchronization 125 MHz CLK_OUT with Synchronous Ethernet Mode Enabled

8.0 Conclusion

The benefit of the National Semiconductor DP83640 Synchronous Ethernet mode feature is clearly demonstrated through the provided empirical data. It is shown that by using Synchronous Ethernet mode, precision can be improved by over 100 times when compared with results from comparable configurations with Synchronous Ethernet mode disabled.

When utilized within a PTP enabled network environment, Synchronous Ethernet mode can be useful for any application requiring sub-nanosecond precision when recording data. Synchronous Ethernet mode is also useful for applications requiring a precise locked extension of a Master clock source across a network link, or isolation from the effects of local reference clock instability in a synchronized slave system.

While the precision improvement is dramatic, network topology constraints must be met for the proper use of Synchronous Ethernet mode. These constraints include phase locking the master PTP clock to the master physical layer clock and utilizing a direct connect link between a frequency locked network path between a phase locked master PTP clock node and a slave PTP clock node.

Notes

Notes

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