

LMH730033 Evaluation Board

National Semiconductor
Application Note 1808
Mike Stout
February 26, 2008

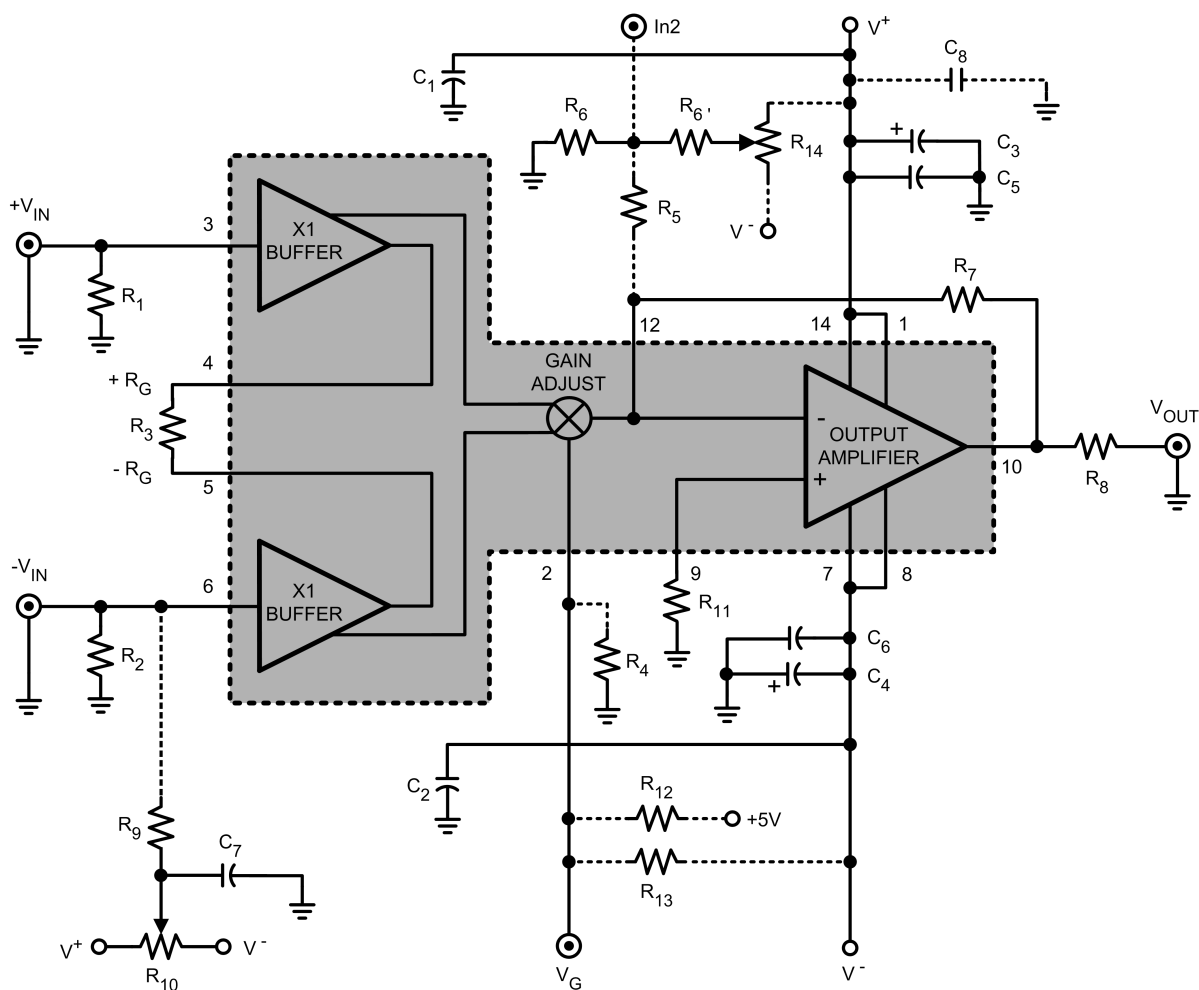


LMH730033 Evaluation Board

Complete Schematic

Figure 1 shows the complete evaluation circuit implemented on this board. The primary connections are shown with solid

lines, while several optional circuit connections are shown with dashed lines. Shaded area is inside the device.



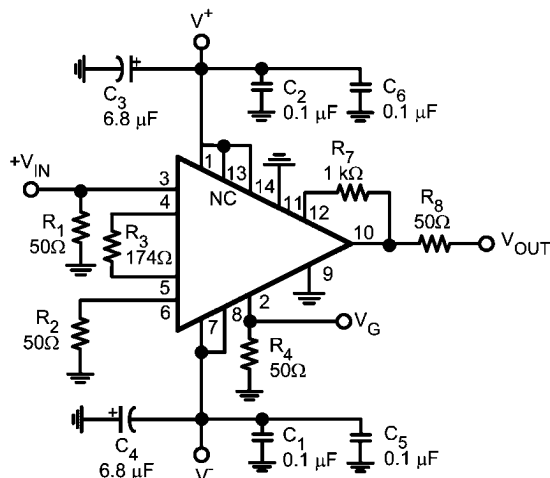
30055901

FIGURE 1. External Components & Amplifier Internal Block Diagram

AN-1808

Basic Connection

Figure 2 represents the simplest board configuration. The specific resistor values depicted here configure the device with a maximum gain of 9.9 V/V:



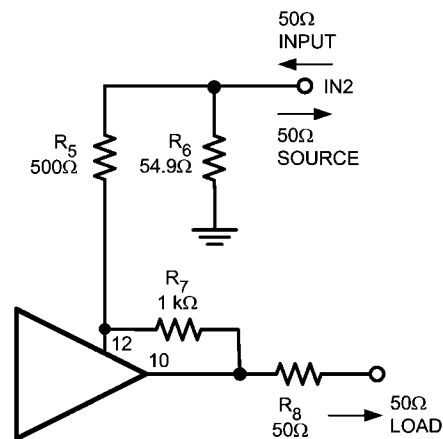
30055902

FIGURE 2. Basic Connection

The circuit of Figure 2 implements a non-inverting variable-gain amplifier with a 50Ω input impedance (R_1), a 50Ω output impedance (R_8), and a maximum gain of 9.9 V/V ($1.72 \times (R_7/R_3)$). Recognizing the combination of the 50Ω series output resistor and the 50Ω load results in a voltage divider, the gain to this match load is one half of the maximum device gain setting, i.e. 4.9 V/V (13.9 dB). The inverting input (In-) is ground-referenced through 50Ω while the output amplifier's non-inverting input is ground-referenced at pin 9 through R_{11} (not shown, replace R_{11} on board with a short).

Summing Signals and Offsets into the Output Stage

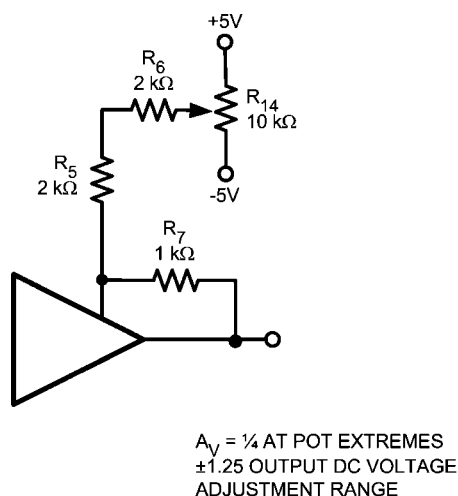
The output amplifier's inverting node (pin 12) is available to introduce any additional signals or offsets into the output. Since pin 12 is a virtual ground, additional signals may be summed into the node without a substantial impact on the signal current flowing from the adjustable-gain path. Briefly, adding an additional impedance on the output amplifier will result in a slight bandwidth reduction of the output amplifier and an increase in the noise gain for the output amplifier's non-inverting input noise voltage. Refer to application note OA-13 for a more thorough discussion of current feedback amplifiers in inverting summing applications. Figure 3 shows an example of using the optional components on the board to sum in a high-speed signal with a gain of -2 to the output pin (or -1 to the matched 50Ω load).



30055903

FIGURE 3. Summing a High-Speed Signal Into The Output

Note that R_6 can be used in either of two locations on this board. In Figure 3 R_6 is positioned as part of the output op amp's inverting input (In2) termination. Alternatively, it can be positioned to pick off the wiper voltage of an offset-adjust pot (R_{14} Figure 1) which is to be fed into the inverting node of the output amplifier. Figure 4 shows this application where an output offset, independent of the gain adjustment stage, is introduced into the inverting node of the output amplifier.



$A_V = 1/4$ AT POT EXTREMES
 ± 1.25 OUTPUT DC VOLTAGE
 ADJUSTMENT RANGE

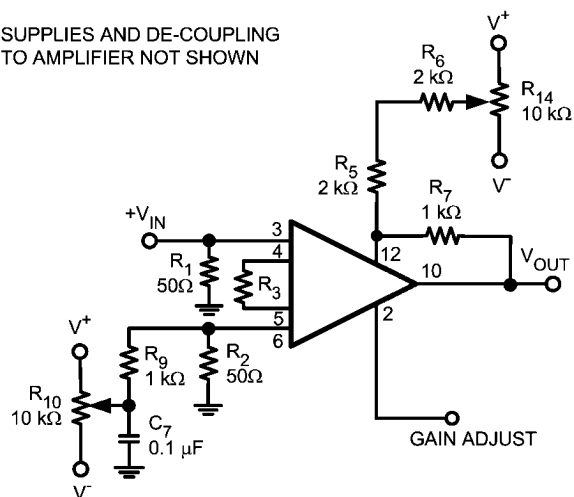
30055905

FIGURE 4. Summing in an Output DC Offset

Nulling the Output DC Offset

There are several factors contributing to the output offset voltage; the differential input buffer, the multiplier core and the output amplifier. The offsets produced by the input buffer and the output amplifier can be nulled with appropriate external circuitry. It will not be possible to completely null the offset effects of the multiplier core because of its non-linear nature. As a result, a small non-linear DC offset voltage gain over the adjustment range will always be present at the output of the device. Figure 5 shows the required external circuitry necessary to add the appropriate nulling offsets at both the input buffer and the output amplifier.

SUPPLIES AND DE-COUPLING
TO AMPLIFIER NOT SHOWN



30055904

FIGURE 5. Input and Output Stage DC Nulling

The output stage offset should be trimmed prior to the input stage. With the gain adjust pin set at minimum gain (maximum

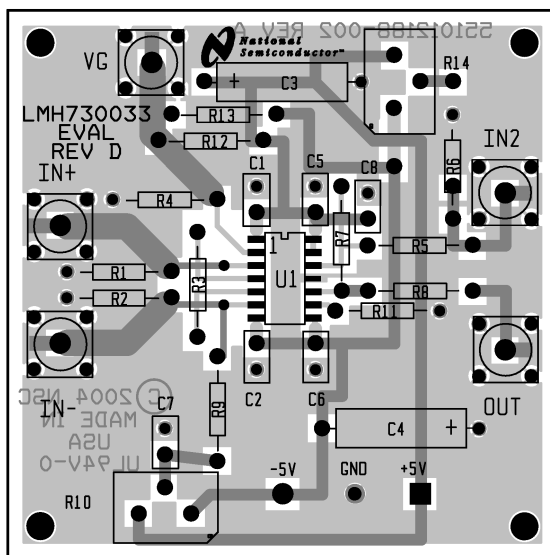
attenuation), the output stage offset may be nulled independently from the input stage. R_{14} should be adjusted to yield the desired output error voltage (typically <1 mV). Having corrected for the input offset voltage and bias current errors of the output amplifier, returning the gain adjust pin to the maximum gain voltage will allow the input buffer stage DC offset errors to be corrected. With no input signal present, but with matched source impedances at each of the two buffer inputs, R_{10} in Figure 5 can be adjusted to bring the output to within the desired error band.

Adjusting the input and the output stage offsets at the two gain extremes will hold the output DC error at a minimum at these two points in the gain range. If a more limited gain range is anticipated, the adjustments should be made at these operating points. The non-linear DC error introduced by the multiplier core will cause a residual, gain dependent, offset to appear at the output as the gain is swept from minimum to maximum. Also, neither the input nor the output offset adjustment described here will improve temperature drift effects.

Printed Circuit Board Layout

The LMH730033 was designed for evaluation of the LMH6502 and LMH6503.

Figure 6 shows both component and circuit side views.



30055906

FIGURE 6. LMH730033 (Component and Circuit Side)

Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH	www.national.com/webench
Audio	www.national.com/audio	Analog University	www.national.com/AU
Clock Conditioners	www.national.com/timing	App Notes	www.national.com/appnotes
Data Converters	www.national.com/adc	Distributors	www.national.com/contacts
Displays	www.national.com/displays	Green Compliance	www.national.com/quality/green
Ethernet	www.national.com/ethernet	Packaging	www.national.com/packaging
Interface	www.national.com/interface	Quality and Reliability	www.national.com/quality
LVDS	www.national.com/lvds	Reference Designs	www.national.com/refdesigns
Power Management	www.national.com/power	Feedback	www.national.com/feedback
Switching Regulators	www.national.com/switchers		
LDOs	www.national.com/ldo		
LED Lighting	www.national.com/led		
PowerWise	www.national.com/powerwise		
Serial Digital Interface (SDI)	www.national.com/sdi		
Temperature Sensors	www.national.com/tempsensors		
Wireless (PLL/VCO)	www.national.com/wireless		

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.

EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.

Copyright© 2008 National Semiconductor Corporation

For the most current product information visit us at www.national.com



**National Semiconductor
Americas Technical
Support Center**
Email:
new.feedback@nsc.com
Tel: 1-800-272-9959

**National Semiconductor Europe
Technical Support Center**
Email: europe.support@nsc.com
German Tel: +49 (0) 180 5010 771
English Tel: +44 (0) 870 850 4288

**National Semiconductor Asia
Pacific Technical Support Center**
Email: ap.support@nsc.com

**National Semiconductor Japan
Technical Support Center**
Email: jpn.feedback@nsc.com