The LM4935 Headset/Push-Button Detection Guide

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Overview

The LM4935 features an advanced headset detection scheme that can sense the insertion or removal of any type of available headset . The headset detect circuitry can differentiate between mono, stereo, mono with microphone, and stereo with microphone headsets, as shown in Figure 1. It can operate while the LM4935 is placed into low current standby mode, which promotes extended battery life. In standby mode, it consumes no extra current, if the headset has not been inserted into the headset jack.

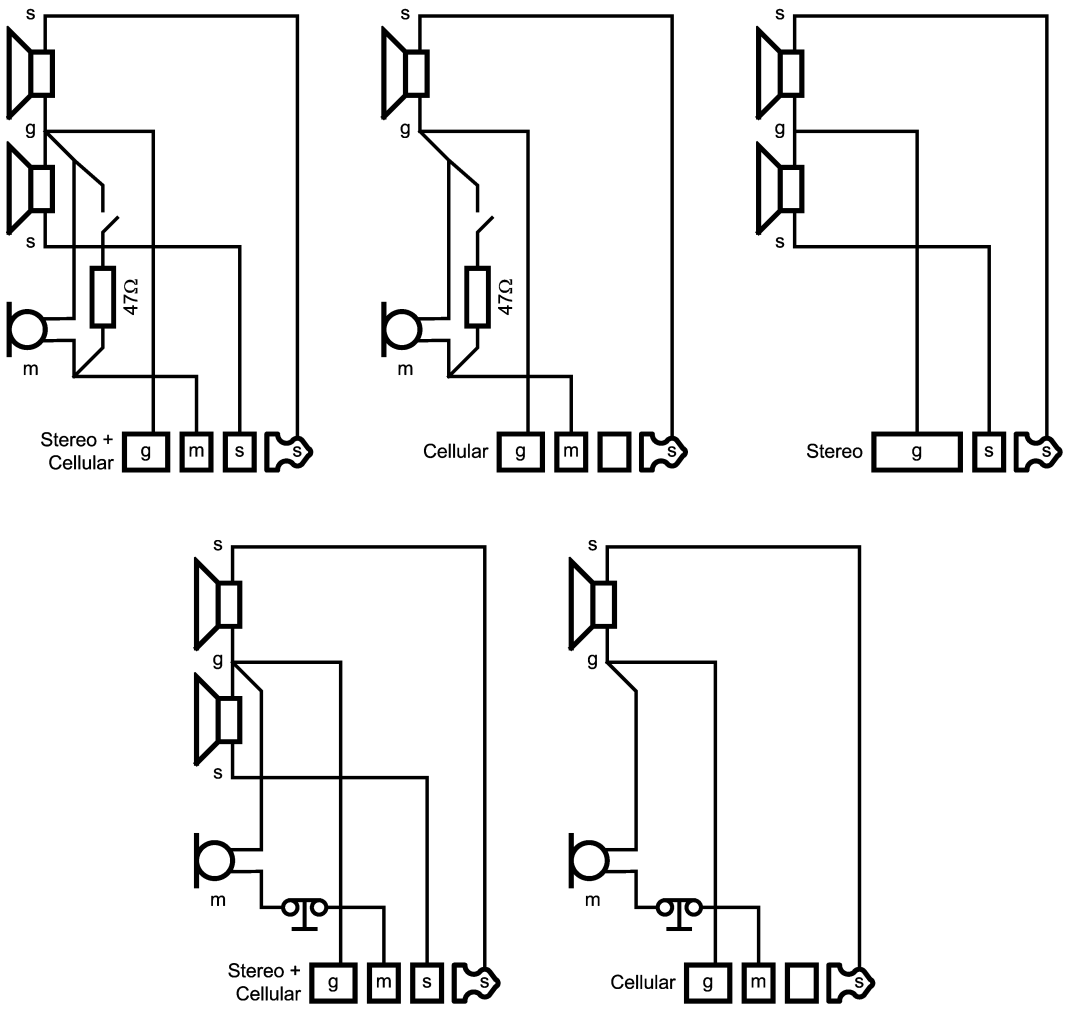

FIGURE 1. Headset Configurations Supported by the LM4935

OCL and AC-Coupled Modes

The headset detect circuitry also accommodates AC-coupled and output capacitor-less (OCL) headphone amplifier configurations. However, the connections between the headset jack and the LM4935 depends on the configuration of the headphone amplifier, as shown in Figure 2.

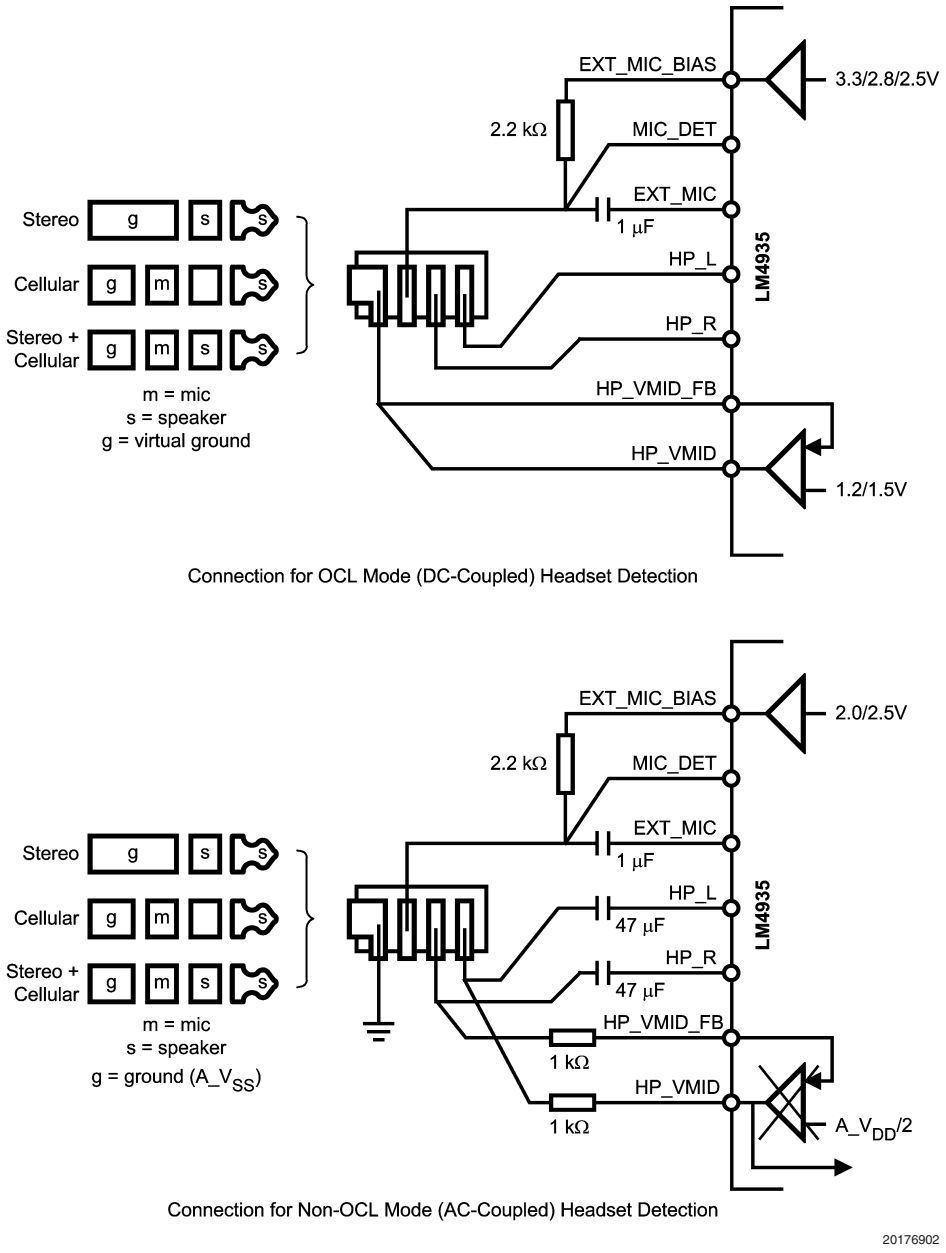

FIGURE 2. OCL and AC-coupled Headset Jack Connection Schemes

Headset Status Feedback

The headset detect circuitry takes advantage of the LM4935's read/write I^2C interface by updating bits 0 through 3 of the amplifier's STATUS register (0x18h) in real time.

TABLE 1. STATUS (0x18h)

Bits	Field	Description
0	HEADSET	This field is a logic high when headset presence is detected (only valid if the detection system is enabled).
1	STEREO_ HEADSET	This field is a logic high when a headset with stereo speakers is detected (only valid if the detection system is enabled).
2	MIC	This field is a logic high when a headset with a microphone is detected (only valid if the detection system is enabled).
3	BTN	This field is a logic high when the button on a headset is pressed (only valid if the detection system is enabled). The IRQ is cleared when the button has been released **and** a write command has been initiated on the status register.
4	SAR TRIG 1	If this field is a logic high, then an event has happened on SAR trigger 1 (write to this register to clear the IRQ).
5	SAR TRIG 2	If this field is a logic high, then an event has happened on SAR trigger 2 (write to this register to clear the IRQ).
6	TEMP	If this field is a logic high, then a temperature event has occurred (write to this register to clear the IRQ). This bit will stay high even when the IRQ is cleared, so long as the event occurs. This bit is only valid whenever the loudspeaker amplifier is turned off.
7	GPIN	When GPIO_SEL is set to a readable configuration, a digital input on GPIO1 can be read back here.

Setting the LM4935's DETECT register (0x17h) bit 0 to a logic high causes the amplifier to issue an interrupt (set the IRQ pin high) when a headset insert/removal event has occurred. An I^2C read transaction is triggered by an interrupt request, when the contents of the STATUS register (0x18h) are read back by the baseband IC (or microprocessor). This allows the baseband IC to perform the appropriate function dictated by the change in the mobile phone's headset status.

TABLE 2. DETECT (0x17h)

Bits	Field	Description
0	DET_INT	If set, an IRQ is issued when a change is detected in the headset status. Clearing this bit will clear an IRQ that has been triggered by the headset detect.
1	BTN_INT	If set, an IRQ is issued when the headset button is pressed. Clearing this bit will clear an IRQ that has been triggered by a button event.
2	TEMP_INT	If set, an IRQ is issued during a temperature event. If cleared, the LM4935 will still automatically cycle the power amplifiers off when the internal temperature is too high. This bit should not be set whenever the loudspeaker amplifier is turned on. Clearing this bit will clear an IRQ that has been triggered by a temperature event.

Headset Status Feedback (Continued)

TABLE 2. DETECT (0x17h) (Continued)

Bits	Field	Description	
6:3	HS_ DBNC_TIME	Sets the time used for debouncing the analog signals from the detection inputs used to sense the insertion/removal of a headset.	
		HS_DBNC_TIME	Time (ms)
		0000_2	0
		0001_2	8
		0010_2	16
		0011_2	32
		0100_2	48
		0101_2	64
		0110_2	96
		0111_2	128
		1000_2	192
		1001_2	256
		1010_2	384
		1011_2	512
		1100_2	768
		1101_2	1024
		1110_2	1536
		1111_2	2048

Reduced Power Consumption

To reduce power consumption and processor loading, the headset detect circuitry automatically disables audio amplifiers that are not in use. The left and right headphone amplifiers will be disabled when the LM4935 is set to active mode, the headset detect is enabled, and a headset is not present. In the AC-coupled configuration, the headphone amplifiers will be muted. In the OCL configuration, the headphone amplifiers will be switched off. The external microphone bias pin (EXT_BIAS) is disabled for both AC-coupled and OCL configurations. However, the automatic changes made by the headset detect circuitry while the LM4935 is running in active mode will take precedence over I^2C control register settings.

Push-Button Press / Release Detect

The LM4935 has the capability to detect button press if a button is present on the headset microphone. Both parallel push-button (push-button in parallel with the headset microphone) and series push-button (push-button in series with the headset microphone) headsets can be detected. However, the button type (series or parallel) needs to be predefined by BUTTON_TYPE (bit 3 of the MIC_2 (0x0Ch) register). Button presses can be detected even when the part is in standby mode; this consumes 10µA of analog supply current for a series push-button and 100µA for a parallel push-button. Upon push-button press or release, the headset detect circuitry updates bit 3 of the STATUS (0x18h) register. If a parallel push-button headset is inserted into the headset jack in active OCL mode with the internal microphone selected (INT_EXT = 0; bit 6 of reg (0x0Bh)) , the INT_EXT bit must be set to a logic high before BTN (bit 3 of STATUS (0x18h)) can be read. When a button press is sensed, the LM4935 can also be programmed to raise an interrupt on the IRQ pin by setting bit 1 of DETECT(0x17h).

TABLE 3. MIC_2 (0x0Ch)

Bits	Field	Description		
0	OCL_ VCM_ VOLTAGE	Selects the voltage used as virtual ground (HP_VMID pin) in OCL mode. This will depend on the available supply and the power output requirements of the headphone amplifiers.		
		OCL_VCM_VOLTAGE	Voltage	
		0	1.2V	
		1	1.5V	
2:1	MIC_ BIAS_ VOLTAGE	Selects the voltage as a reference to the internal and external microphones. Only one bias pin is driven at once depending on the INT_EXT bit setting found in the MIC_1 (0x0Bh) register. MIC_BIAS_VOLTAGE should be set to '11' only if A_V_{DD} > 3.4V. In OCL mode, MIC_BIAS_VOLTAGE = '00' (EXT_BIAS = 2.0V) should not be used to generate the EXT_BIAS supply for a cellular headset external microphone.		
		MIC_BIAS_VOLTAGE	EXT_BIAS	INT_BIAS
		00_2	2.0V	2.0V
		01_2	2.5V	2.5V
		10_2	2.8V	2.8V
		11_2	3.3V	3.3V
3	BUTTON_TYPE	If set, the LM4935 assumes that the button (if used) in the headset is in series (series push button) with the microphone, opening the circuit when pressed. The default is for the button to be in parallel (parallel push button), shorting out the microphone when pressed.		
5:4	BUTTON_ DEBOUNCE_ TIME	Sets the time used for debouncing the pushing of the button on a headset with a parallel push button.		
		BUTTON_DEBOUNCE_TIME	Time (ms)	
		00_2	0	
		01_2	8	
		10_2	16	
		11_2	32	

Headset / Push-Button Debouncing

The LM4935 provides debounce programmability for both headset insertion/removal and push-button press detect. Headset debounce programmability is used to avoid false detection by ignoring glitches generated by the physical act of inserting or removing a headset from a headset jack. This debounce time is defined by HS_DBNC_TIME (bits 6:3 of DETECT(0x17h)) and can be set for up to 2048ms. Parallel push-button debounce programmability is used to avoid false detection by ignoring glitches due to mechanical switch bouncing during a parallel push-button press or release. Parallel push-button debounce time is defined by BTN_DBNC_TIME (bits 5:4 of MIC_2(0x0Ch)) and can be set for up to 32ms. Because the initial effect of a series push-button press (microphone disconnected) is indistinguishable from a headset removal, the debounce time for a series push-button is defined by the headset debounce time, HS_DBNC_TIME.

Enabling the Headset / Push-Button Detect Circuit

For reliable headset and push-button detection, it is recommended to program the settings of the headset detect circuitry first before activating the headset detect circuitry. The following bits should be defined in this order:

1. OCL (bit 7 of BASIC(0x00h)) which programs the LM4935's headphone amplifier to be either AC-coupled or OCL.
2. HS_DBNC_TIME (bits 6:3 of DETECT(0x17h)) which sets the headset insertion/removal and series push-button (if used) debounce time.
3. BUTTON_TYPE (bit 3 of MIC_2(0x0Ch)) which predefines whether a series or parallel type push-button on the headset is going to be used.
4. BTN_DBNC_TIME (bits 5:4 of MIC_2(0x0Ch)) which sets the parallel push-button (if used) debounce time.

Once these bits have been defined, the headset and push-button detection circuitry can be enabled by setting CHIP_MODE (bit 0 of BASIC(0x00h)).

TABLE 4. BASIC (0x00h)

Bits	Field	Description			
1:0	CHIP_MODE	The LM4935 can be placed in one of four modes which dictate its basic operation. When a new mode is selected, the LM4935 will change operation silently and re-configure the power management profile automatically. The modes are described as follows:			
		CHIP MODE	Audio System	Detection System	Typical Application
		00_2	Off	Off	Power-down Mode
		01_2	Off	On	Stand-by mode with headset event detection
		10_2	On	Off	Active without headset event detection
		11_2	On	On	Active with headset event detection
7	OCL	If set, the part is placed in OCL (Output Capacitor Less) mode.			

Push-To-Talk (PTT) Handset Push-Button Detect Capability

The LM4935 can be seamlessly integrated into systems utilizing a PTT (push-to-talk) push-button located on the handset itself . A PTT push-button press can be detected using the LM4935's multipurpose successive approximation register (SAR) ADC. A logic signal set by the position of the PTT push-button can be applied to either the VSAR1 or VSAR2 input pins of the LM4935. The LM4935 can issue an interrupt when this signal passes a preprogrammed logic signal threshold voltage. The logic signal applied to either VSAR1 or VSAR2 is then continuously sensed by the SAR ADC. If there is a change in logic level at either pin, an IRQ is issued. SAR_TRIG_1 (bit 4 of STATUS(0x18h)) becomes a logic high whenever a SAR trigger event is detected on the VSAR1 input pin. SAR_TRIG_2 (bit 5 of STATUS(0x18h)) becomes a logic high whenever a SAR trigger event is detected on the VSAR2 input pin. Once an IRQ is issued, the STATUS register (0x18h) can be read to determine the cause of the interrupt request. For a more detailed discussion on the operation and programmability of the SAR ADC please refer to the LM4935 datasheet.

A PTT push-button press can also be detected using the LM4935's GPIO interface. A logic level set by the position of the PTT push-button is applied to the LM4935's GPIO1 pin. The voltage that is applied to the GPIO1 pin can be read via GPIN (bit 7 of STATUS(0x18h)). GPIN directly monitors the status of the PTT push-button. This method does not automatically raise an interrupt request upon a PTT push-button press. Therefore, a periodic read of the STATUS(0x18h) register is required when using the GPIO1 pin for PTT push-button detect.

Revision Table

Rev	Date	Description
0.1	04/24/06	Initial release.

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