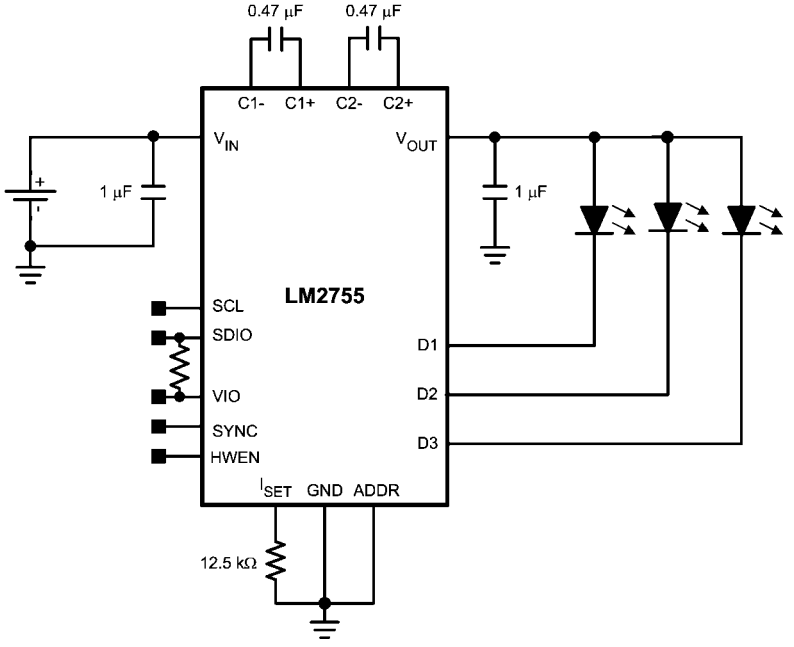
LM2755 Charge Pump LED Controller with I2C Compatible Interface in µSMD

National Semiconductor
Application Note 1778
April 30, 2008

Typical Application



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Basic Description

The LM2755 is a charge-pump-based, constant current LED driver capable of driving 3 LEDs with a total output current up to 90mA. The diode current waveforms of each LED can be trapezoidal with timing and level parameters (rise time, fall time, high level, low level, delay, high time, low time) programmed via an I²C compatible interface. The 32 brightness levels found on the LM2755 are exponentially spaced (as opposed to linearly spaced) to better match the response of the human eye to changing brightness levels.

Bill of Materials

Component Symbol	Value	Package	Manufacturer	Part #
LM2755	--	TMD18AAA µSMD18	National	LM2755TMX
LM2755 Evaluation Board	--	--	National	551012853-001 RevA
DA	Blue LED	--	OSRAM	LB M673-L1M2-35-Z
DB	Green LED	--	OSRAM	LG M676-N2Q1-24-Z
DC	Amber LED	--	OSRAM	LA M676-Q2S1-1-Z
DRGB	RGB LED	--	TT Electronics / OptekTech	OVSTRGBAC6
C_{IN}	1.0uF 10V X5R	0603	TDK	C1005X5R1A105M
C_{OUT}	1.0uF 10V X5R	0603	TDK	C1005X5R1A105M
C_1,C_2	0.47uF 10V X5R	0603	TDK	C1005X5R1A474M
R_{SET}	12.4K OHM 1/10W 1%	0603	Vishay Dale	CRCW060312K4FKEA

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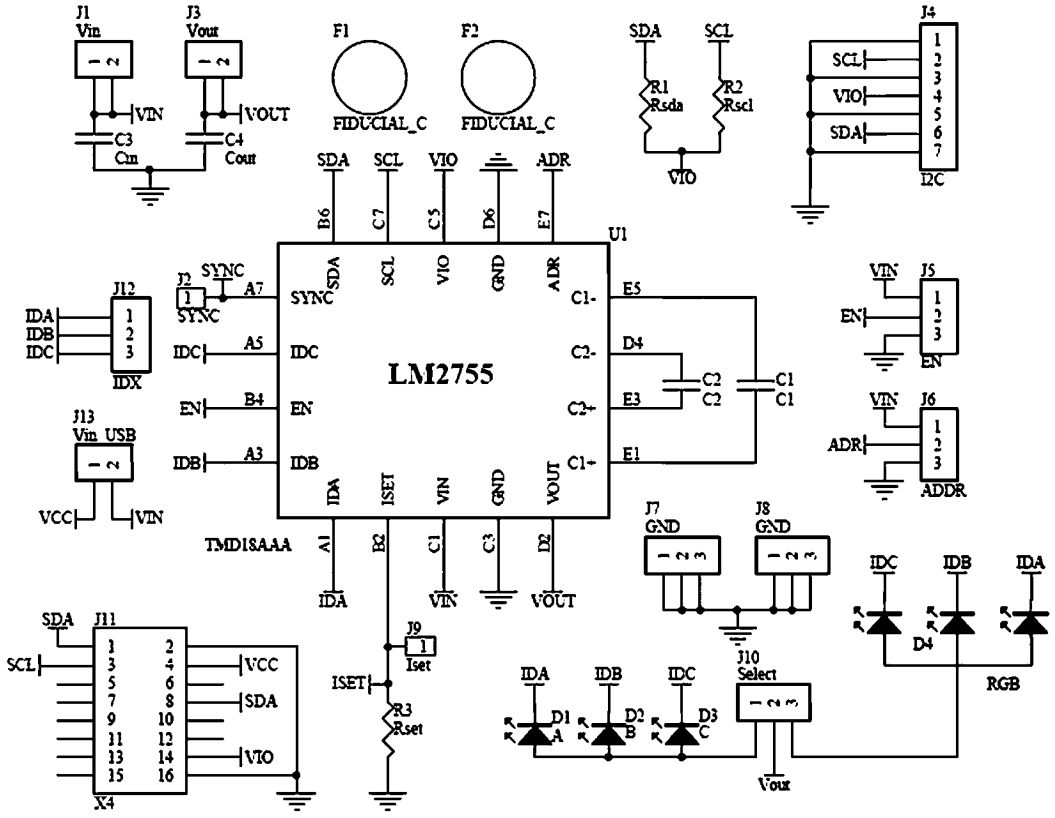
LM2755 Evaluation Board Schematic



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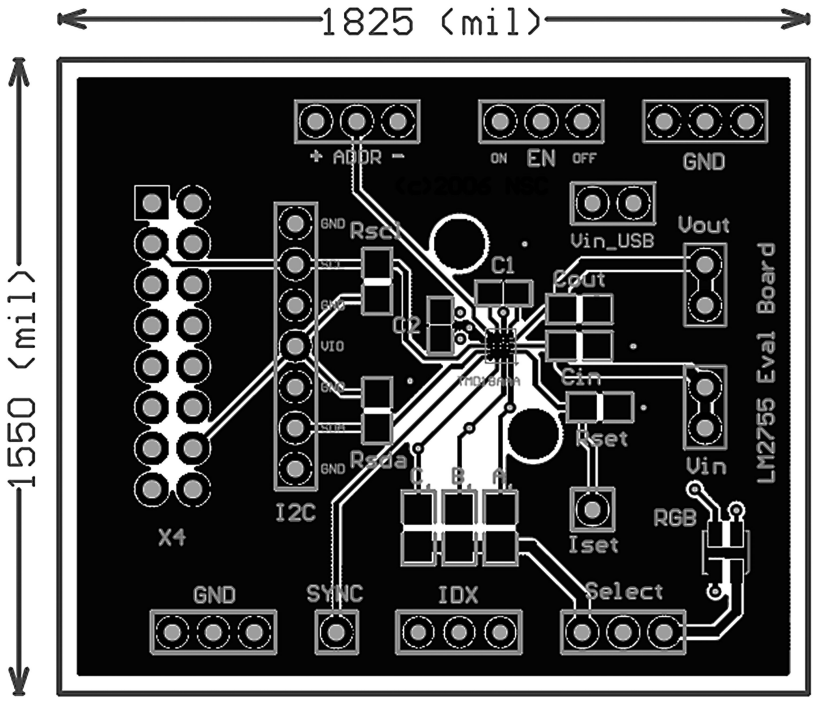
LM2755 Evaluation Board Layout



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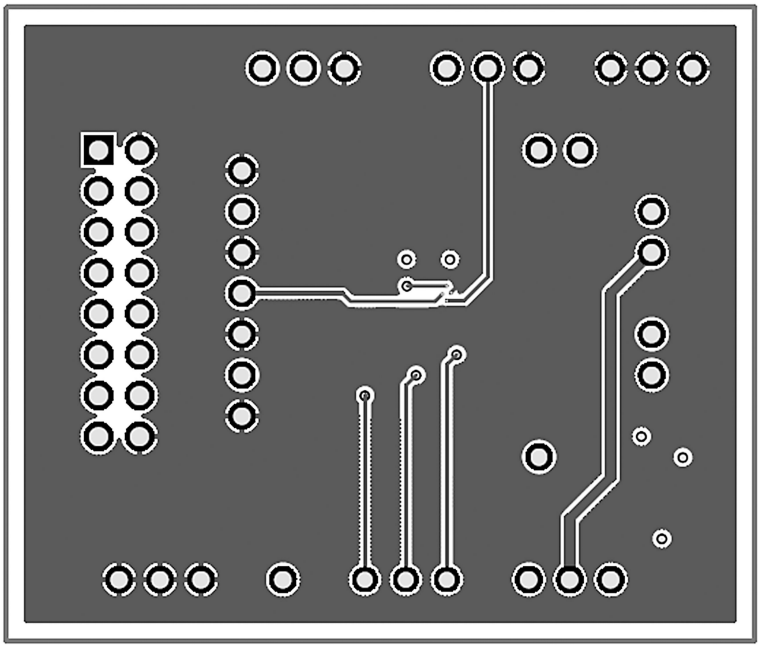
Top Layer



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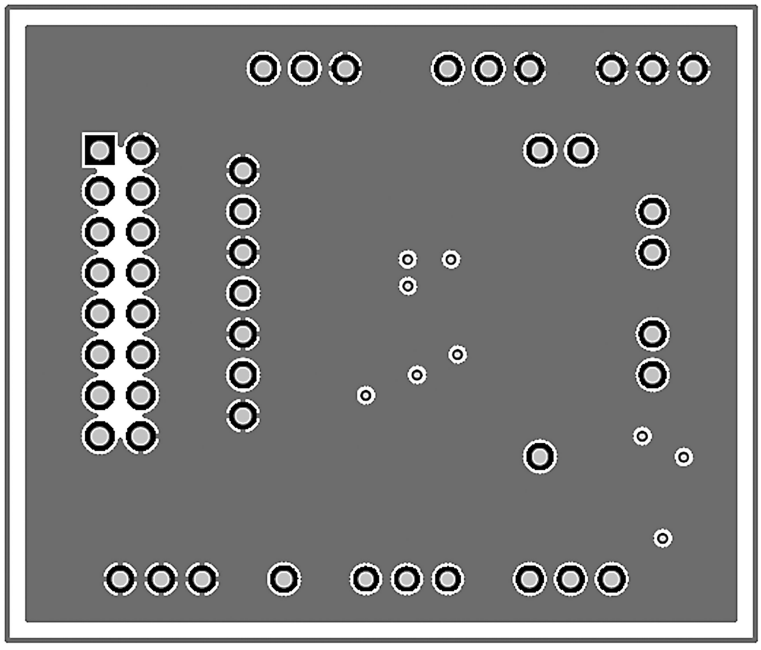
Middle Layer 1



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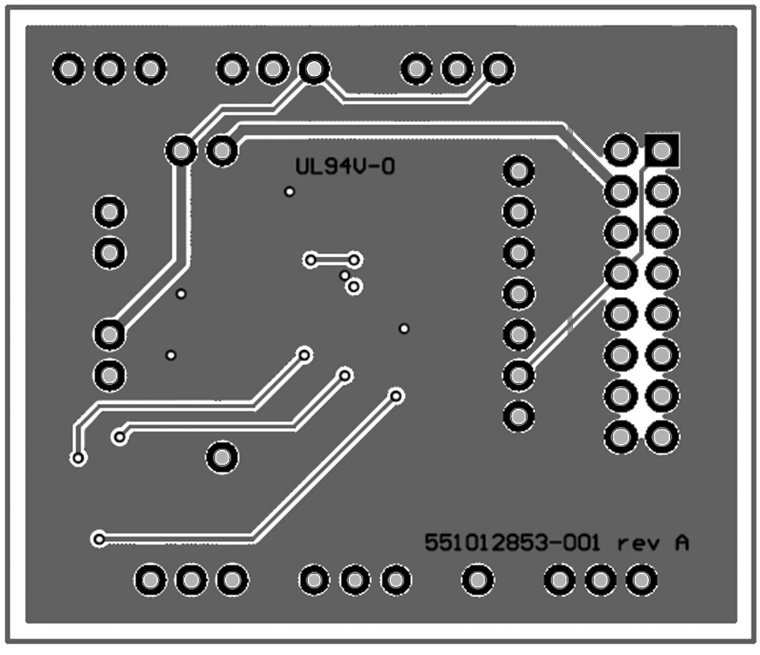
Middle Layer 2



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Bottom Layer (mirrored)

Board Operation

BASIC CONNECTIONS

To operate the LM2755 Charge Pump LED Controller with I2C Compatible Interface in µSMD, connect a supply voltage (2.7V-5.5V) between board connectors VIN and GND and attach an I²C interface using one of the methods described in the *EXTERNAL CONTROL INTERFACE SECTION* of this document.

Default Jumper Connections:

- EN: Connects the "+" post to the middle post of the header strip. This connects VIN to the EN pin of the LM2755, enabling the part.
- ADDR: Connects the "-" post to the middle post of the header strip. This selects the I2C chip id to a 0x18 while the "+" sets the I2C chip ID to a 0x67.
- SELECT: This connects POUT to the anodes of the LEDs. Connecting the center post to the LEFT pin connects the individual Red, Green, and Blue LEDs while the RIGHT pin connects the combination RGB LED
- Vin_USB: Connects the adjustable voltage supply of the USB Docking board to the VIN of the LM2755. If the USB board is not used, this jumper does not need to be placed. If the USB Docking board is going to be used for the I2C interface, but not for VIN, make sure the Vin_EXT jumper is removed.

With the default jumper connections made, the board will be ready to operate once an input voltage and an I2C interface generator (external or USB docking board) are connected.

HWEN Pin

The LM2755 has a hardware enable/reset pin (HWEN) that allows the device to be disabled by an external controller without requiring an I²C write command. Under normal operation, the HWEN pin should be held high (logic '1') to prevent an unwanted reset. When the HWEN is driven low (logic '0'), all internal control registers reset to the default states and the part becomes disabled. Please see the *Electrical Characteristics* section of the datasheet for required voltage thresholds.

SYNC Pin

The SYNC pin allows the LM2755 to use an external clock to generate the timing within. This allows the LM2755's current-sinks to pulse-width modulate (PWM) and transition at a user controlled frequency. The PWM frequency and the step-time increment can be set by feeding a clock signal into the sync pin and enabling bit '6' in the general purpose register (See the I2C Compatible Interface section for more details.). The maximum frequency allowed to ensure current level accuracy is 1MHz. This external clock is divided down by 32x to create the minimum time-step and PWM frequency. For a 1MHz external clock, the PWM frequency becomes 31.25KHz and the minimum step time becomes 32 µseconds. If not used, it is recommended that the SYNC pin be tied to ground.

ADDR Pin

The ADDR pin allows the user to chose between two different I2C chip addresses for the LM2755. Tying the ADDR pin high sets the chip address to hex 67 (0x67 or 67h), while tying the ADDR pin low sets the chip address to hex 18(0x18 or 18h). This feature allows multiple LM2755's to be used within a system in addition to providing flexibility in the event another chip in the system has a chip address similar to the default LM2755 address (0x18).

EXTERNAL CONTROL INTERFACE CONNECTION

The LM2755 Evaluation Board provides two ways to connect an I²C compatible interface to the LM2755 IC. The first method to connect the interface is through a set of connectors on the bottom of the evaluation board that allow the board to plug into National's USB interface board directly. The second method of interface connection is through a header strip located on the left hand side of the evaluation board. There are pins available to connect VIO (contoller reference voltage), SCL (Interface Clock Line), and SDIO (Interface Data Line) each separated by a ground pin. The evaluation board has two external pull-ups that connect both SCL and SDIO to VIO to compliment the open drain inputs found on the LM2755. The *OPERATION DESCRIPTION* section of this application note describes the internal registers and I²C compatible interface in greater detail.

OPERATION DESCRIPTION

Application Information

SETTING FULL-SCALE LED CURRENT

The current through the LEDs connected to D1, D2 and D3 can be set to a desired level simply by connecting an appropriately sized resistor (R_{SET}) between the I_{SET} pin of the LM2755 and GND. The LED currents are proportional to the current that flows through the I_{SET} pin and are a factor of 200 times greater than the I_{SET} currents. The feedback loop of the internal amplifier sets the voltage of the I_{SET} pin to 1.25V (typ.). The statement above is simplified in the equation below:

$$I_{Dx\ (Full\text{-}Scale)} = 200 \times (V_{ISET} / R_{SET})$$

Please refer to the I²C Compatible Interface section of this datasheet for detailed instructions on how to adjust the brightness control registers.

BRIGHTNESS LEVEL CONTROL

Once the desired R_{SET} value has been chosen, the LM2755 has the ability to internally dim the LEDs by modulating the currents with an internally set 20kHz PWM signal. The PWM duty cycle percentage is independently set for each LED through the I²C compatible interface. The 32 brightness levels follow a exponentially increasing pattern rather than a linearly increasing one in order to better match the human eyes response to changing brightness. The brightness level response is modeled in the following equations.:

$$I_{Dx\ LOW} = (0.9)^{(31-n_{LOW})} \times I_{Dx\ Fullscale}$$

$$I_{Dx\ HIGH} = (0.9)^{(31-n_{HIGH})} \times I_{Dx\ Fullscale}$$

n_{HIGH} and n_{LOW} are numbers between 0 and 31 stored in the brightness level registers. When the waveform enable bits are set to '1', n_{HIGH} and n_{LOW} are the brightness level boundries. These equations apply to all Dx outputs and their corresponding registers. A '0' code in the brightness control register sets the current to an "off-state" (0mA).

TIME STEP CONTROL

Bit 0-Bit 2: The value of the 3 bits is equal to N, which is used in the timing control equations. $0 \leq N \leq 7$. The minimum internal time step (N=0) is 50µs. Setting the time-step to N=7 results in a minimum time step of 400µsec. Time step = 50µsec × (N+1)

Bit 3-Bit 7: Not used

DELAY CONTROL

The LM2755 allows the programmed current waveform on each diode pin to independantly start with a delay upon en-

abling the waveform dimming bits in the general purpose register. There are 256 delay levels available. The delay time is set by the following equation:

$$t_{delay} = N \times n_{delay}$$

n_{delay} is stored in the Dx delay registers and N is stored in the Time Step Control register.

By default, n_{delay} =0 with a range of $0 \leq n_{delay} \leq 255$.

TIMING CONTROL

$T_{PWM\ INTERNAL}$ =50µs, N is a value stored in the Time Step register, and n_{Trise} n_{Tfall}, n_{Thigh}, n_{Tlow} are numbers between 0 and 255, stored in the timing control registers. The durations of the rise, high, fall and low times are given by:

$$t_{rise/fall\ Total} = t_{PWM\ INTERNAL} \times 2^N \times (n_{high}\text{-}n_{low}) \times n_{Trise/fall}$$

where $0 \leq n_{Trise/fall} \leq 255$

$$t_{rise\ or\ fall\ Total} = 50\mu s \times (n_{high}\text{-}n_{low}) \text{ when } n_{Trise/fall} = 0$$

$$t_{high\ or\ low} = t_{PWM\ INTERNAL} \times 2^N \times (n_{high/low} + 1)$$

where $0 \leq n_{Thigh/low} \leq 255$

SYNC PIN TIMING CONTROL

It is possible to replace the internal clock with an external one placed on the external SYNC pin. Writing a '1' to bit6 in the general purpose register switches the system clock from being internally generated to externally generated. The period of the PWM modulating signal becomes:

$$t_{PWM} = t_{SYNC} / 32$$

The maximum recommended SYNC frequency is 1MHz. This frequency yields a PWM frequency of 31.25KHz and the minimum step time of 32 µsec.

I²C Compatible Interface

DATA VALIDITY

The data on SDIO line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

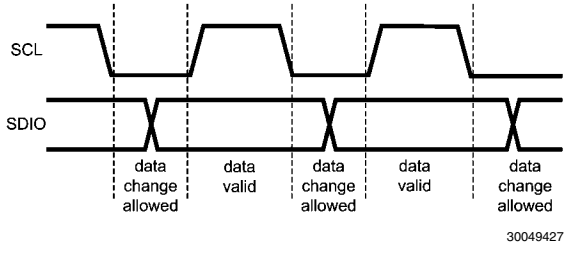


FIGURE 1. Data Validity Diagram

A pull-up resistor between VIO and SDIO must be greater than [**(VIO-V_{OL}) / 3mA**] to meet the V_{OL} requirement on SDIO. Using a larger pull-up resistor results in lower switching current with slower edges, while using a smaller pull-up results in higher switching currents with faster edges.

START AND STOP CONDITIONS

START and STOP conditions classify the beginning and the end of the I²C session. A START condition is defined as SDIO signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDIO transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP conditions. The I²C bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise. The data on SDIO line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when CLK is LOW.

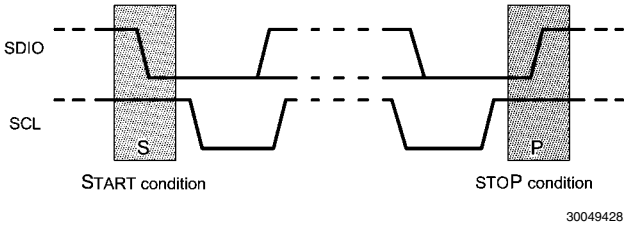


FIGURE 2. Start and Stop Conditions

TRANSFERING DATA

Every byte put on the SDIO line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDIO line (HIGH) during the acknowledge clock pulse. The LM2755 pulls down the SDIO line during the 9th clock pulse, signifying an acknowledge. The LM2755 generates an acknowledge after each byte has been received.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM2755 address is 18h is ADR is tied low and 67h if ADR is tied high . For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

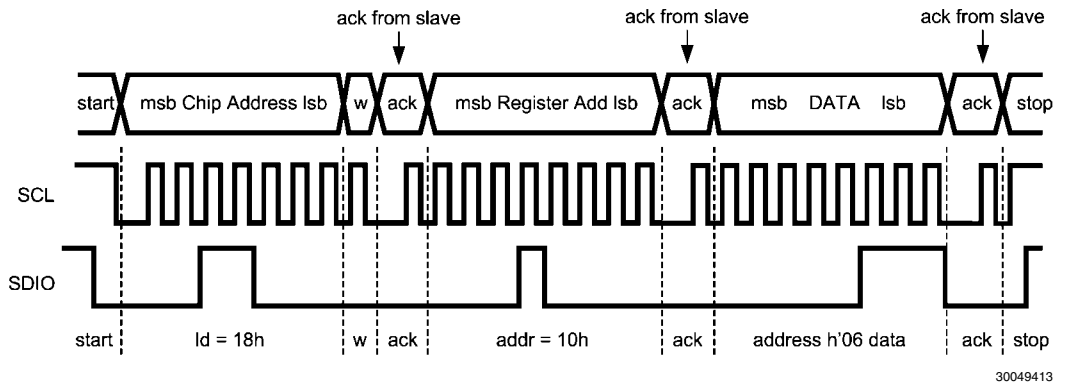


FIGURE 3. Write Cycle
w = write (SDIO = "0")
r = read (SDIO = "1")
ack = acknowledge (SDIO pulled down by either master or slave)
rs = repeated start
id = chip address, 18h if ADR = '0' or 67h if ADR = '1' for LM2755

I²C COMPATIBLE CHIP ADDRESS

The chip address for LM2755 is 0011000 (0x18) when ADDR = '0' or 1100111(0x67) when ADR = '1'.

Dimming Waveform

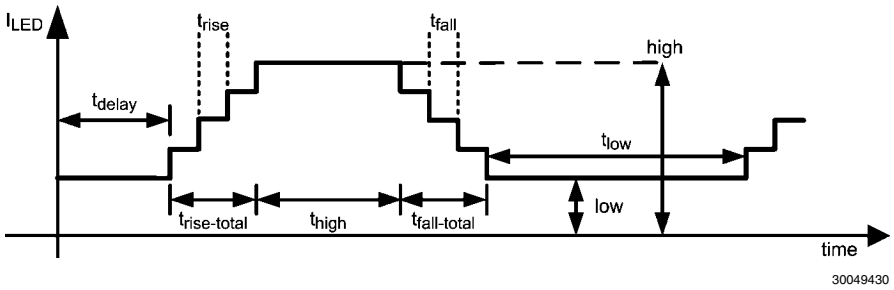


FIGURE 4.

INTERNAL REGISTERS OF LM2755

Register Name	Internal Hex Address	Power On Value
General Purpose	x10	0000 0000
Time Step	x20	1000 1000
D1 High Level	xA9	1110 0000
D1 Low Level	xA8	1110 0000
D1 Delay: t_{delay}	xA1	0000 0000
D1 Ramp-Up Step Time: t_{rise}	xA5	0000 0000
D1 Time High: t_{high}	xA3	0000 0000
D1 Ramp-Down Step Time: t_{fall}	xA4	0000 0000
D1 Timing: t_{low}	xA2	0000 0000
D2 High Level	xB9	1110 0000
D2 Low Level	xB8	1110 0000
D2 Delay: tdelay	xB1	0000 0000
D2 Ramp-Up Step Time: t_{rise}	xB5	0000 0000
D2 Time High: t_{high}	xB3	0000 0000
D2 Ramp-Down Step Time: t_{fall}	xB4	0000 0000
D2 Timing: t_{low}	xB2	0000 0000
D3 High Level	xC9	1110 0000
D3 Low Level	xC8	1110 0000
D3 Delay: tdelay	xC1	0000 0000
D3 Ramp-Up Step Time: t_{rise}	xC5	0000 0000
D3 Time High: t_{high}	xC3	0000 0000
D3 Ramp-Down Step Time: t_{fall}	xC4	0000 0000
D3 Timing: t_{low}	xC2	0000 0000

General Purpose Register Description

- Bit 0: enable output D1 with high current level.
- Bit 1: enable output D2 with high current level.
- Bit 2: enable output D3 with high current level.
- Bit 3: enable dimming waveform on output D1.
- Bit 4: enable dimming waveform on output D2.
- Bit 5: enable dimming waveform on output D3.
- Bit 6: enable external clock. '1' = External Clock Sync, '0' = Internal Clock Used
- Bit 7: If Bit 7 = 0 the charge pump is powered on before any dimming waveform is enabled. If Bit7 = 1 the dimming waveform can be enabled before charge pump is powered on.

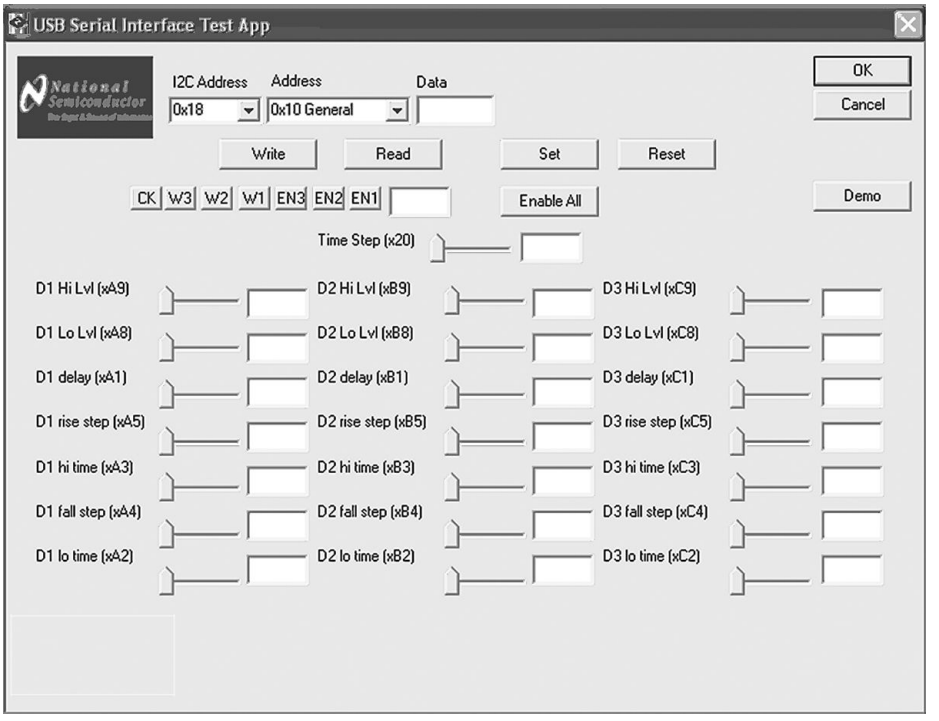
Software Interface Information

In order to fully evaluate the LM2755 part, an "I²C Compatible" interface must be used for any functionality to occur. A detailed description of the interface control is described in the LM2755 datasheet.

National has created an I²C compatible interface generation program and USB docking board that can help exercise the part in a simple way. Contained in this document is a description of how to use the USB docking board and interface software.

The LM2755 evaluation board has the means to "plug into" the USB docking board. The USB docking board can provide all of the control signals and power required to operate the evaluation board. A standard USB cable must be connected to the board from a PC.

The I²C compatible interface program provides all of the control that the LM2755 part requires. For proper operation, the USB docking board should be plugged into the PC before the interface program is opened. Once connected, and the program is executed, a basic interface window will open.



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GUI Start-Up

At the top of the interface, the user can read or write to any of the data registers on the LM2755 part using the two pull down menus (for the slave i.d. and the desired data address), the data field, and the read and write buttons.

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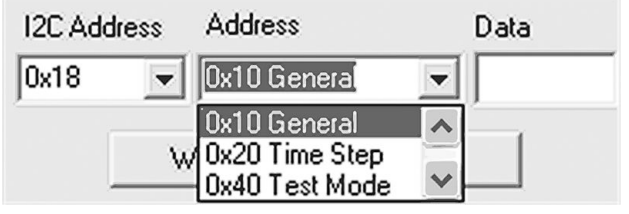
Generic Read/Write Field



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Drop Down Menu

Just below the pull down menus are convenient toggle buttons to set/reset the control bits in the General Purpose Register.

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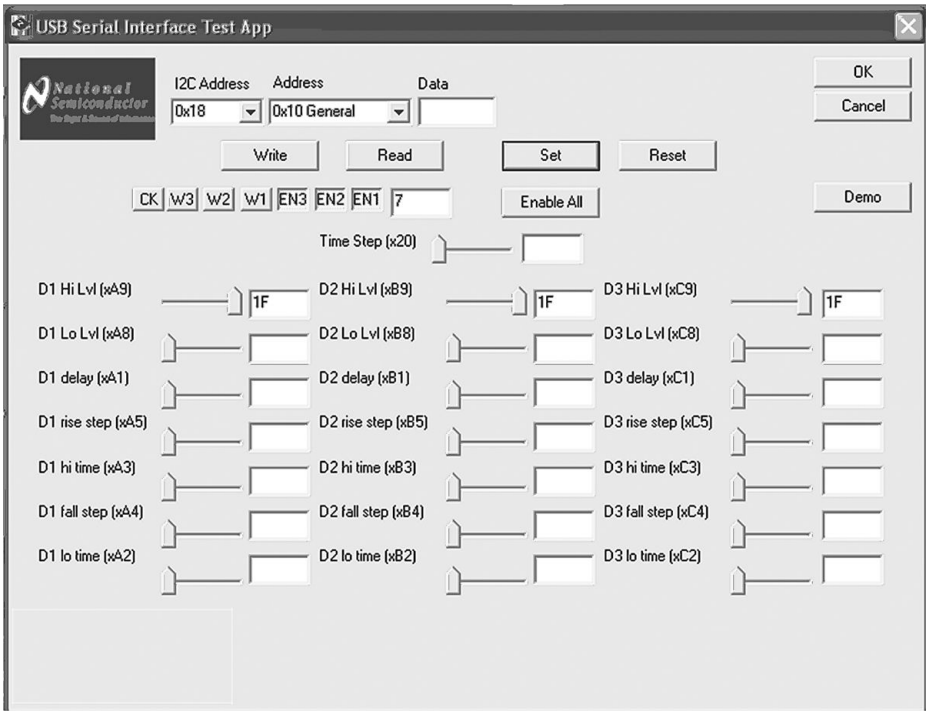
Control and Configuration Buttons

- CK: When depressed, the external clock is used to set the timing for all of the waveform control.
- W3-W1: When depressed, the waveforms profile for the drivers are enabled
- EN3-EN1: These bits, when depressed, enable BankA, BankB and BankC.



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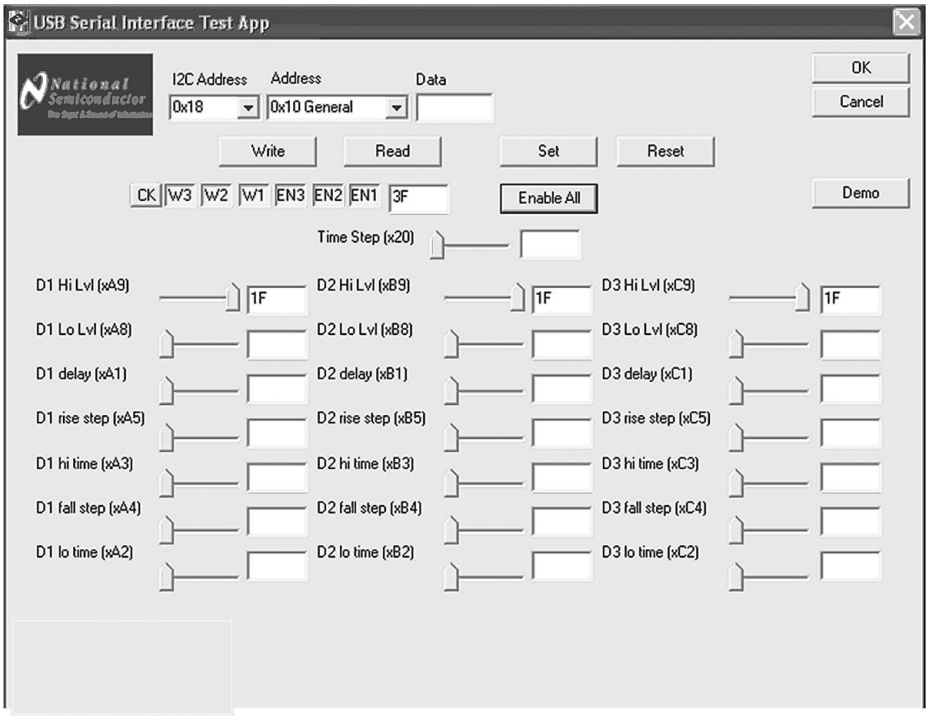
Results of Pressing the Set Button

Pressing the Set button enables D1, D2 and D3 on the LM2755 and sets the brightness levels in each bank to full-scale.



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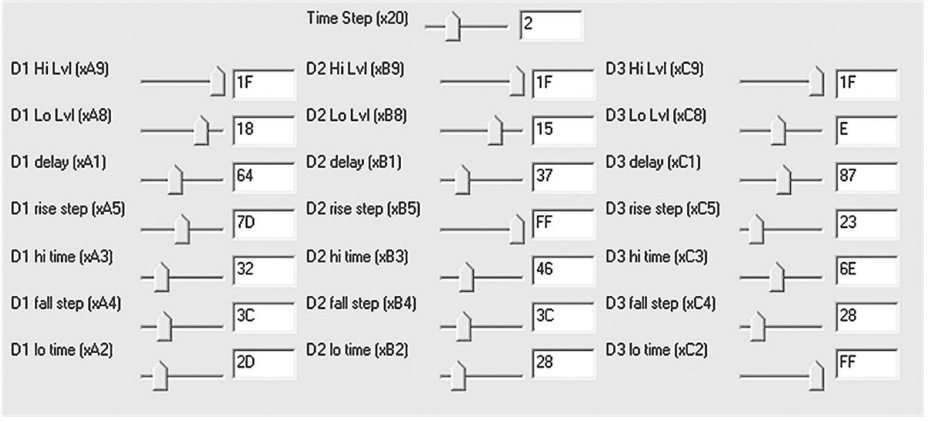
Enable ALL

- Pressing the Enable ALL button enables D1, D2 and D3 on the LM2755 and sets the brightness levels in each bank to full-scale. The waveforms stored in the other registers are also enabled on each of the Dx Drivers



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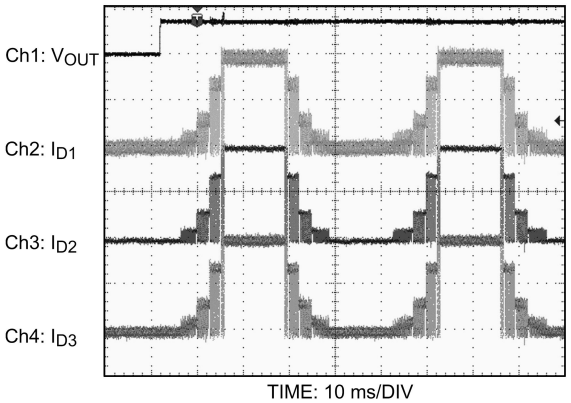
Control Sliders

- Time Step: Sets the base time unit for all timing control
- D1 Sliders: Sets the waveform profile for D1
- D2 Sliders: Sets the waveform profile for D2
- D3 Sliders: Sets the waveform profile for D3

Example Diode Current Waveforms



TIME: 10 ms/DIV
Ch1: 5V/Div Ch2: 10 mA/Div
Ch3: 10 mA/Div Ch4: 10 mA/Div

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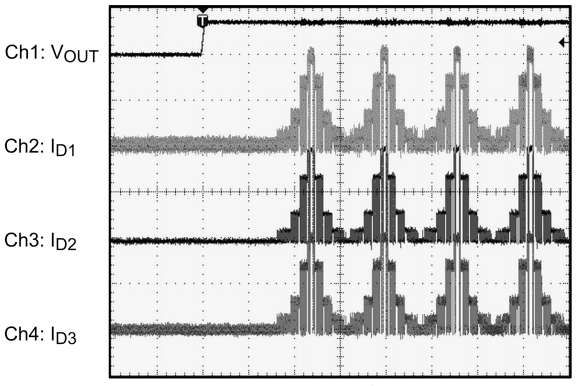

TIME: 2 ms/DIV
Ch1: 5V/Div Ch2: 10 mA/Div
Ch3: 10 mA/Div Ch4: 10 mA/Div

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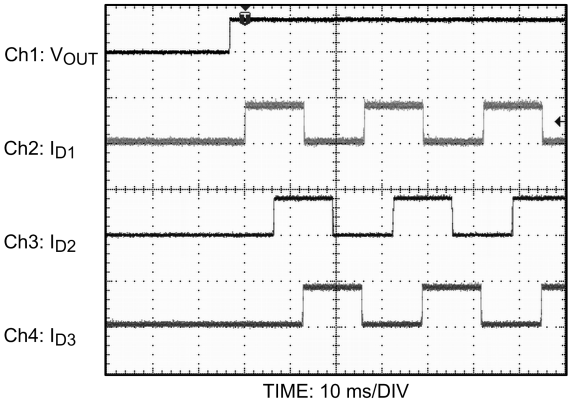

TIME: 10 ms/DIV
Ch1: 5V/Div Ch2: 10 mA/Div
Ch3: 10 mA/Div Ch4: 10 mA/Div

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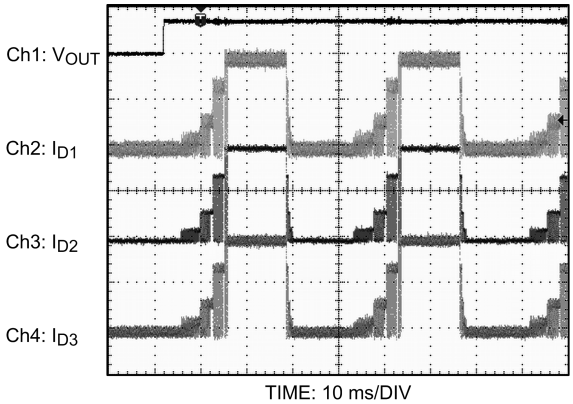

TIME: 10 ms/DIV
Ch1: 5V/Div Ch2: 10 mA/Div
Ch3: 10 mA/Div Ch4: 10 mA/Div

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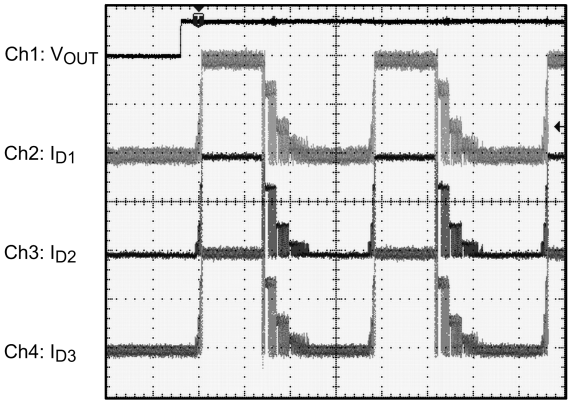

Ch1: 5V/Div Ch2: 10 mA/Div
Ch3: 10 mA/Div Ch4: 10 mA/Div

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Notes

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Ethernet	www.national.com/ethernet	Packaging	www.national.com/packaging
Interface	www.national.com/interface	Quality and Reliability	www.national.com/quality
LVDS	www.national.com/lvds	Reference Designs	www.national.com/refdesigns
Power Management	www.national.com/power	Feedback	www.national.com/feedback
Switching Regulators	www.national.com/switchers		
LDOs	www.national.com/ldo		
LED Lighting	www.national.com/led		
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Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

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