LMH6321 (PSOP and TO-263) Single Open Loop High Speed Buffer Evaluation Boards

National Semiconductor
Application Note 1461
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General Description

The LMH6321MR-EVAL (for the 8-Pin PSOP type package) and the LMH6321TS-EVAL (for the 7-Pin TO263 type package) evaluation boards are designed to aid in the characterization of National Semiconductor's high speed high current buffers. Use the evaluation boards as a guide for high frequency layout and as a tool to aid in device testing and characterization. Both boards have identical circuit configurations and are designed for either inverting or non-inverting gain.

The evaluation board schematic is shown in *Figure 1*. The schematic shows some of the components with the recommended values. Use all surface-mount components.

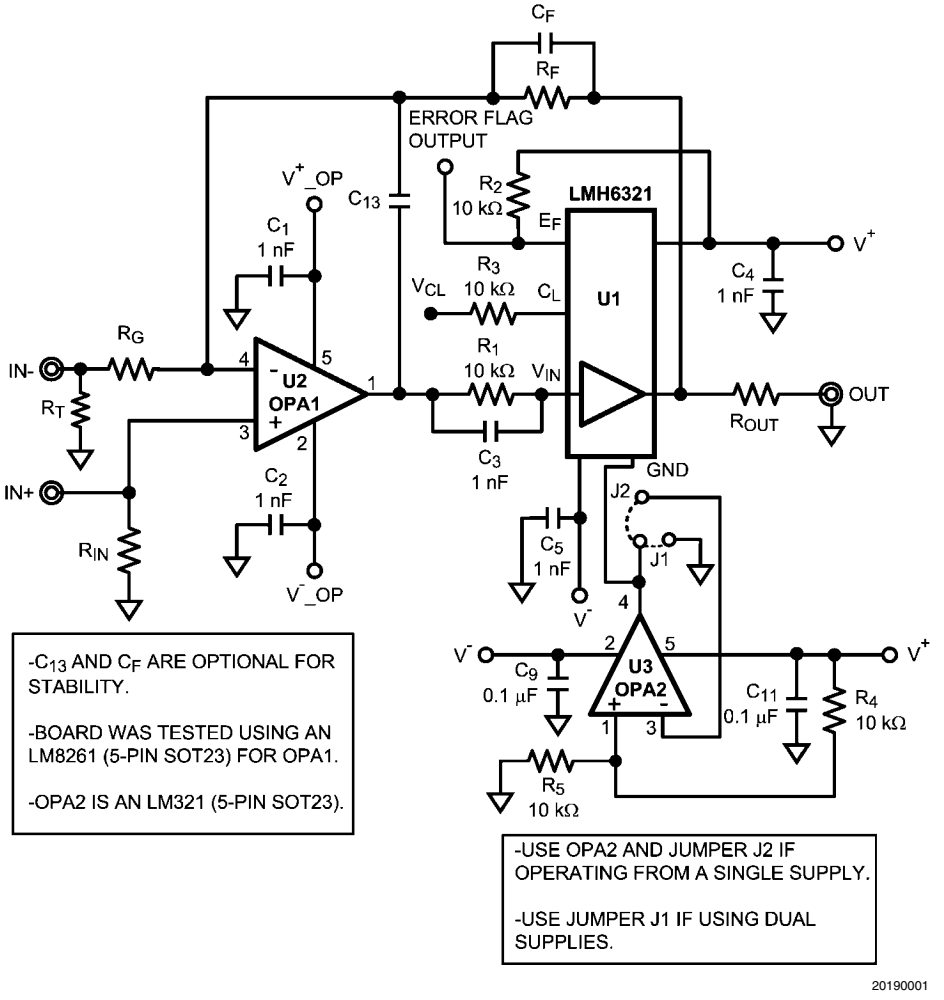


FIGURE 1. Eval Board Schematic

Connection Diagrams

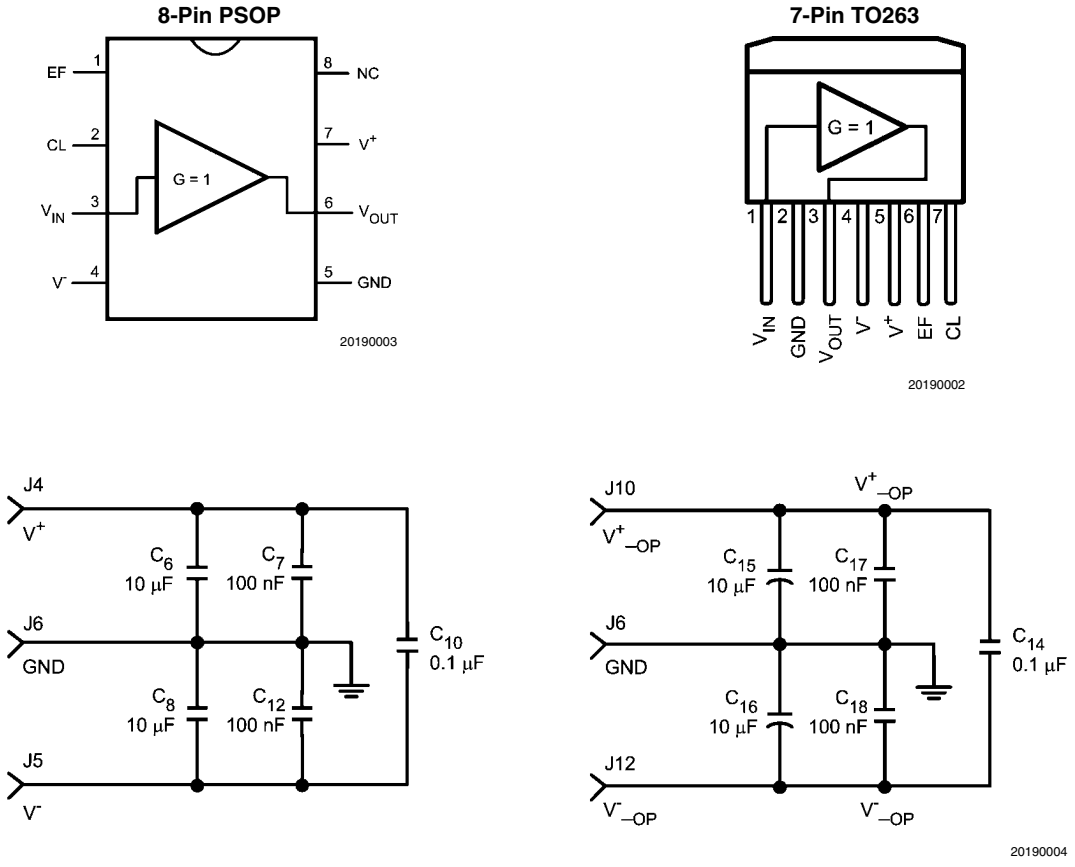


FIGURE 2. Power Supply Connection Diagram

Basic Operation

These boards are a very straight forward design that allows for the evaluation of the LMH6321 in a closed-loop configuration with an op amp. *Figure 1* shows the schematic for both boards. The input signals are brought into the boards via two SMA connectors to either the inverting or non-inverting inputs. No jumpers or modification of the boards is necessary to use one or the other configurations. The resistors R_{IN} and R_T are used to set the input termination resistance to the op amp for non-inverting and inverting operation, respectively. The non-inverting gain is set by the following equation:

$$\text{NON-INVERTING GAIN: } 1 + R_F/(R_G + R_T) \quad (1)$$

The inverting gain is given by:

$$\text{INVERTING GAIN: } R_F/R_G \quad (2)$$

The Op Amp

The boards were tested using the LM8261 in a 5-Pin SOT23 for OPA1 (pre-assembled boards come equipped with this part), but any single op may be used that has the same pin out. In addition, pads for an 8-pin SOIC package are on the opposite side of the board (standard pin out for a single op amp), to increase flexibility in choosing the op amp.

Terminating The Board

The output of the buffer travels through a series resistance, and then leaves the board through an SMA connector. R_{OUT}, matches transmission lines or isolates the output from capacitive loads. The SMA board output traces are optimized for connection to a coaxial cable of 50Ω impedance. That is, the board output traces have a characteristic impedance of 50Ω, thus R_4 can also be used to back-match the output cable. However, by changing R_4, other output impedances can be matched, but keep in mind that by using other termination impedances, e.g., 75Ω, the results will be noticeably different, especially for high frequency response. Even with optimal layout, board parasitics play a large part in high frequency performance, and different termination resistors will change the frequency of the dominant parasitic poles and zeros. To suppress transmission line reflections, it is absolutely necessary to have the impedance at the load end of the connected cable matched to the cable impedance. Also, it should be noted that having the output series resistor matched to the cable impedance will give an additional 6 dB of attenuation. If this attenuation is not acceptable, the circuit can be configured in a gain of 2 to compensate.

The value of R_4 for terminating a 50Ω line, or lines, is not 50Ω. R_4 is in series with the effective output impedance of the buffer/driver, R_{DR}, which is typically 5Ω. Thus the value of R_4 necessary to match the characteristic line impedance, Z_O, should be

$$R_4 = Z_O - (N)(R_{DR}) \quad (3)$$

Where N is the number of driven transmission lines.

When is Termination Needed?

Sometimes we can get away with treating a signal line as a simple trace. However, a trace becomes a transmission line at

$$\text{LENGTH} \geq t_r/6 \times t_{pr} \quad (4)$$

where

t_r is the rise time of a signal pulse

and

t_{pr} is the signal propagation rate

Typical t_{pr} is about 150 ps/inch on a board of FR-4 material.

This formula tells us that the line length beyond which a trace must be treated as a transmission line is a function of rise time and the propagation rate of the signal across the board (a function of board material). When in doubt, always treat the line as a transmission line.

Output Current Selection

The maximum output current (I_{SC}) is continuously adjustable between 10 mA and 300 mA, by programming a current (I_{EXT}) into the C_L pin from 25 µA to 750 µA. This is done by connecting a resistor between the C_L pin and a DC source (V_{CL}). This current is given by

$$I_{EXT} = V_{CL}/R_{EXT} \quad (5)$$

for the GND pin equal to zero volts. In the more general case, where V_{GND} is different from zero volts (i.e., a single supply is used), then (5) becomes

$$I_{EXT} = (V_{CL} - V_{GND})/R_{EXT} \quad (6)$$

(see *Figure 4*)

The relationship between I_{EXT} and I_{SC} is

$$I_{SC} = 400\ I_{EXT} \quad (7)$$

Combining equations (5) and (7), we can write output current in terms of the external resistor, R_{EXT}, and programming voltage, V_{CL}.

$$R_{EXT} = 400\ V_{CL}/I_{SC} \quad (8)$$

(If the V_{CL} pin is left open, the output short circuit current will default to about 700 mA. At elevated temperatures this current will decrease).

As an example, an I_{EXT} of 25 µA or 750 µA will give an I_{SC} of 10 mA or 300 mA, respectively.

As indicated in *Figure 1*, a 10 kΩ resistor (R_3) is recommended (though a wide range of resistance values are possible). In this case the output current can be adjusted directly with V_{CL} over a range of $+0.25V \leq V_{CL} \leq +7.5V$, corresponding to 10 mA and 300 mA, respectively.

Cautionary Notes

1. As mentioned, if dual supplies are used, then the GND pin can be connected to a hard ground via a jumper wire (this is the way assembled boards are shipped). Although the LMH6321 will most often be used with dual supplies, it can be used with a single supply. In this case the GND pin must be set to a voltage of one V_{BE} (~0.7V) or greater, or more commonly, mid rail, by a stiff, low impedance source. This precludes the use of a resistive voltage divider. The reason for this is because, when the error flag turns on, a ground current flows out of the GND pin and if a resistive voltage divider were used, this current would produce a voltage drop that would lift the GND pin, thus causing error in the output current. This is because the GND pin is one of the inputs to the error amplifier in the Current Limit circuit, and C_L is the other input. This amplifier has a large open loop gain, which forces C_L and GND to be at the same potential. Thus any error in the GND pin voltage will force the same voltage at the C_L pin, which will cause an error in the calculated current limit value, *Figure 3*. However, *Figure 4* shows a way to resolve this. An op amp, configured as a buffered voltage source, can be used to drive the GND pin to ½ of V+ when $R_1 = R_2$. The high open loop gain of the op amp forces a very low impedance at the GND pin, which ensures that this pin will be held stiffly at the voltage chosen. The boards come equipped with a circuit that does this. The pin out is standard for an 8 pin single op amp. An LM321 is used on pre-assembled boards, as shown in *Figure 1*.

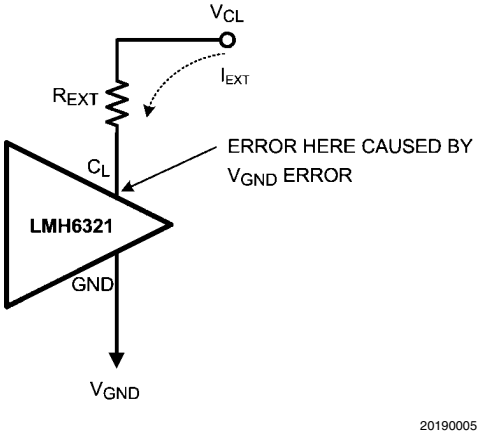


FIGURE 3.

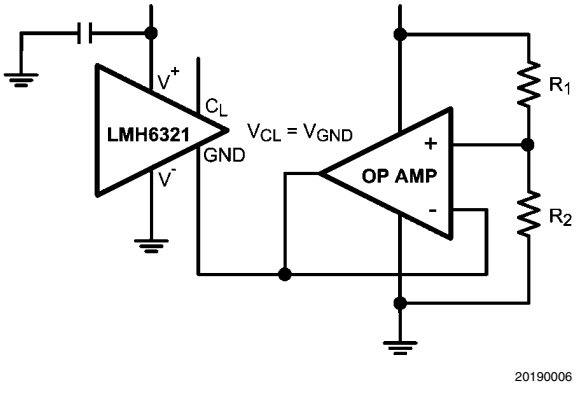


FIGURE 4.

2. A few degrees before the thermal shutdown temperature (~160 to 165C) is reached the part is starting to shutdown and the error flag will show an oscillation. This does not affect the proper functioning of the thermal shutdown. Typical oscillation frequency is 700 to 900 kHz.
3. Keep parasitic capacitance to a minimum at the C_L and GND pins, as they are the input and output of an on-Chip amplifier configured as a buffer.
4. Adding a buffer inside any op amp feedback loop will add another pole (phase lag) to the response. If the unity gain crossing of op amp is near the gain-bandwidth of the buffer the over-all phase lag of the circuit will consume most, if not all of the available phase margin, and oscillation will occur. For this reason it is important that the buffer has a GBW significantly larger than that of the op amp, so that loop performance will be determined solely by the op amp. With most general purpose, precision, and low power op amps, the bandwidth of the LMH6321 is so great that the op amp totally controls the loop stability. If however, a wideband op amp is used, the phase margin and open loop frequency response can be altered by the additional pole(s) contributed by the buffer and this should be taken into consideration. The buffer phase shift is algebraically summed with the op amp phase shift, and may cause a stable op amp loop to become marginally stable (large overshoot, ringing), depending on the relative positions of the op amp and buffer poles. In the application shown in *Figure 1*, the LM8261 op amp (OPA1) has a GBW of 15 MHz, while the –3d B bandwidth of the LMH6321 is greater than 100 MHz, giving sufficient loop phase margin. Optional pads have been added to the EVAL boards to allow for the addition of compensating capacitors CC and C_F, should they prove necessary.

Layout Considerations

Printed circuit board layout and supply bypassing play major roles in determining high frequency performance. When designing you own board use these evaluation boards as a guide and follow these steps to optimize high frequency performance:

1. Use a ground plane
2. Include large (10 µF tantalum) bypass capacitors (C_6 and C_8 in *Figure 1*) from both supplies to ground.
3. As near to the device as practicable, use 0.1 nF ceramic capacitors (C_1, C_2, C_4, C_5) from both supplies to ground. Try to position these less than 0.1 inch from power pins.
4. Remove the ground and power planes from under the input and output pins.

5.6. Minimize all trace lengths to reduce series inductance

Use terminated transmission lines for long signal traces.

7. The op amp and the buffer are powered from different supply pins, thus allowing for a low voltage op amp to be used even when the buffer is being powered with the full ±15V it is capable of.

The capacitor between both supplies (C_{10}) is recommended for best 2nd harmonic distortion performance. The optional zener diode (ZD) between both supplies protects the device from reverse polarity supply connections, under the condition these supplies have the current limit on.

Error Flag Operation

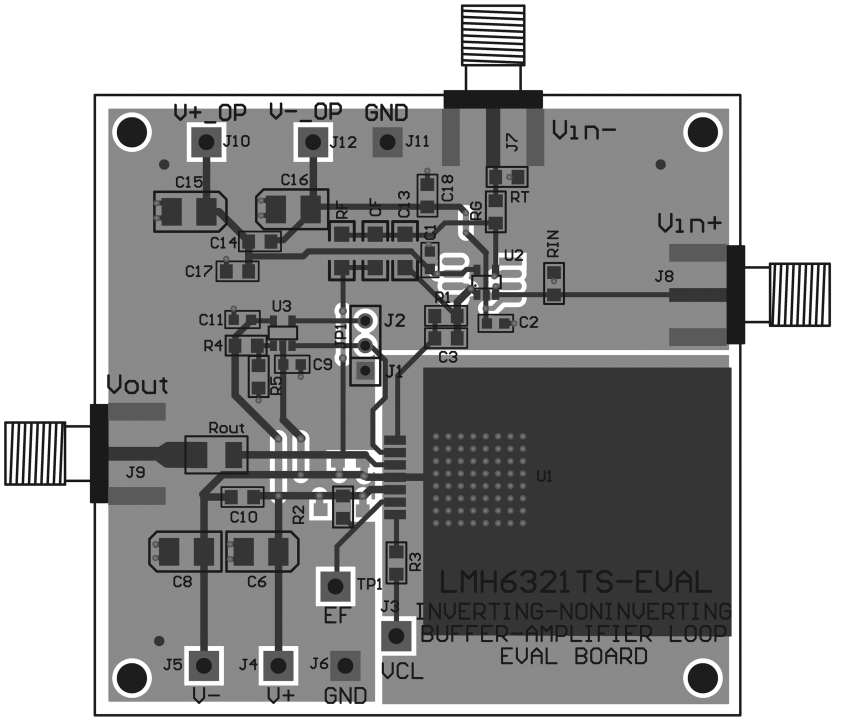
The LMH6321 provides an open collector output at the EF pin that produces a low voltage (Flag transistor ON) when the Thermal Shutdown protection is engaged, due to a fault condition. Under normal operation, the Error Flag pin is pulled to V^+ by an external resistor. When a fault occurs that causes the die temperature to rise to about 165°C, the EF pin goes low, but then returns to V^+ when the fault disappears. This voltage change can be used as a diagnostic signal to alert a microprocessor of a system fault condition. If this function is used, a 10 kΩ pull-up resistor (R_2 in *Figure 1*) is recommended, but larger resistors may be used. The larger the resistor the lower will be the voltage at this pin under thermal shutdown. *Table 1* shows some typical values of V_{EF} for 10 kΩ and 100 kΩ. If the error flag function is not used, the EF pin should be tied to ground.

TABLE 1. V_F vs. R_2 *Figure 1*

R_2	@ V^+ = 5V	@ V^+ = 15V
10 kΩ	0.24V	0.55V
100 kΩ	0.036V	0.072V

Board Layout

7-Pin TO263



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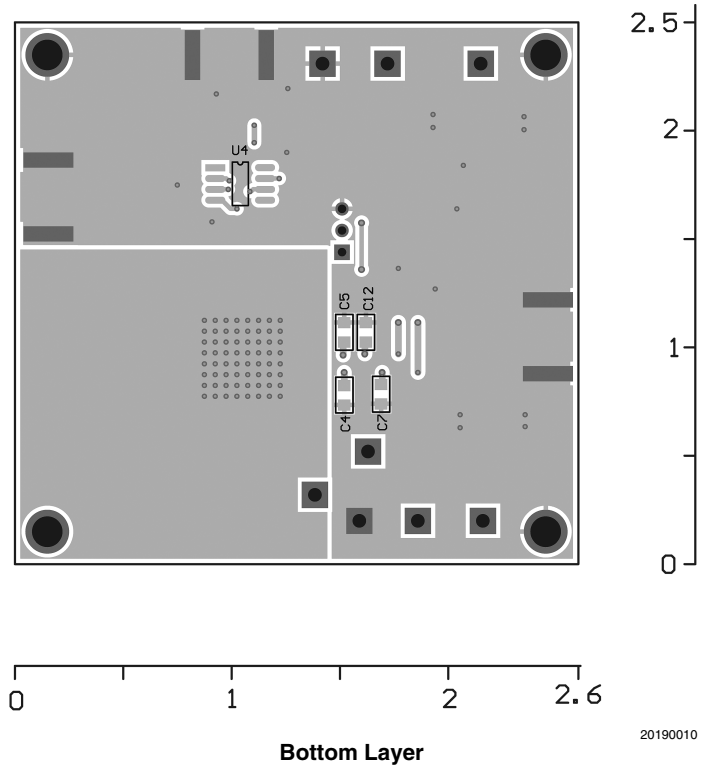

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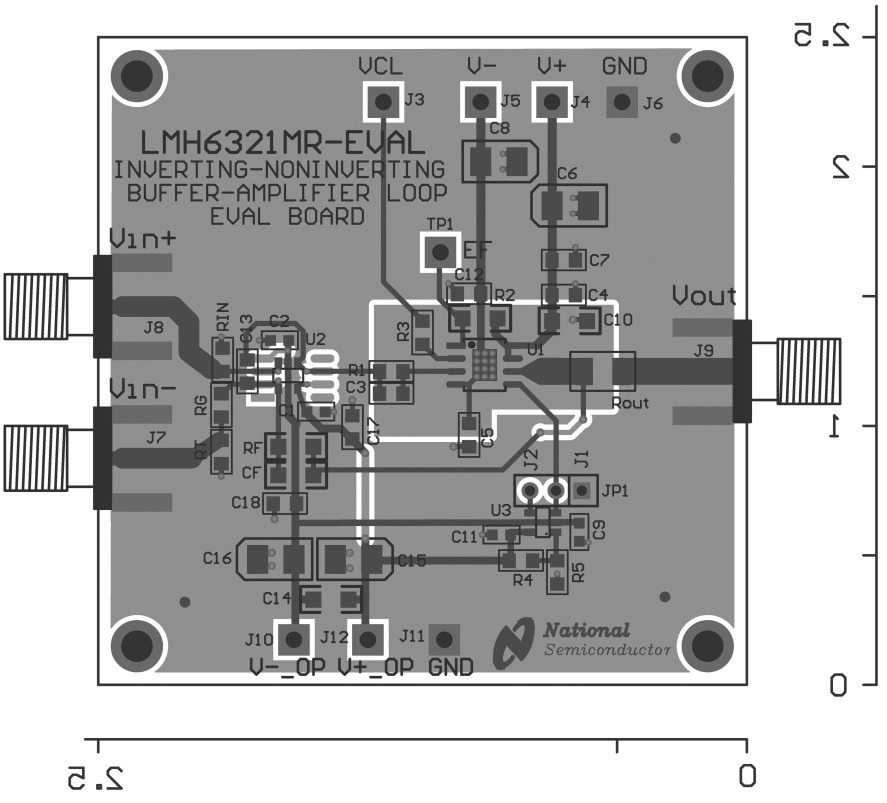
8-Pin PSOP



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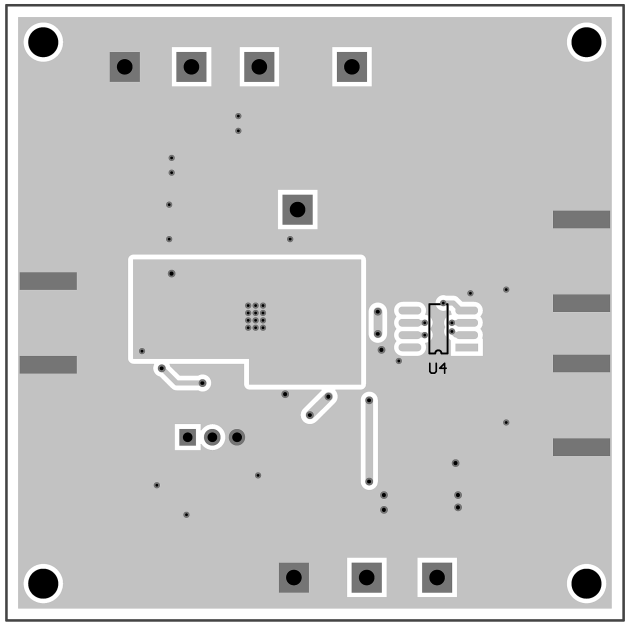

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Notes

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