

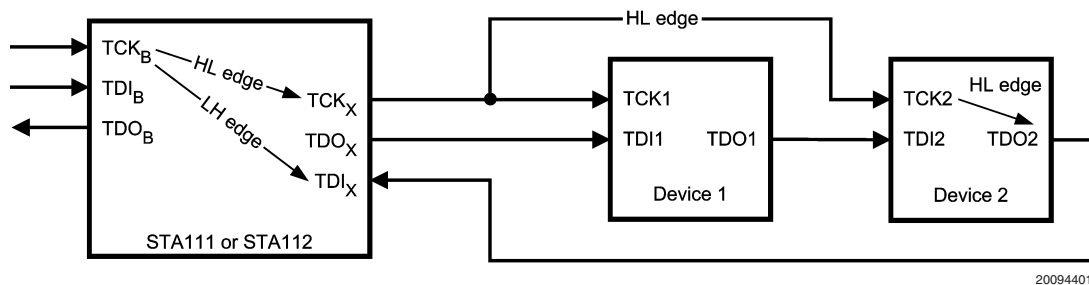
# Scan Bridge (STA111/STA112) Timing

National Semiconductor  
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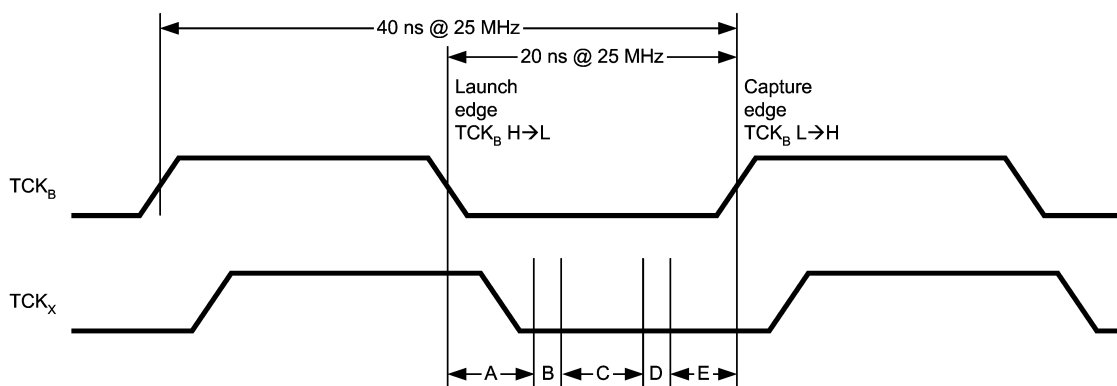
When multiple devices are connected to an STA111 or STA112 local scan port (LSP), there are delays associated with the LSP path of the local scan chain that must be considered during timing analysis. Because of the propagation delay of the STA111/112 and the delay through any devices on the LSP, the tester (backplane) TCK is delayed as it is propagated thru the local scan chain.

For proper operation of the STA111/112, it is a requirement that Instruction and Data must be sent and captured in one clock cycle of  $TCK_B$ . It is critical that this capture occurs before the rising edge of the next clock cycle (Figure 2).



Basic Scan Bridge block diagram

FIGURE 1.



A = Propagation delay  $TCK_B$  to  $TCK_X$   
B = Board delay,  $TCK_X$  to  $TCK_2$   
C = Chain Propagation delay,  $TCK_2$  to  $TDO_2$   
D = Board delay,  $TDO_2$  to  $TDI_X$   
E = Setup time,  $TDI_X$  to  $TCK_B$

Scan Bridge Timing Diagram

FIGURE 2.

Consideration must be taken for the propagation delay of each device or element in the local chain, including the board delay. For the above example (Figure 1), the total delay from the  $TCK_B$  HL edge to "valid data present" at  $TDI_X$  (for capture by the LH  $TCK_B$  edge) is the sum of:

- Propagation delay  $TCK_B$  to  $TCK_X$  (typically 8ns)
- Board delay,  $TCK_X$  to  $TCK_2$  (typically 1ns)
- Chain Propagation delay,  $TCK_2$  to  $TDO_2$  (typically 8ns)
- Board delay,  $TDO_2$  to  $TDI_X$  (typically 1ns)

- Setup time,  $TDI_X$  to  $TCK_B$  (typically 3ns)

For more details regarding the operation of the SCANSTA111 or SCANSTA112, refer to the following documentation available on our website at <http://www.national.com/scan>:

- SCANSTA111 Datasheet
- SCANSTA112 Datasheet
- AN-1259, SCANSTA112 Programmers reference

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