LM3678 Evaluation Board

National Semiconductor
Application Note 1722
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Introduction

The LM3678 evaluation board is a working demonstration of a synchronous buck DC-DC converter. This application note contains information about the evaluation board. For more details and electrical characteristics about the converter operation, please refer to the LM3678 datasheet.

Operating Range

- V_{IN} range: 2.5V to 5.5V
- Recommended load current: up to 1.5A
- V_{OUT} = 0.8/1.2V

Package

LLP-10 no-pullback (3mm x 3mm x 0.8mm)

Typical Application

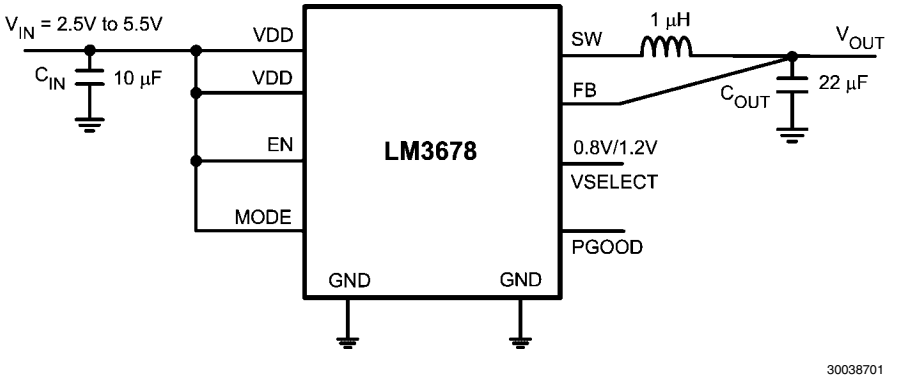
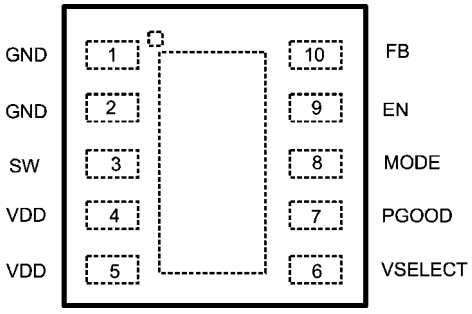
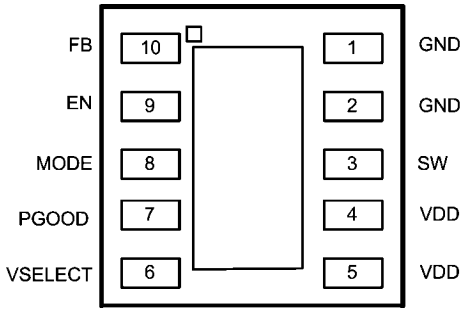


FIGURE 1. Typical Application Circuit

Connection Diagrams



Top View



Bottom View

Note: the above figures are not to any actual scale

Pin Descriptions

Pin#	Name	Description
1	GND	Ground
2	GND	
3	SW	Switching node connection to the internal PFET switch and NFET synchronous rectifier.
4	VDD	Power supply input. Connect to the input filter capacitor (*Figure 1*).
5	VDD	
6	VSELECT	Output Voltage Select. For Example : VSELECT = LOW V_{OUT} = 0.8V VSELECT = HIGH, V_{OUT} = 1.2V
7	PGOOD	Power Good Flag. This common drain logic output is pulled to ground when the output voltage is not within ± 7.5% of regulation.
8	MODE	Mode Control Pin: Mode = 1 selects forced PWM mode Mode = 0 selects auto PFM-PWM mode
9	EN	Enable Pin. The device is in shutdown mode when voltage to this pin < 0.4V and enabled when > 1.0V. Do not leave this pin floating.
10	FB	Feedback Analog Input. Connect directly to the output filter capacitor for fixed voltage versions.
DAP	DAP	Die Attach Pad; connect the DAP to GND on PCB layout to enhance thermal performance. It should not be used as a primary ground connection.

Powering the LM3678 for Bench Measurements

When powering the LM3678 with a bench power supply, it is recommended to place a 100µF tantalum capacitor across the VIN and GND supply terminals of the bench power supply. This capacitor will reduce the input spike caused by the power supply and long power cables. The combination of the power supply and inductance within the power cables produce a large voltage spike that may damage the device. In addition, consideration must be given to the enable pin of the device. The enable should never be taken high, until minimum guaranteed operating voltage of 2.7V is reached. The enable pin should also never exceed the input voltage.

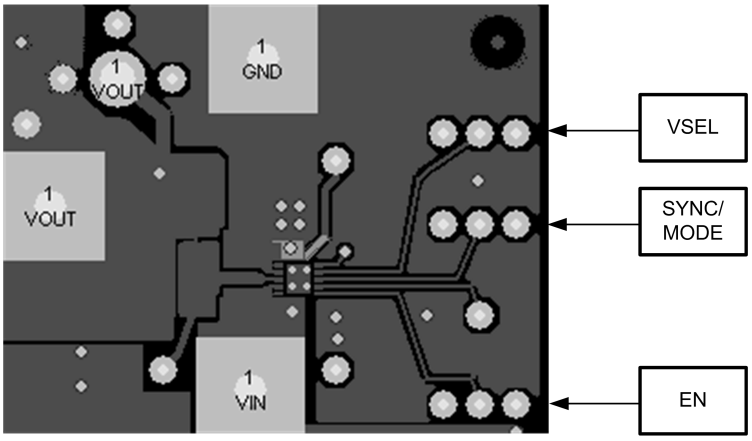
Operating Information

The LM3678 evaluation board is set for the following default positions:

- V_{OUT} = 1.2V, for 0.8V, set VSELECT pin to low via jumper
- Mode = H (PWM Mode), for Auto Mode, set Mode = Low (move jumper to inner position).
- EN pin is tied to V_{IN} via a jumper

Evaluation Board Layout

LM3678 is a four-layer board designed to maximize the performance. Top layer consists of high-current path and bottom layer for low-current and logic signals path. Inner layer 1 and layer 2 are dedicated for PGND (power GND) and SGND (analog and logic GND). For optimum performance, it is recommended to separate the PGND and SGND pins and join them together at the start GND on the PCB.



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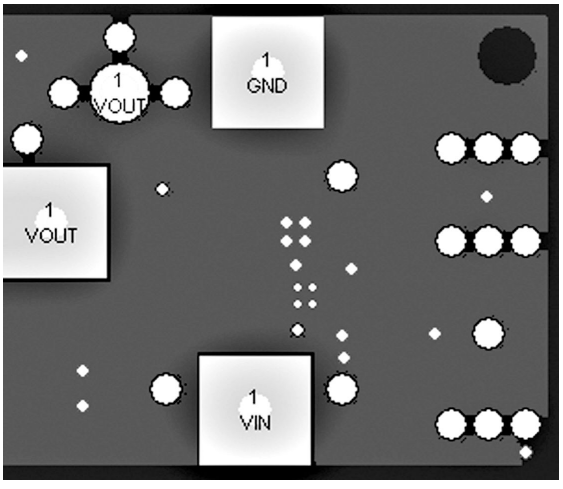
Top Layer



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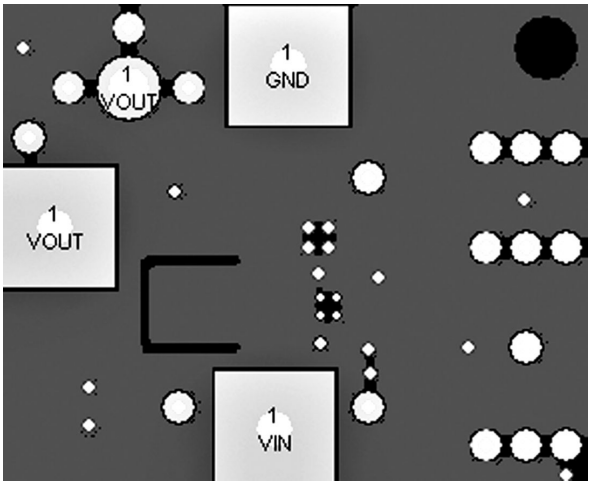
Mid Layer 1



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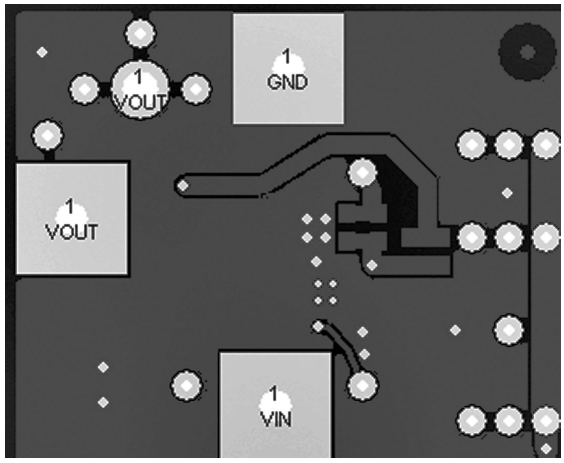
Mid Layer 2



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Bottom Layer

BOM for LM3678

BOM

Component Name	Manufacturer	Specification	Case Size
LM3678SD	NSC	LLP-10	3mm x 3mm x 0.8mm
C1 = 10µF	Taiyo-Yuden	JMK212BJ106K	0805 (2012)
C2 = 22µF		JMK212BJ226MG	0805 (2012)
Inductor	Taiyo-Yuden	NR4012T-1RON	4mm x 4mm x 1.2mm
R1	Vishay/any manufacturer	0603	0Ω

TEST POINT

V_{SEL}, Mode & EN	**Header**	**3 in series 3 (3 x 1)**
V_{SEL}, Mode & EN	Jumper Female (Handle centerline)	A26242–ND
V_{IN} banana jack - red	Johnson Components	108–0902–001
V_{OUT} banana jack - yellow	Johnson Components	108–0907–001
GND banana jack - black	Johnson Components	108–0903–001

Notes

Notes

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