LMK04000 Family Phase Noise Characterization

National Semiconductor
Application Note 1910
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1.0 Introduction

The purpose of this applications report is to present phase noise and jitter measurements representing the clock outputs of the LMK04000 family of Precision Clock Conditioners, when paired with various voltage controlled oscillators (VCXOs). The intent is to illustrate the relationship between clock output phase noise and VCXO phase noise. The LMK04000 family provides superior jitter cleaning capability by employing a dual, cascaded phase locked loop (PLL) architecture. A generic example of a dual PLL architecture is shown in Figure 1. The figure also shows a clock distribution section following the VCO output.

The first PLL utilizes a narrow loop bandwidth to frequency lock the external VCXO to the incoming reference clock. The narrow loop bandwidth rejects most of the phase noise associated with the reference clock, allowing the VCXO phase noise to dominate. The frequency-locked VCXO is injected as the reference clock to the second PLL that employs a wider loop bandwidth to lock an internal VCO. This wider loop bandwidth means the VCO is both phase and frequency-locked to the VCXO, thus the VCXO phase noise dominates. For phase noise offsets higher than the loop bandwidth, the internal VCO phase noise and the output dividers and drivers will determine the output phase noise. This can be illustrated more explicitly by considering the total phase noise at the output of the synthesizer. Because the synthesizer noise determines the clock output noise, it is sufficient to only look at the synthesizer noise. The following equation shows that the total noise is the weighted sum of reference clock noise, PLL noise and VCO noise:

$$S_{TOTAL}(f) = S_{REF}(f) \bullet G^2_{REF} \bullet |H(f)|^2 + S_{PLL}(f) \bullet G^2_{PLL} \bullet |H(f)|^2 + S_{VCO}(f) \bullet |1 - H(f)|^2$$

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The weighting function H(f) is the lowpass closed loop transfer function, formed by parameters such as the charge pump gain, loop filter response, VCO gain, and feedback path (N) counter. This equation represents the noise model at the output of each of the PLL stages shown in *Figure 1*. The gains associated with the reference clock noise (G_{REF}) and PLL noise (G_{PLL}) are also functions of specific loop parameters. Though the explicit expressions for these gains and closed loop response H(f) are not derived here, the relevance of this equation can still be seen. In general, the synthesizer parameters that comprise H(f) and the gain values represented in the equation are under the control of the designer and should be chosen such that the overall noise at the synthesizer output (S_{TOTAL}(f)) is minimized. In this case, minimization means achieving the smallest integrated noise. When the noise equation is applied to PLL2, S_{REF}(f) represents the VCXO noise. In the case of the LMK04000 family, S_{PLL}(f) and S_{VCO}(f) are "fixed" by the device characteristics, but S_{REF}(f) is dependent on the VCXO chosen by the designer. *Therefore it is important to select a VCXO that supports the phase noise and jitter requirements of the target application*.

The inclusion of a particular VCXO model or manufacturer in this report does not constitute an endorsement by National Semiconductor. The purpose of the data contained in this report is to offer the reader some insight on the direct relationship between the phase noise and jitter performance of the total clocking solution and VCXO characteristics.Though no VCXO cost data is presented here, there is a significant correlation between VCXO cost and performance. The LMK04000 family is targeted toward applications that require jitter cleaning, frequency synthesis and multiple clock distribution. While the LMK04000 family offers the industry's best performance in these categories, not all applications require the same level of performance. Hence, the LMK04000 family offers designers the capability to tailor the cost and performance of their clocking solutions by selecting the VCXO that best meets the overall needs of the application. This objective is further enhanced through the built-in features of the LMK04000 family that support the use of discretely implemented external crystal oscillators as well as off-the-shelf VCXO modules. The use of external crystal oscillators is addressed in a separate applications report.

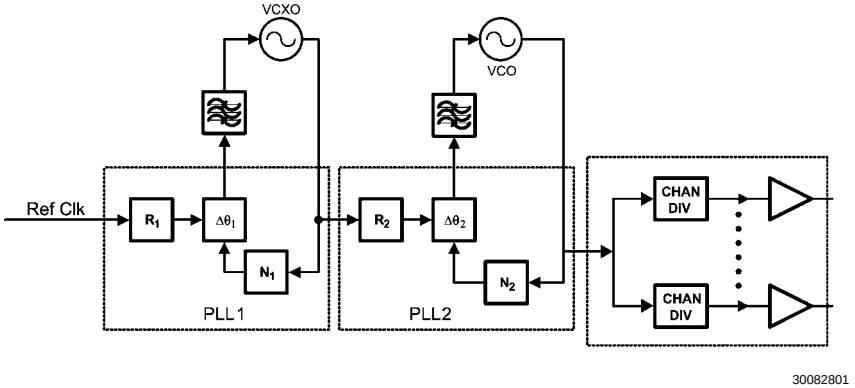

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FIGURE 1. Dual-PLL Jitter Cleaning Clock Synthesizer Architecture

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2.0 LMK04000 Family Description

Figure 2 shows a detailed block diagram of the LMK04000 Precision Clock Conditioner family. The redundant reference clock inputs (CLKin0, CLKin1) for PLL1 support frequencies up to 400 MHz. The reference clocks may be either single-ended or differential, and an auto-switching mode can be enabled for fail-safe operation. The maximum allowable frequency of the VCXO driving the OSCin port is 250 MHz. The signal at the OSCin port is fed back to the PLL1 phase comparator and is also injected to PLL2 as a phase and frequency reference. Though not shown in the diagram, there is internal support for a discretely implemented VCXO using an external crystal resonator. An optional frequency doubler path for the reference input to the PLL2 phase comparator allows the phase comparison frequency to be increased, thereby lowering the in-band noise of PLL2. An internal VCO is integrated with PLL2, along with optional internal loop filter components that support 3rd and 4th order poles for the PLL2 loop filter. The VCO output is buffered and made available at the Fout pin, and is also routed through a VCO divider to the internal clock distribution bus. The clock distribution section buffers and divides the bus clock through separately configured channels. Each channel features a divider, delay block and output buffer. The mixture of signal formats at the clock outputs is fixed according to the specific device part number.

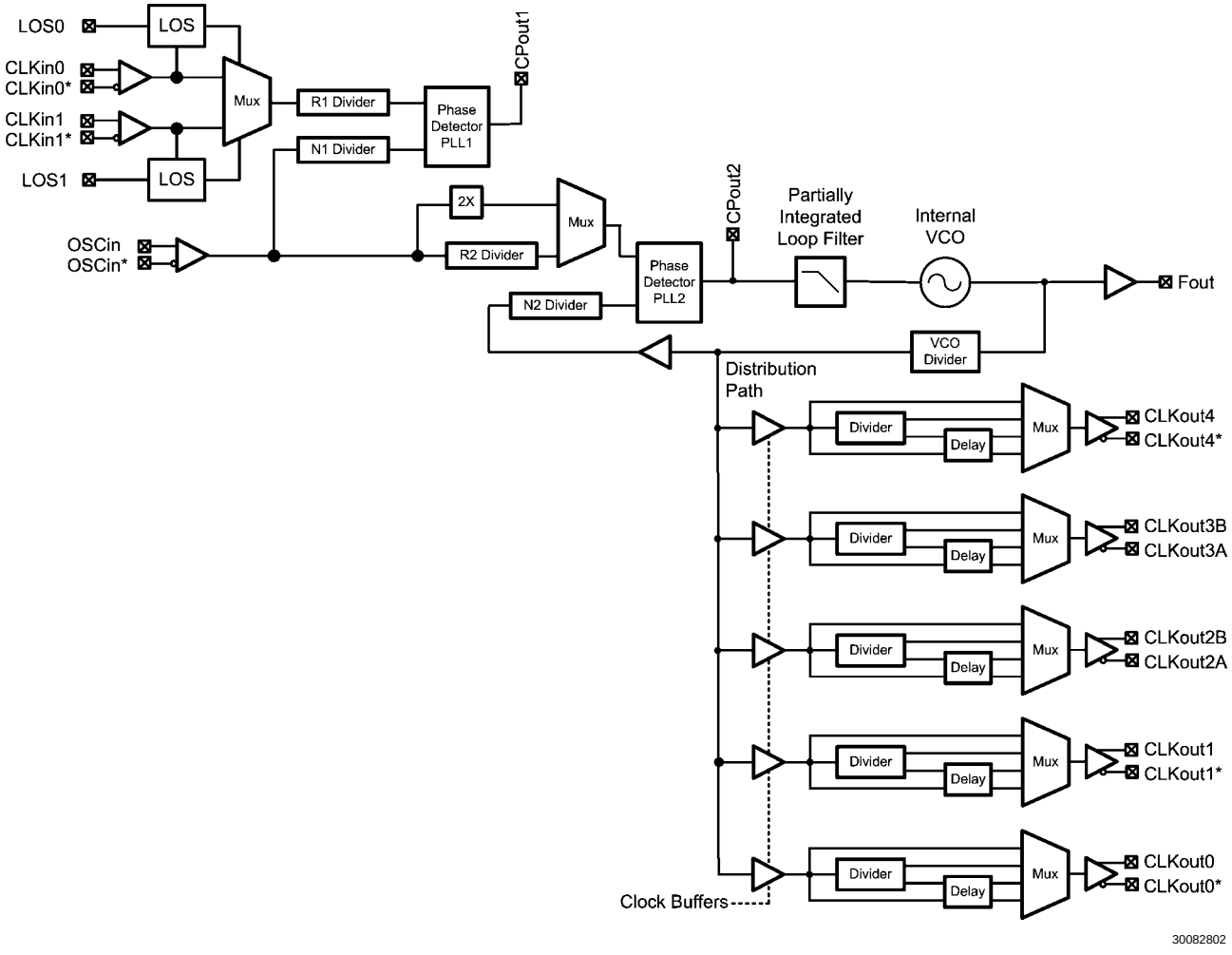

FIGURE 2. LMK04000 Family Block Diagram

The following table shows the currently released devices of the LMK04000 family. As *Table 1* shows, two VCO frequency bands are offered along with two configurations of clock output formats. The device used for the measurements reported here was the LMK04031.

TABLE 1. LMK04000 Family Part Numbers, Output Formats and VCO Bands

NSID	PROCESS	2VPECL/LVPECL OUTPUTS	LVDS OUTPUTS	LVCMOS OUTPUTS	VCO FREQUENCY RANGE
LMK04011BISQ	BiCMOS	5			1430 to 1570 MHz
LMK04031BISQ	BiCMOS	2	2	2	1430 to 1570 MHz
LMK04033BISQ	BiCMOS	2	2	2	1840 to 2160 MHz

3.0 LMK04000 Clock Output Phase Noise and Jitter

Various VCXOs were paired and tested with the LMK04031. The phase noise and jitter was measured at the clock outputs using an Agilent E5052A Signal Source Analyzer. The loop filters for PLL1 and PLL2 were fixed for all measurements. They are shown in *Figure 3*. The closed loop bandwidth was adjusted either by the charge pump current or by adjusting the phase comparison frequency. The VCXOs cover various frequencies, so the measured clock frequencies vary, but are in the range of 122.88 MHz to 129 MHz. *Figure 4* illustrates the test setup for the measurements.

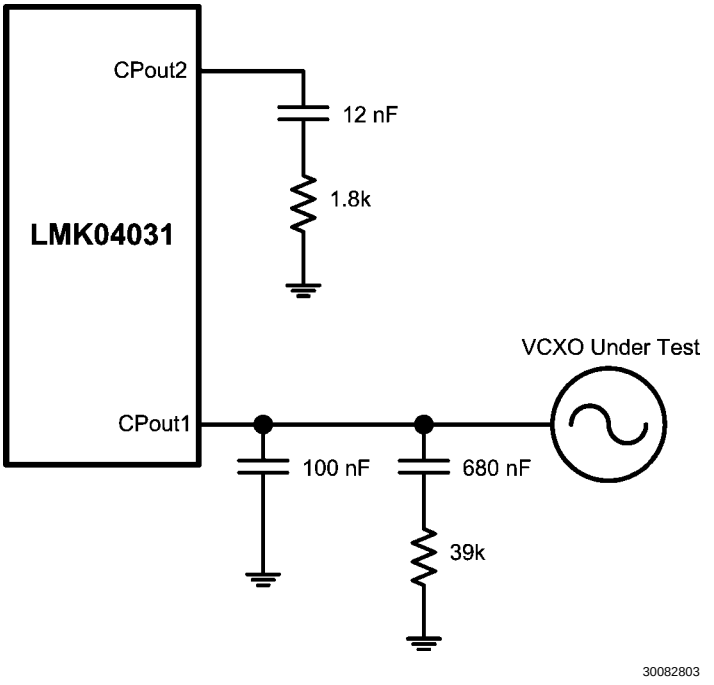

FIGURE 3. PLL1 and PLL2 Loop Filter Components

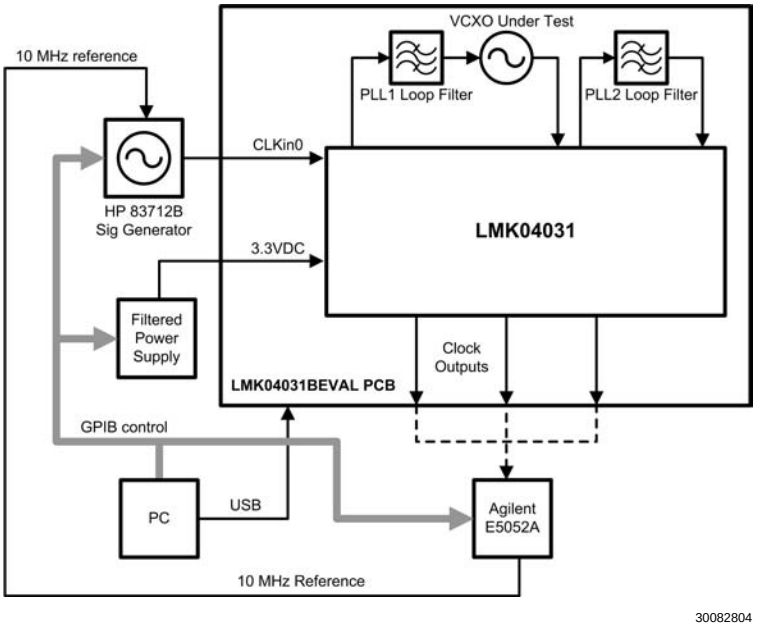

FIGURE 4. Phase Noise and Jitter Measurement Test Setup

The following table summarizes the RMS jitter measured at the Fout pin (buffered VCO output) and at clock output pins for LVDS, LVCMOS and LVPECL clock types. For all jitter measurements at the LMK04031 outputs, the integration bandwidth is 100 Hz to 20 MHz. The VCXO RMS jitter values listed in the table are based upon a measurement bandwidth of 100 Hz to 200 kHz. 200 kHz was chosen as the upper limit because in most cases the loop bandwidth employed for PLL2 will not exceed 200 kHz, and so the VCXO contribution to total jitter beyond a 200 kHz offset is insignificant. Furthermore, because the measurement bandwidth is consistent for all of the VCXOs represented in this note, one can make useful comparisons between them when determining suitability for a particular application.

TABLE 2. Summary of RMS Jitter Measurements

VCXO MODEL		VCXO		LMK04031					
		FREQ (MHz)	**RMS JITTER (fs)** (Note 1)	**Fout FREQ (MHz)**	**Fout RMS JITTER (fs)** (Note 2)	**CLOCK OUTPUT FREQ (MHz)**	**LVDS RMS JITTER (fs)** (Note 2)	**LVPECL RMS JITTER (fs)** (Note 2)	**LVCMOS RMS JITTER (fs)** (Note 2)
pp. 6-9	CTS Model 357	61.44	311	1474.56	390.3	122.88	398.6	413.1	416.2
pp. 10-14	Crystek CVHD-950	122.88	32	1474.56	127.8	122.88	160.7	170	149.9
pp. 15-19	Crystek CVHD-950	80	71	1520	165.5	126.66666	193.1	202.8	178.6
pp. 20-24	Crystek CVPD-920	61.44	285	1474.56	337.5	122.88	339.9	356	335.6
pp. 25-29	Epson Toyocom VG-4501	61.44	143	1474.56	230.2	122.88	250.4	264.2	237.3
pp. 30-34	Epson Toyocom VG-4231	19.44	383	1516.32	609.8	126.36	635.7	615.6	618.8
pp. 35-39	Epson Toyocom TCO-2111-AA	245.76	74	1474.56	148.1	122.88	183.3	184.4	163.1
pp. 40-44	Suntsu SVD series	54	336	1512	486.3	126	497.2	495.4	491.9
pp. 45-49	Suntsu SVD series	61.44	295	1474.56	489	122.88	495.9	494.9	491.2
pp. 50-54	Suntsu SVD series	30.72	655	1474.56	842.5	122.88	860.2	872.6	838.8
pp. 55-59	Vectron 5310	155.52	110	1555.2	155.7	129.6	179.5	187.6	169.1
pp. 60-64	Vectron 5310	134.40	82	1523.2	155.5	126.93333	181.8	191.6	169.6

Note 1: Integration bandwidth for VCXO jitter is 100 Hz to 200 kHz

Note 2: Jitter integration bandwidth for clock measurements is 100 Hz to 20 MHz

The remainder of this report presents phase noise plots captured using the E5052A. Each VCXO section begins with a table that lists the reference clock frequency, PLL1 phase comparison frequency and closed loop bandwidth, and the PLL2 phase comparison frequency and closed loop bandwidth. Each VCXO section also contains a plot of the open loop phase noise of the VCXO, and closed loop phase noise plots of the LMK04031 outputs.

3.1 Phase Noise Plots

TABLE 3. CTS Model 357, 61.44 MHz

Reference Clock (MHz)	F_{comp1} (MHz)	PLL1 Loop BW (Hz)	F_{comp2} (MHz)	PLL2 Loop BW (kHz)
30.72	1.024	30	30.72	95.4

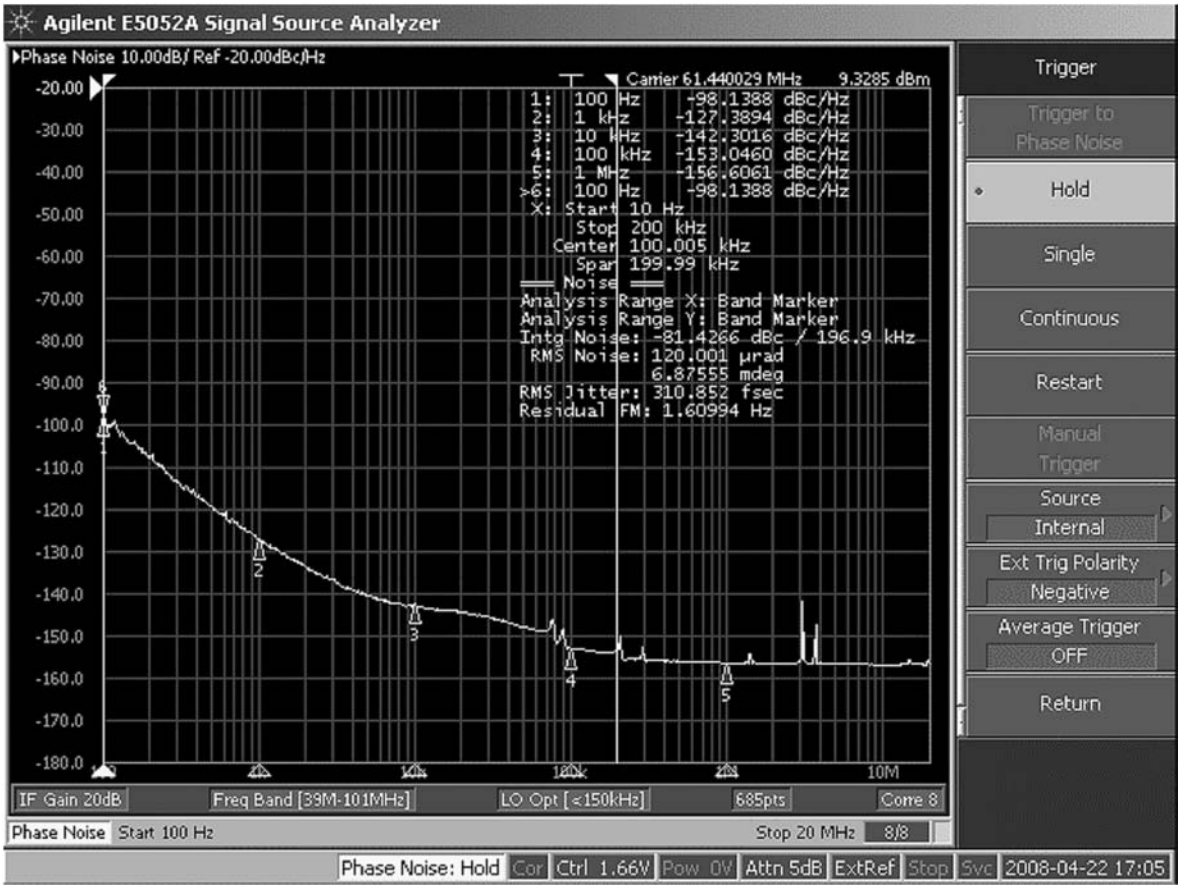

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FIGURE 5. CTS Model 357 VCXO Open Loop Phase Noise, 61.44 MHz

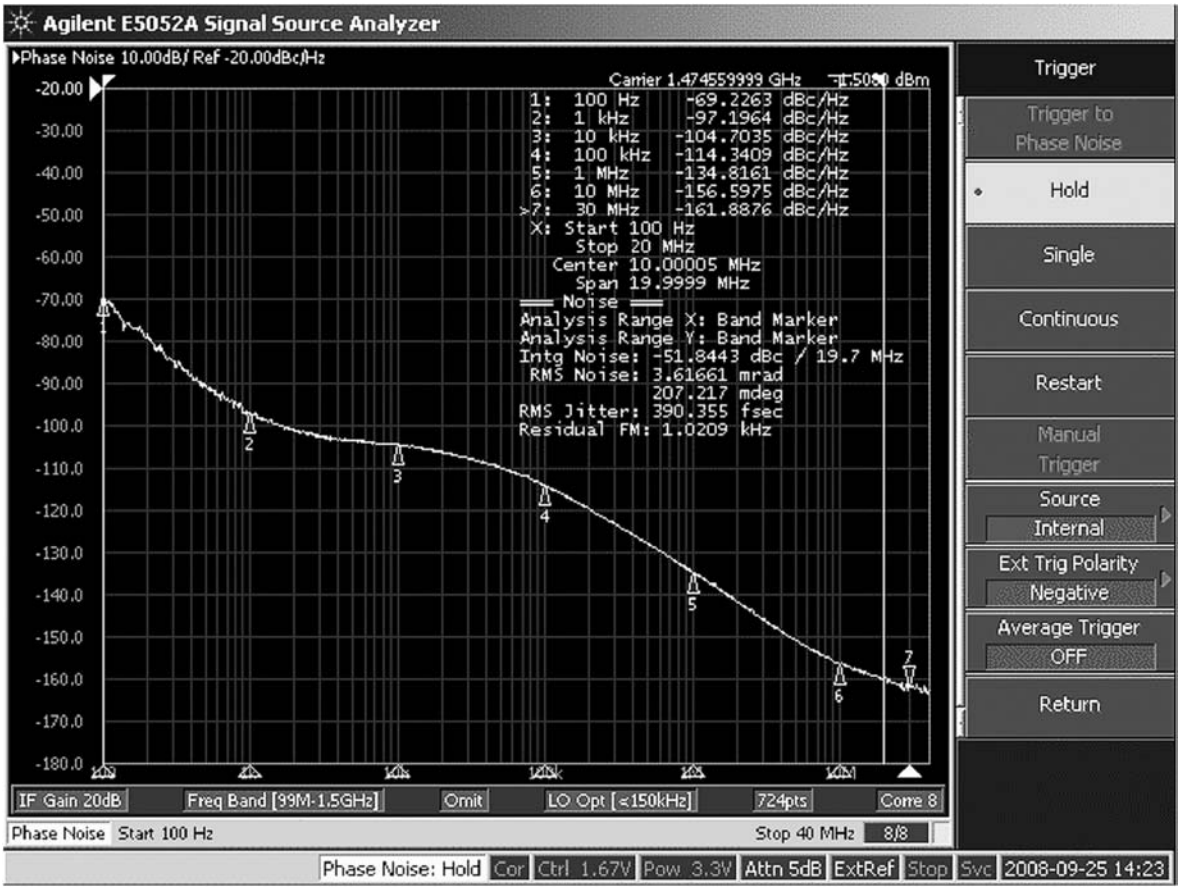

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FIGURE 6. LMK04031 Fout Phase Noise, CTS model 357 VCXO

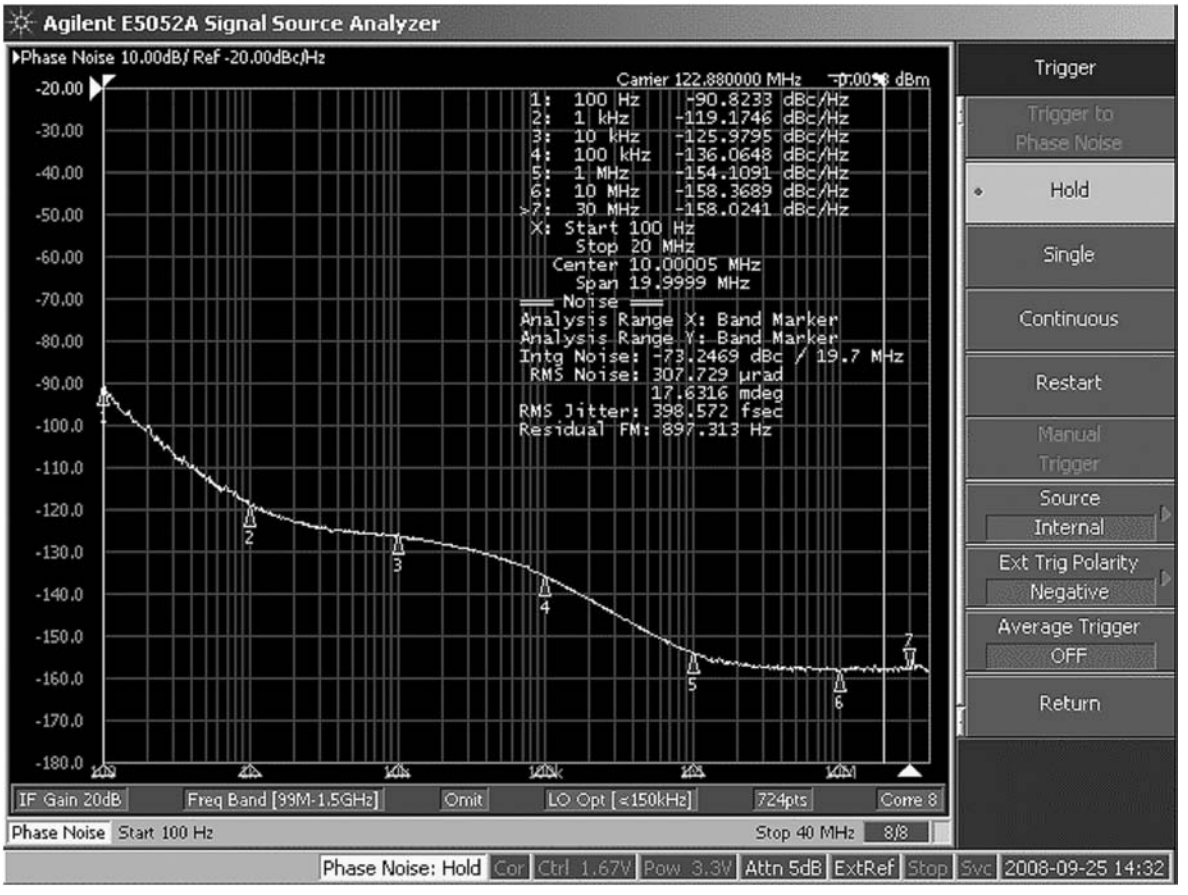

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FIGURE 7. LMK04031 LVDS Phase Noise, CTS model 357 VCXO

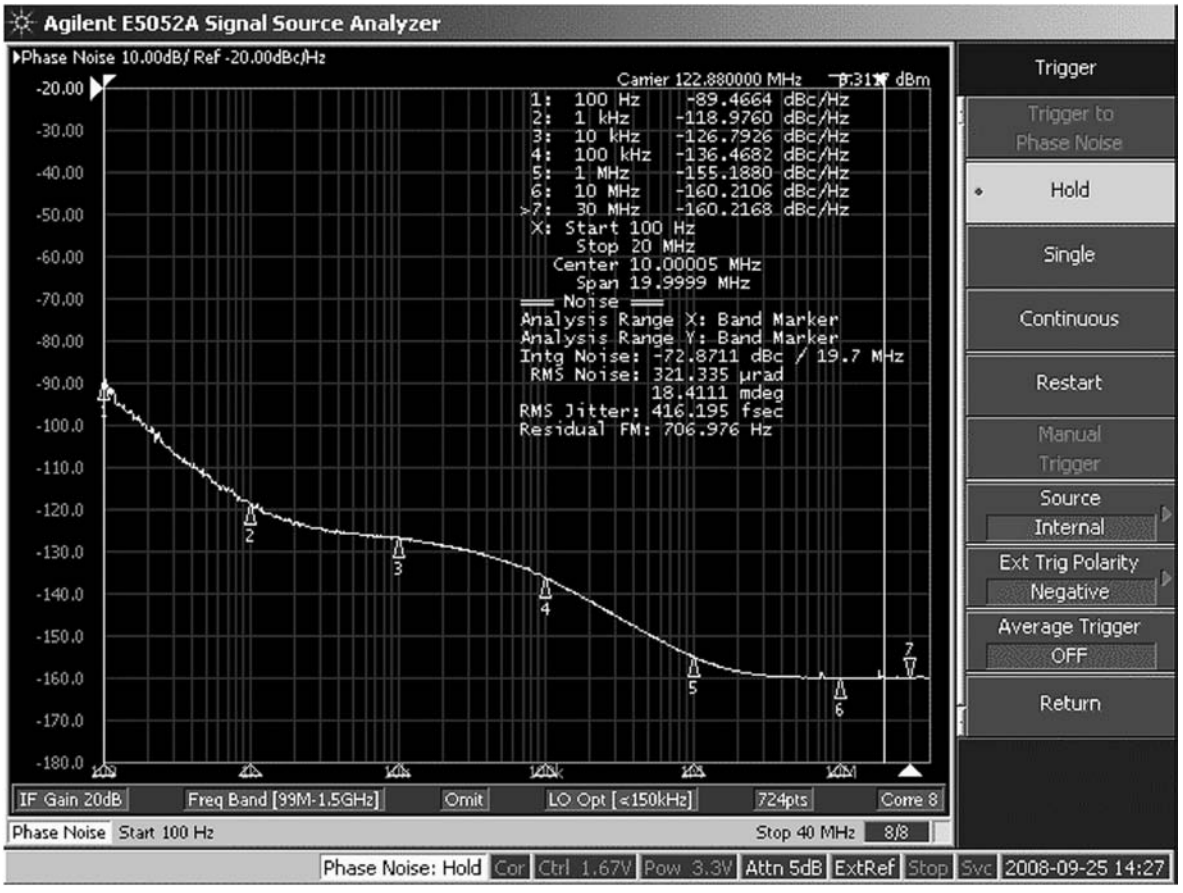

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FIGURE 8. LMK04031 LVCMOS Phase Noise, CTS model 357 VCXO

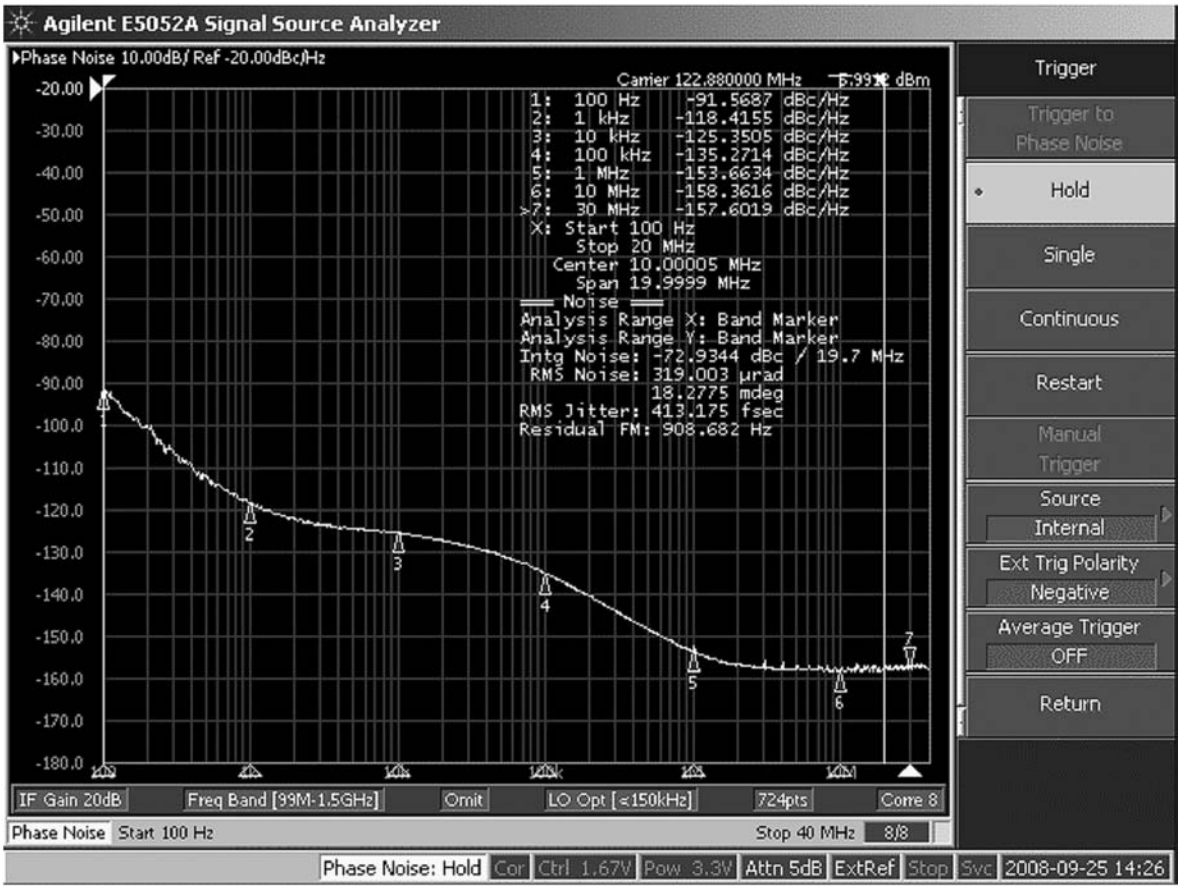

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FIGURE 9. LMK04031 LVPECL Phase Noise, CTS model 357 VCXO

TABLE 4. Crystek CVHD-950-122.88MHz

Reference Clock (MHz)	F_{comp1} (MHz)	PLL1 Loop BW (Hz)	F_{comp2} (MHz)	PLL2 Loop BW (kHz)
122.88	1.024	20	61.44	189.7

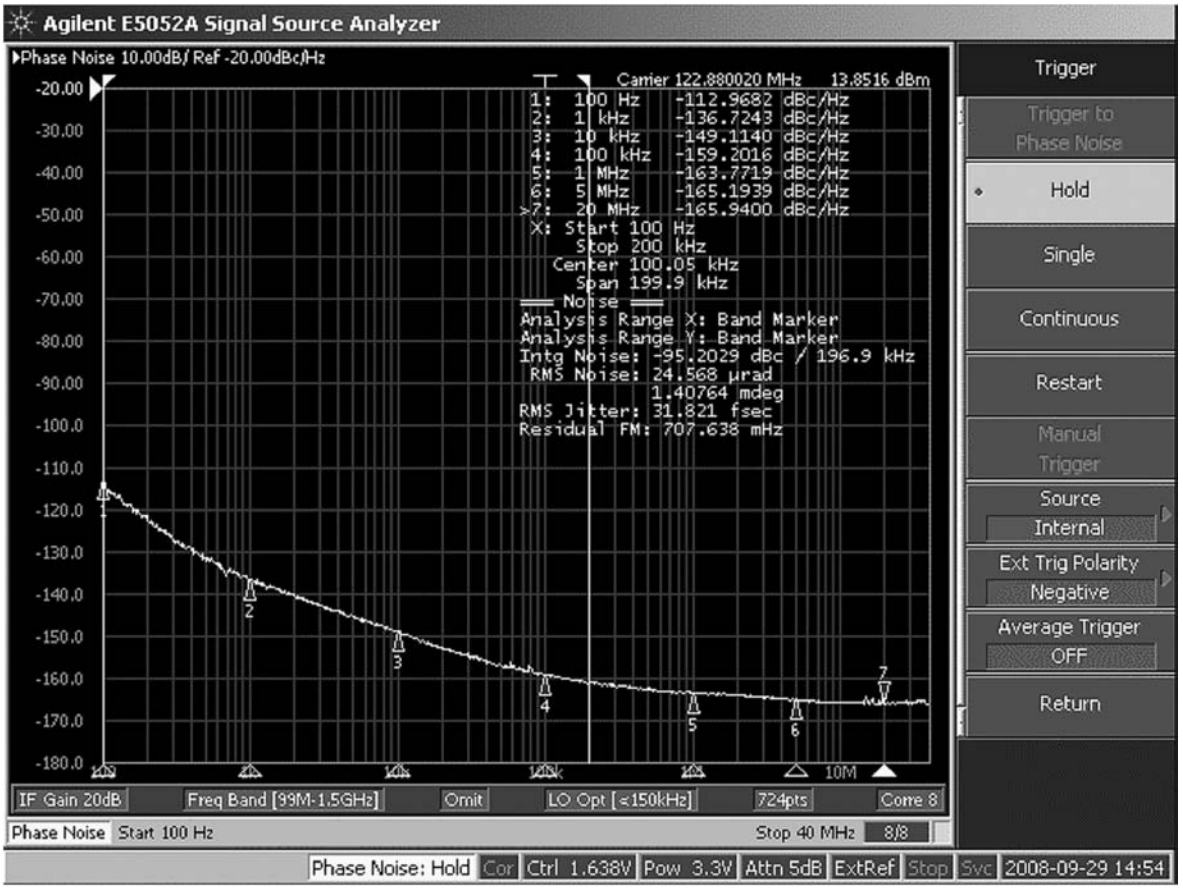

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FIGURE 10. Crystek CVHD-950-122.88 VCXO Open Loop Phase Noise

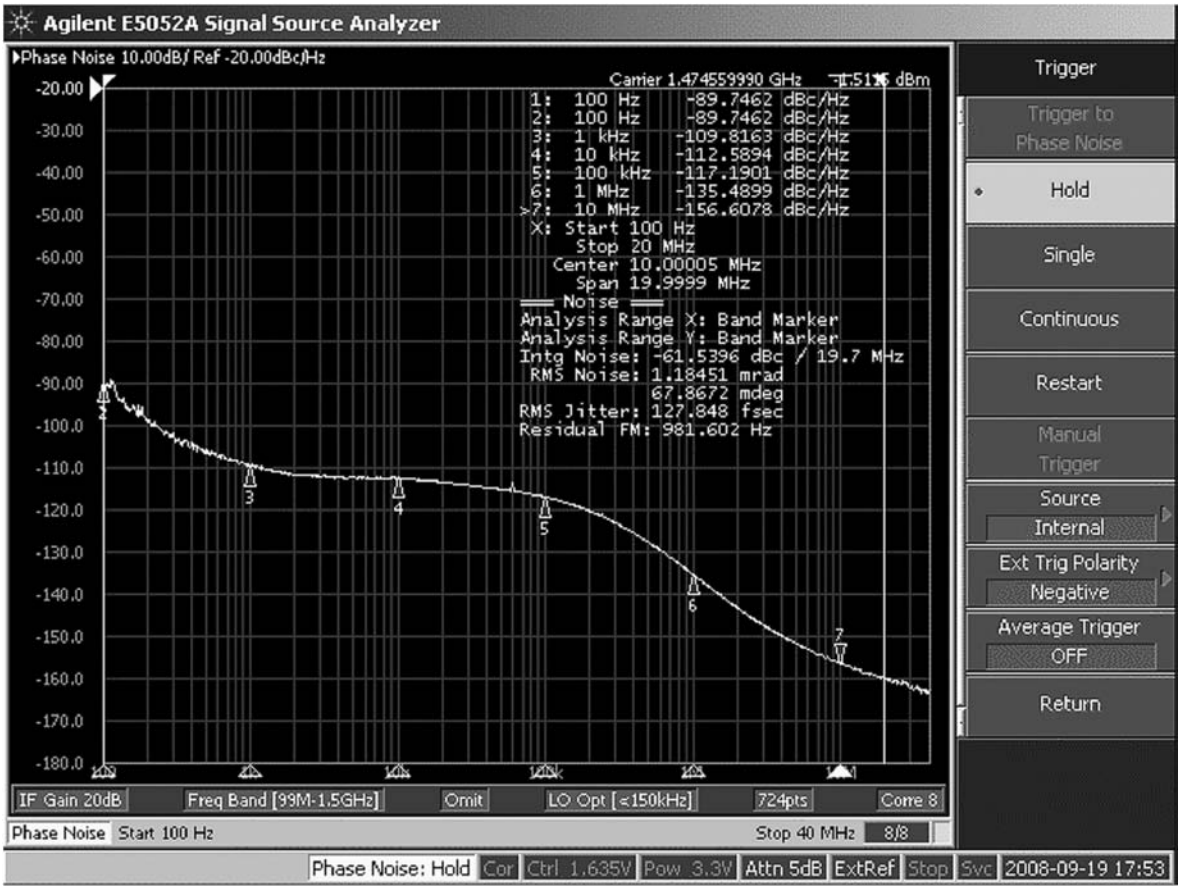

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FIGURE 11. LMK04031 Fout Phase Noise, Crystek CVHD-950-122.88 VCXO

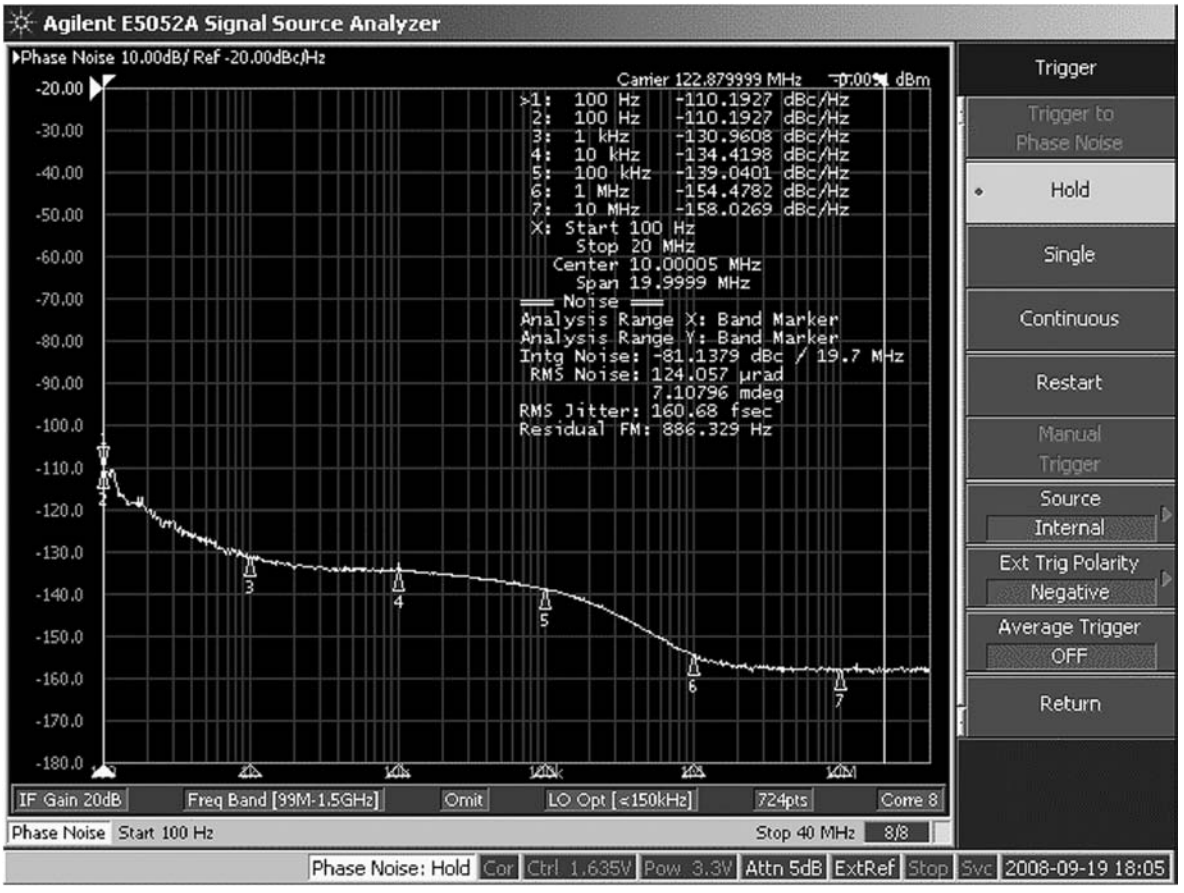

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FIGURE 12. LMK04031 LVDS Phase Noise, Crystek CVHD-950-122.88 VCXO

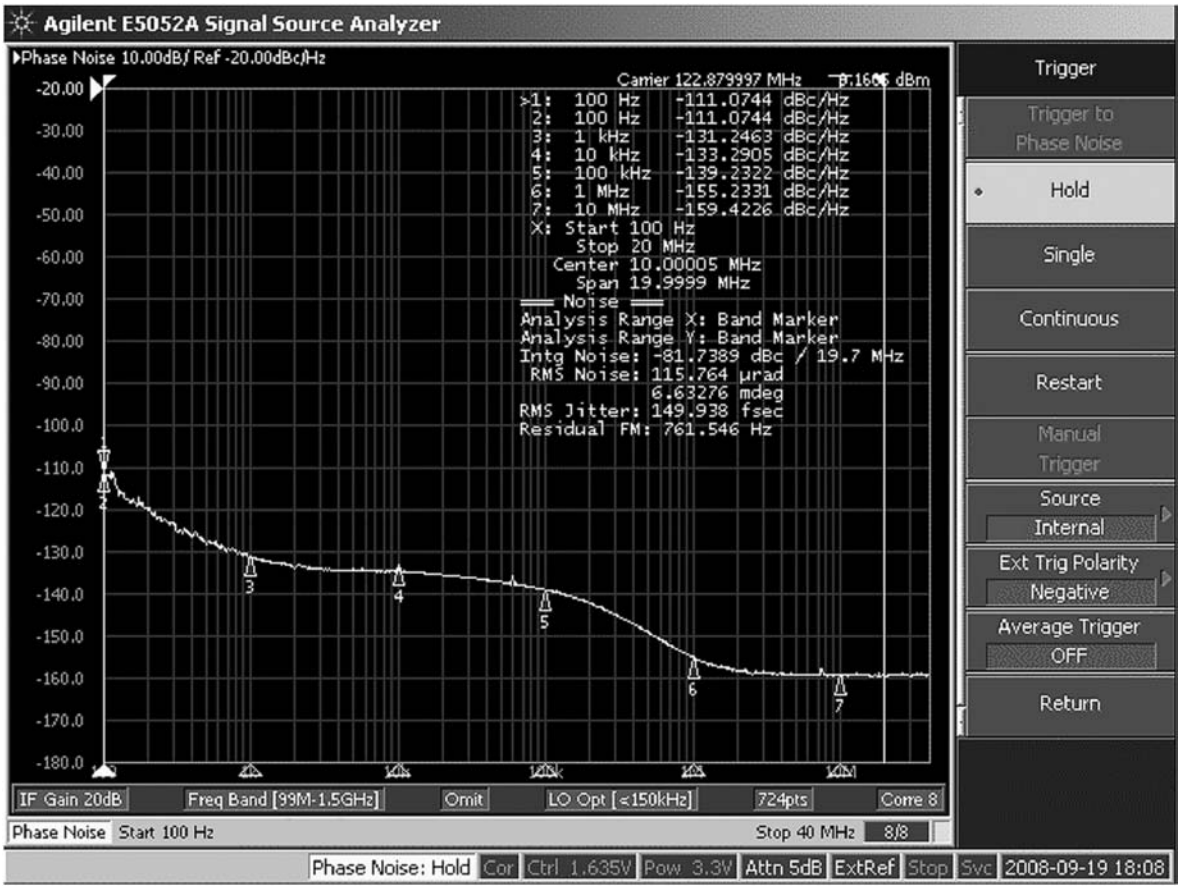

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FIGURE 13. LMK04031 LVCMOS Phase Noise, Crystek CVHD-950-122.88 VCXO

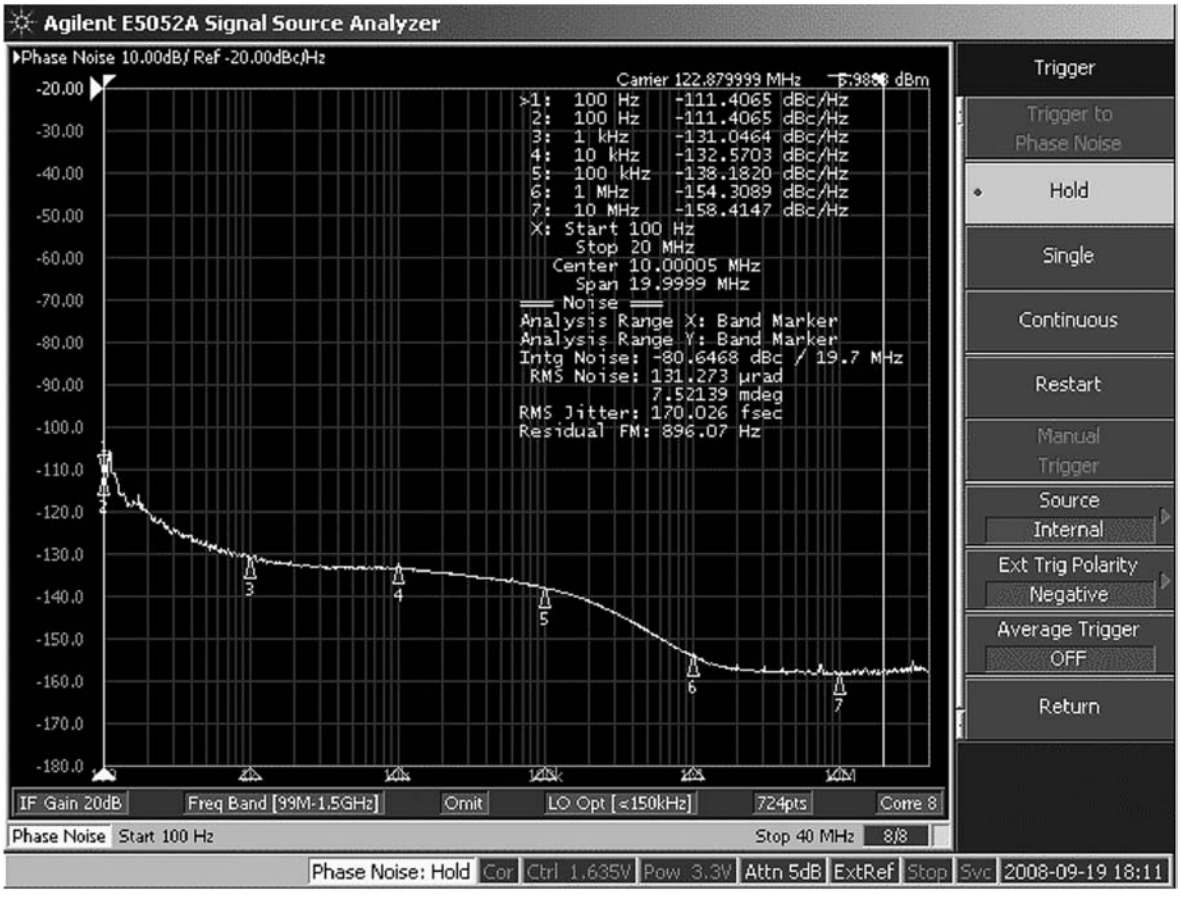

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FIGURE 14. LMK04031 LVPECL Phase Noise, Crystek CVHD-950-122.88 VCXO

TABLE 5. Crystek CVHD-950-80

Reference Clock (MHz)	F_{comp1} (MHz)	PLL1 Loop BW (Hz)	F_{comp2} (MHz)	PLL2 Loop BW (kHz)
40	1.0	20	40	120.3

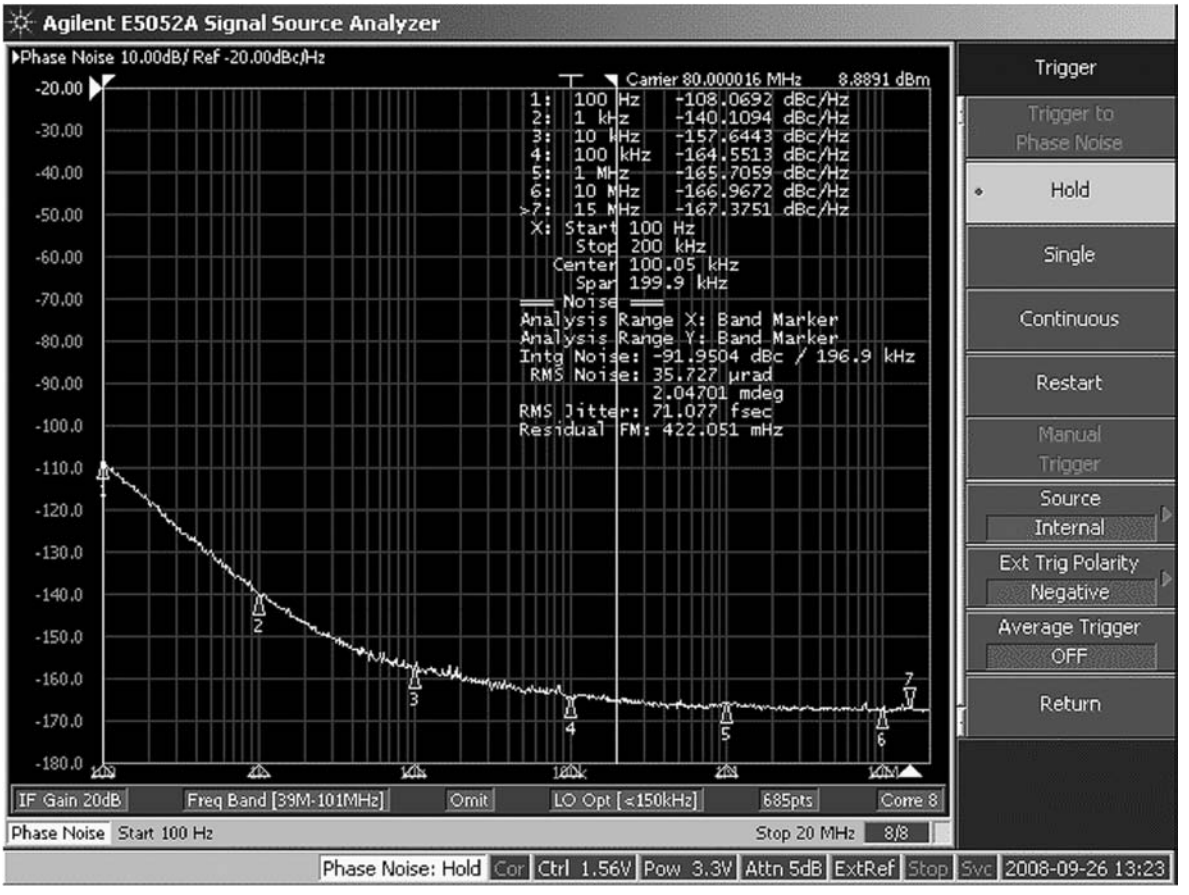

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FIGURE 15. Crystek CVHD-950-80 VCXO Open Loop Phase Noise

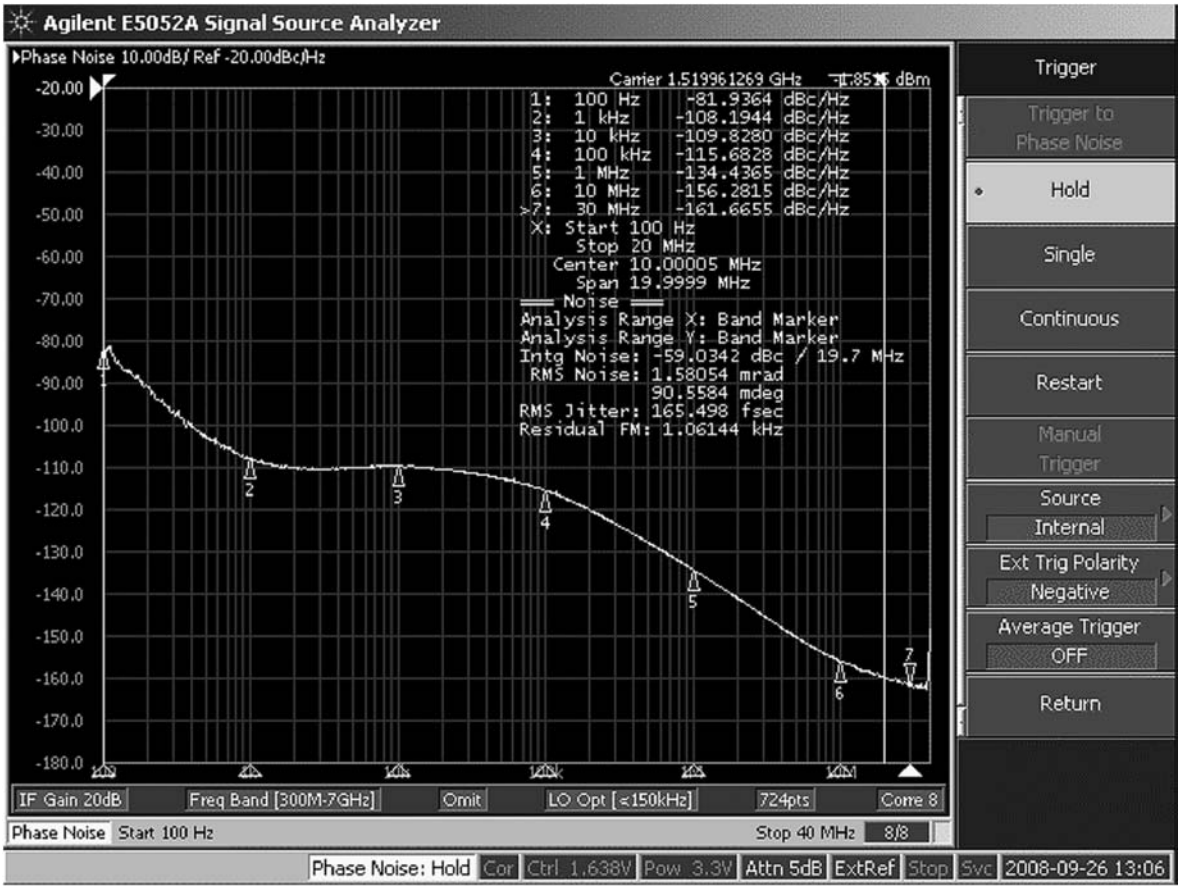

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FIGURE 16. LMK04031 Fout Phase Noise, Crystek CVHD-950-80 VCXO

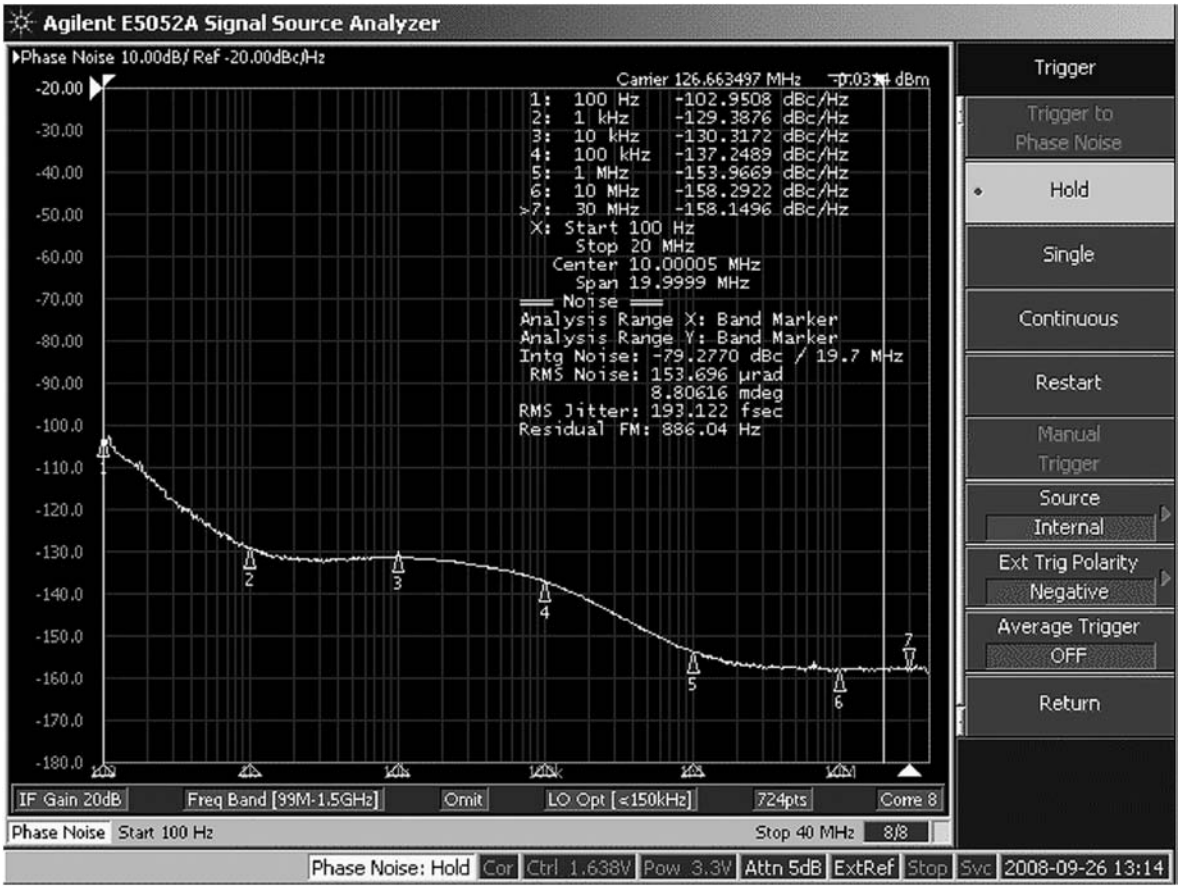

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FIGURE 17. LMK04031 LVDS Phase Noise, Crystek CVHD-950-80 VCXO

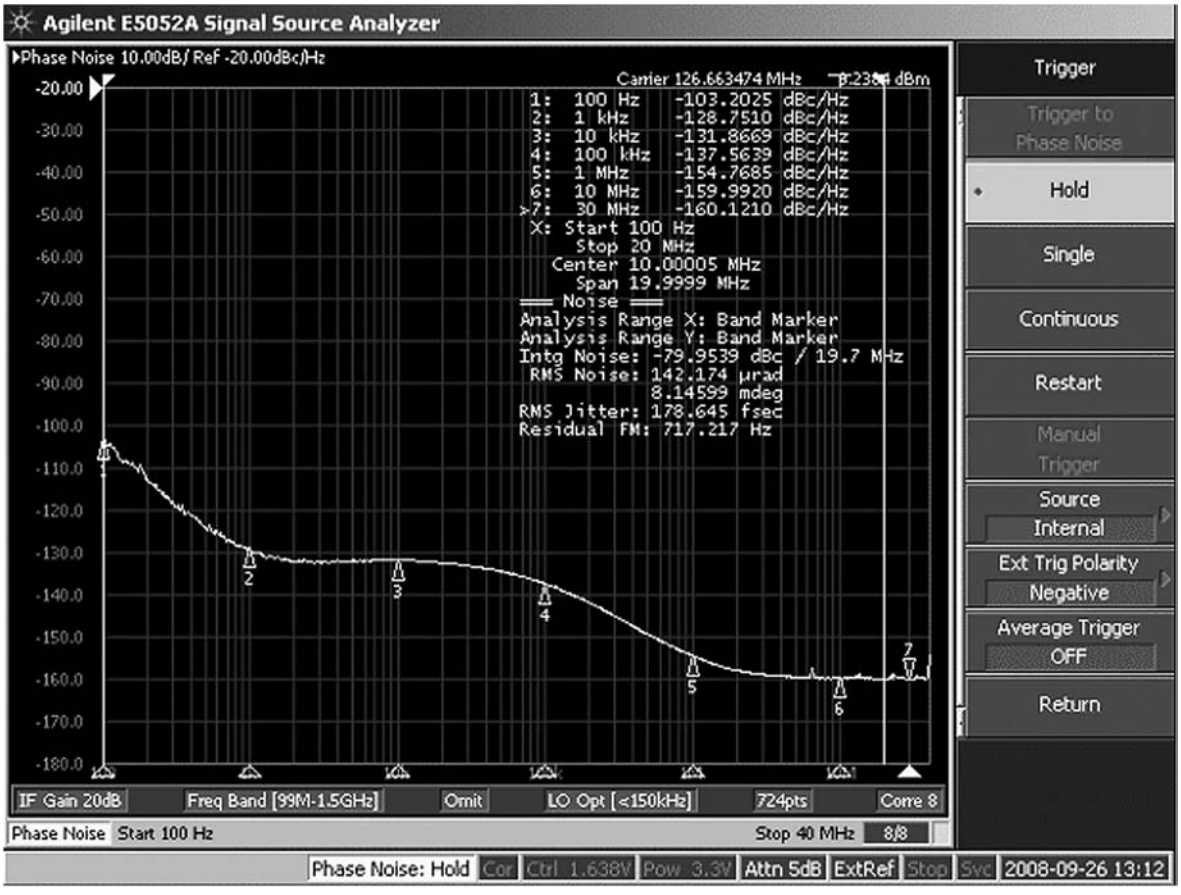

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FIGURE 18. LMK04031 LVCMOS Phase Noise, Crystek CVHD-950-80 VCXO

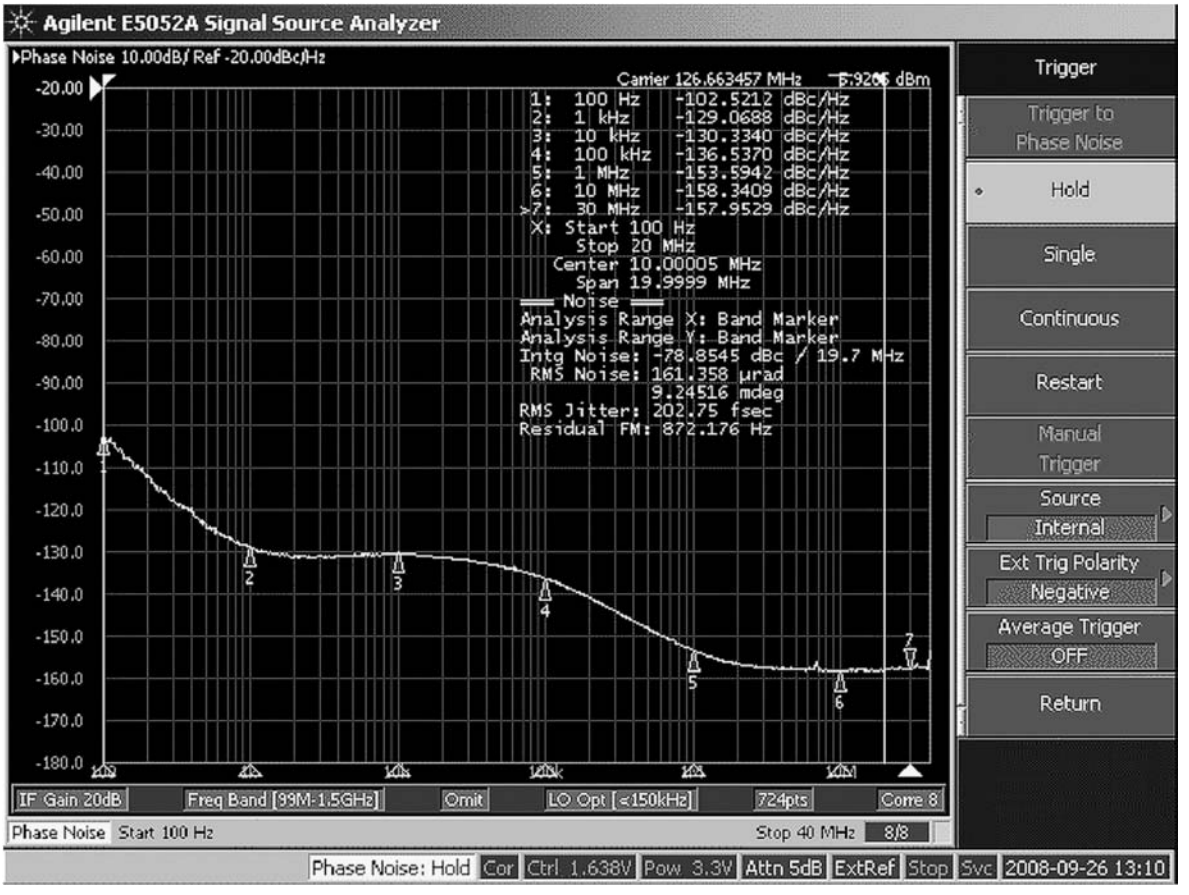

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FIGURE 19. LMK04031 LVPECL Phase Noise, Crystek CVHD-950-80 VCXO

TABLE 6. Crystek CVPD-920-61.44

Reference Clock (MHz)	F_{comp1} (MHz)	PLL1 Loop BW (Hz)	F_{comp2} (MHz)	PLL2 Loop BW (kHz)
30.72	1.024	20	30.72	95.4

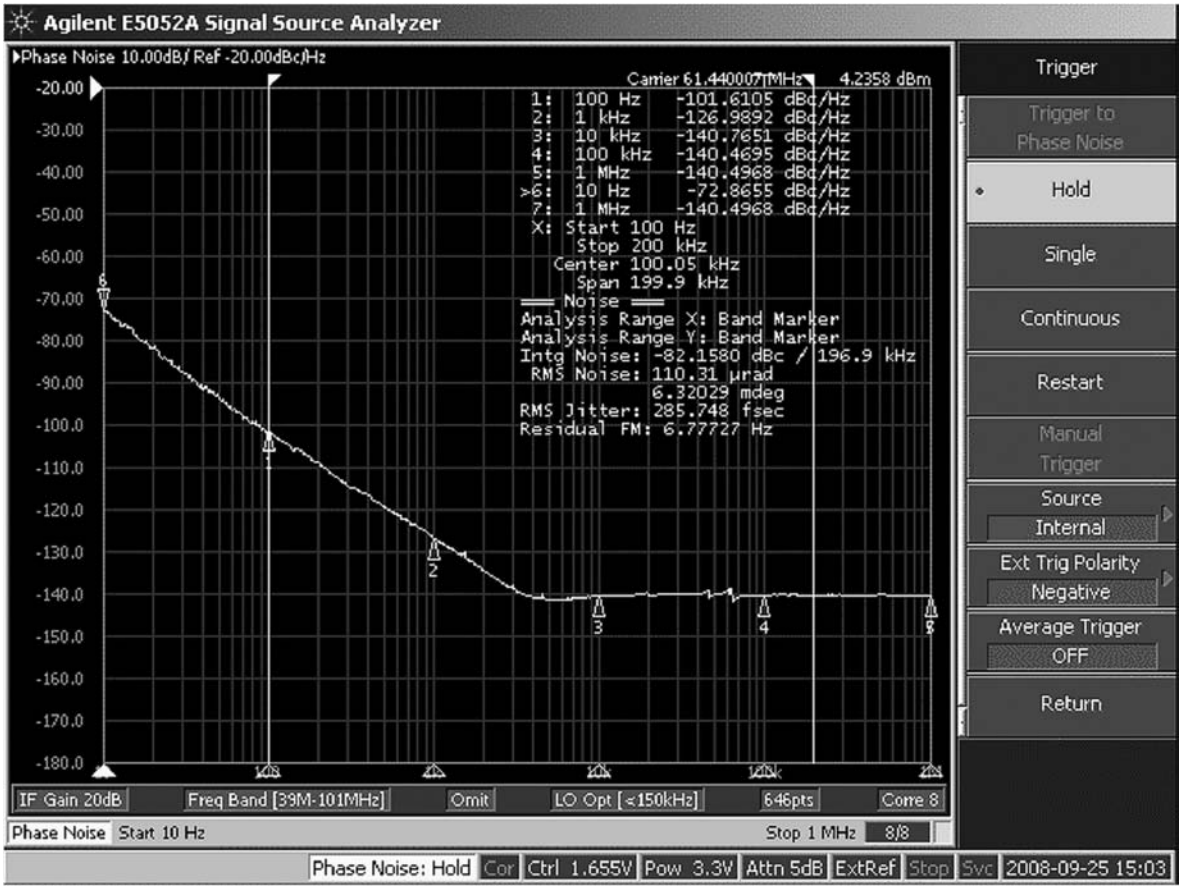

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FIGURE 20. Crystek CVPD-920-61.44 VCXO Open Loop Phase Noise

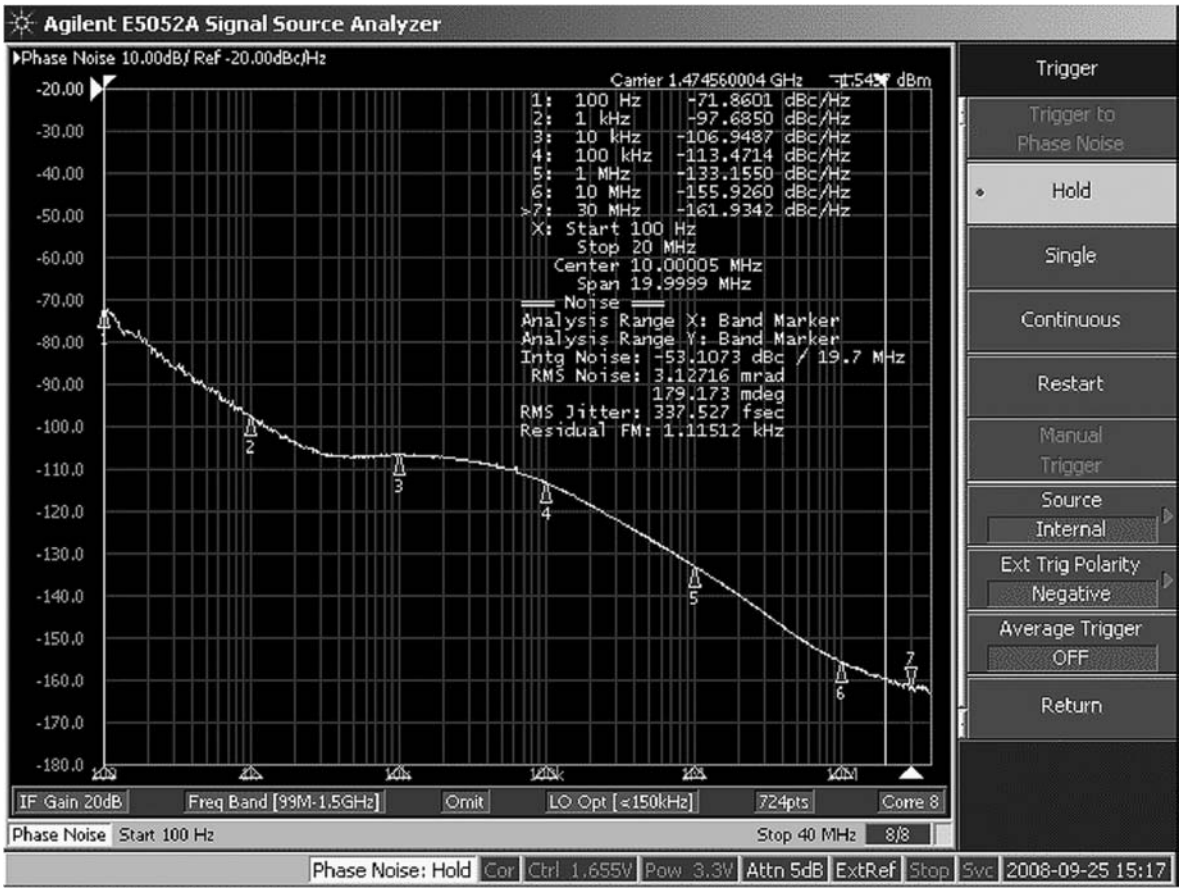

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FIGURE 21. LMK04031 Fout Phase Noise, Crystek CVPD-920-61.44 VCXO

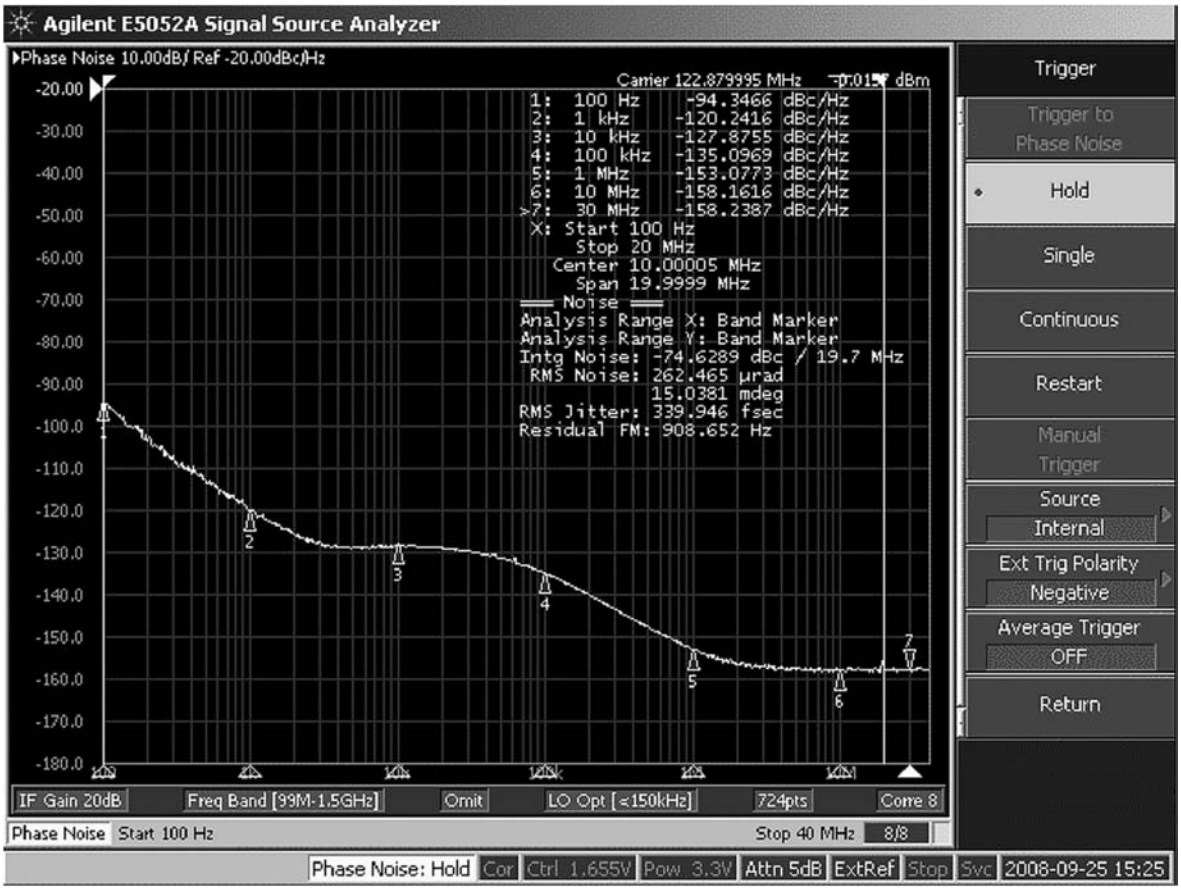

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FIGURE 22. LMK04031 LVDS Phase Noise, Crystek CVPD-920-61.44 VCXO

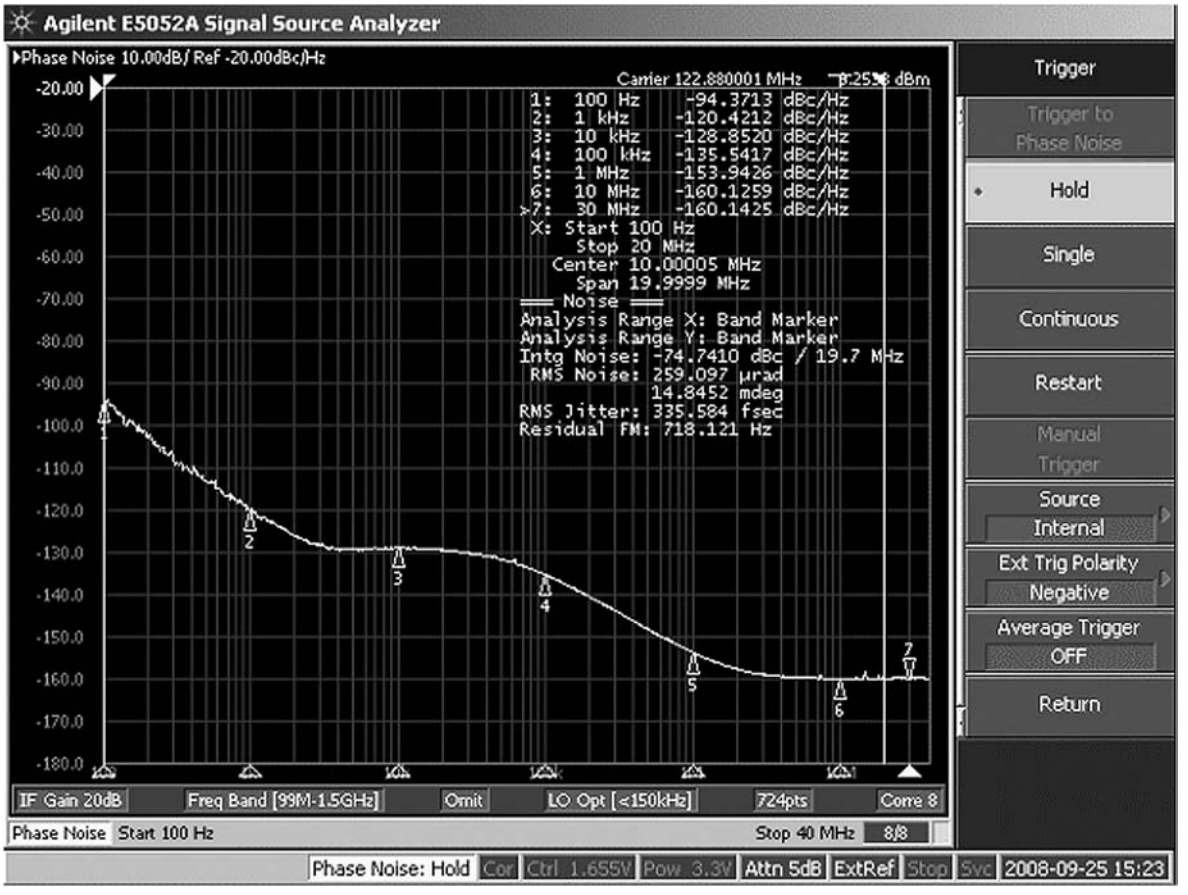

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FIGURE 23. LMK04031 LVCMOS Phase Noise, Crystek CVPD-920-61.44 VCXO

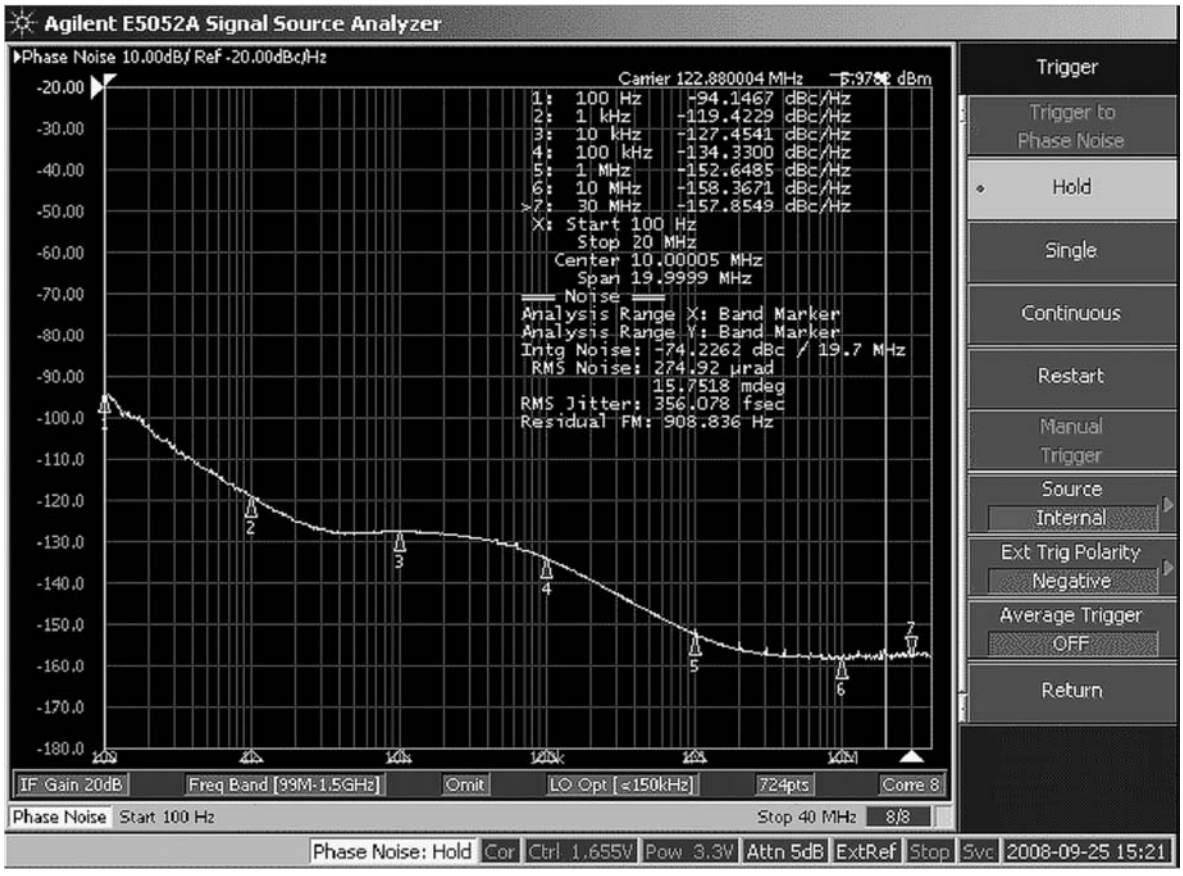

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FIGURE 24. LMK04031 LVPECL Phase Noise, Crystek CVPD-920-61.44 VCXO

TABLE 7. Epson Toyocom VG-4501, 61.44 MHz

Reference Clock (MHz)	F_{comp1} (MHz)	PLL1 Loop BW (Hz)	F_{comp2} (MHz)	PLL2 Loop BW (kHz)
30.72	1.024	20	30.72	95.4

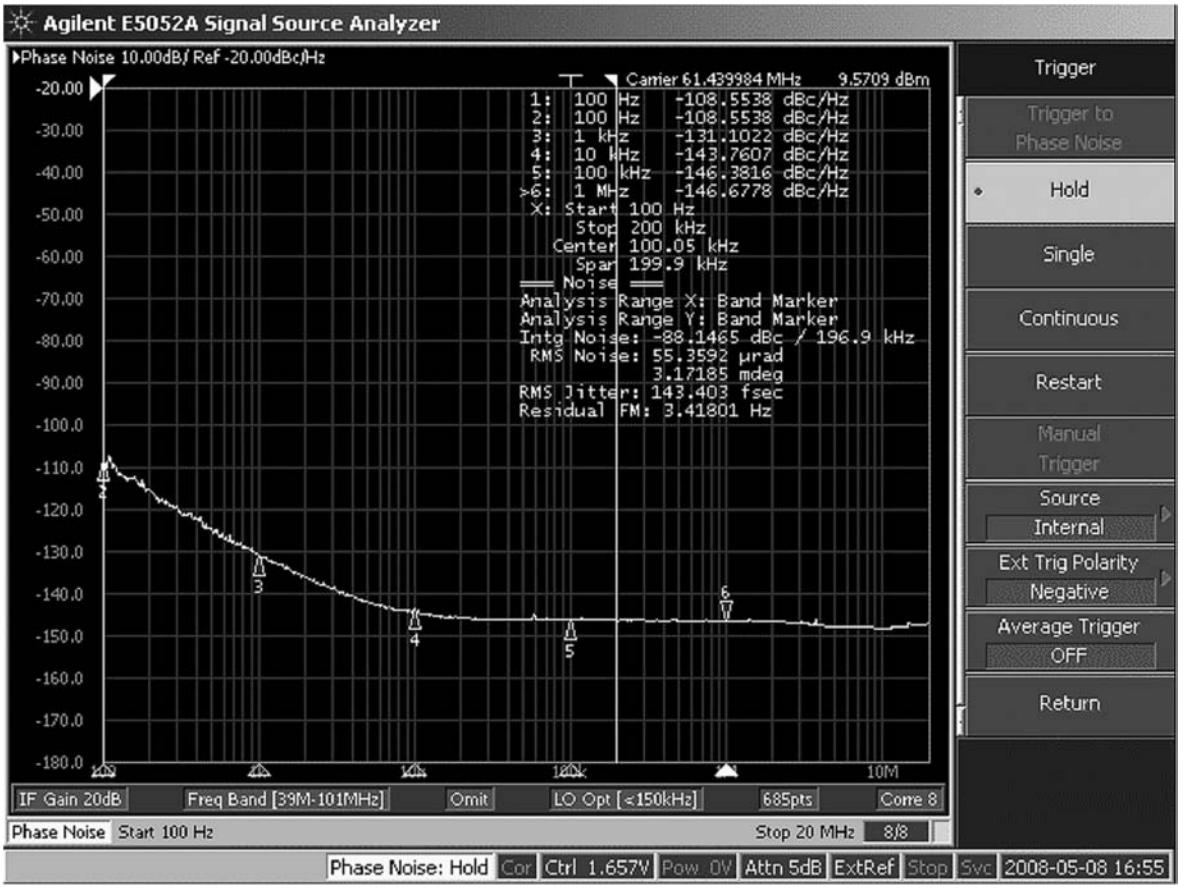

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FIGURE 25. Epson Toyocom VG-4501 VCXO, 61.44 MHz, Open Loop Phase Noise

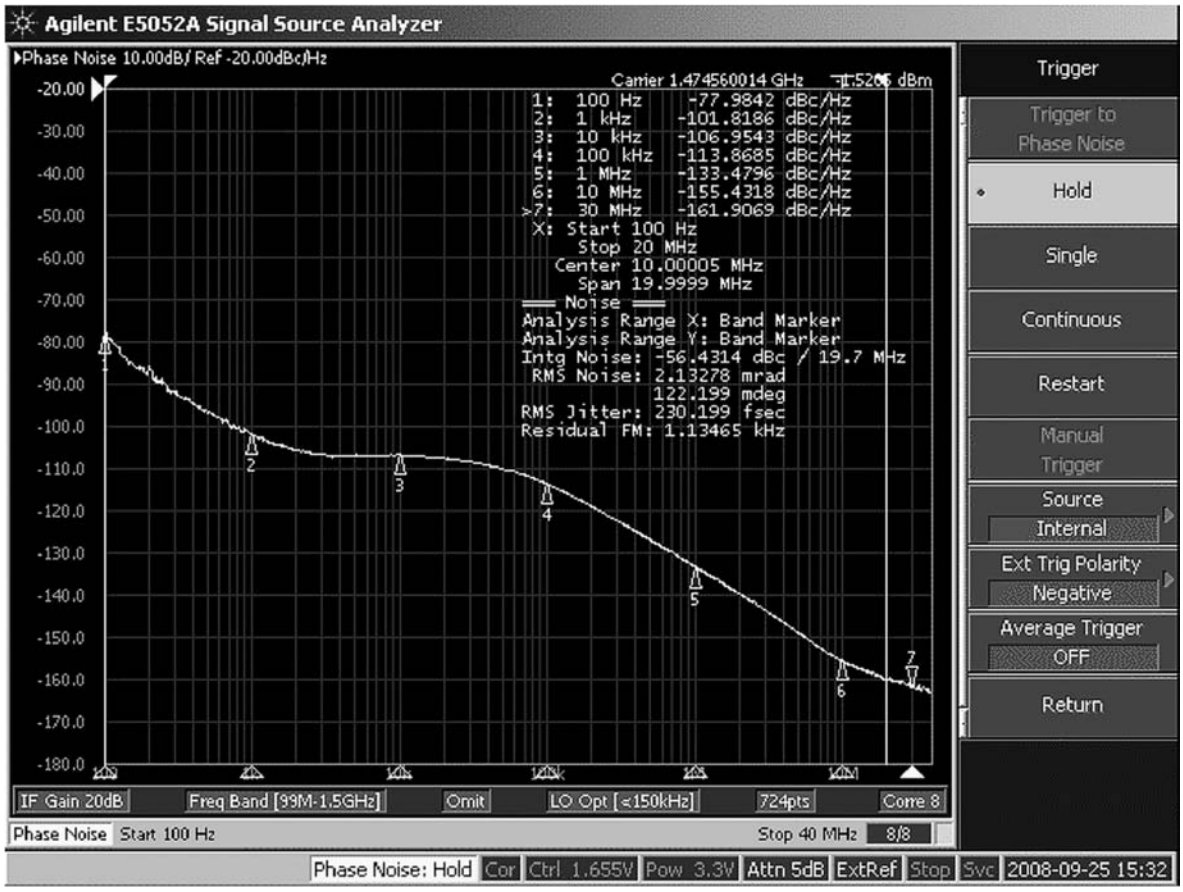

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FIGURE 26. LMK04031 Fout Phase Noise, Epson Toyocom VG-4501 VCXO

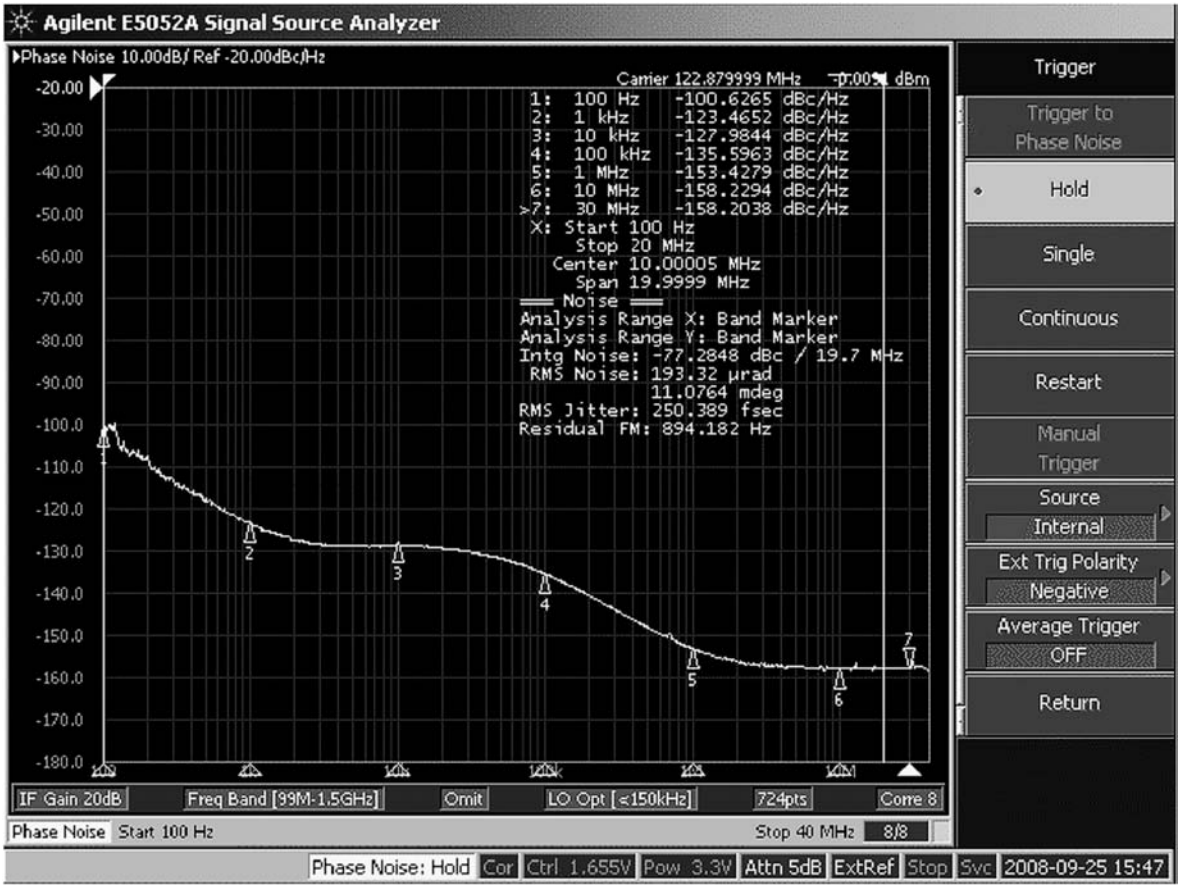

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FIGURE 27. LMK04031 LVDS Phase Noise, Epson Toyocom VG-4501 VCXO

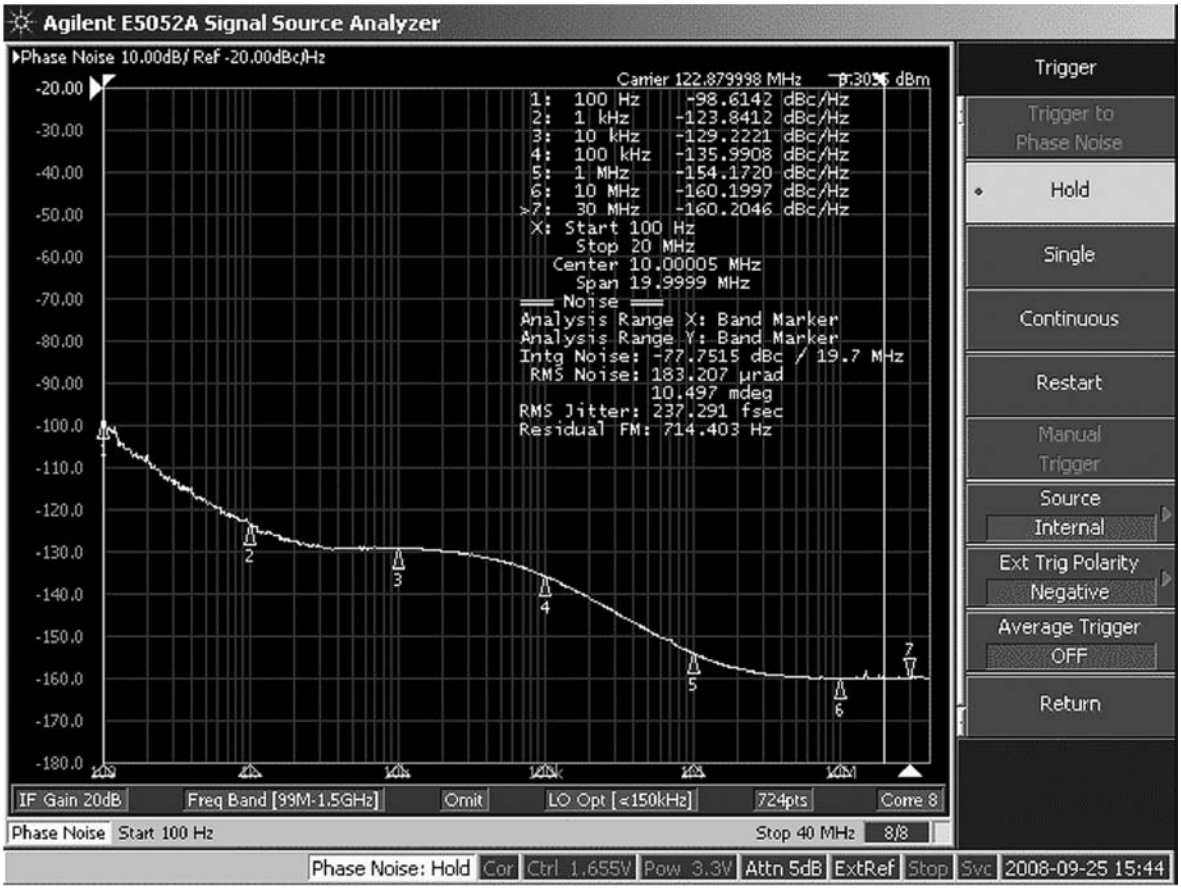

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FIGURE 28. LMK04031 LVCMOS Phase Noise, Epson Toyocom VG-4501 VCXO

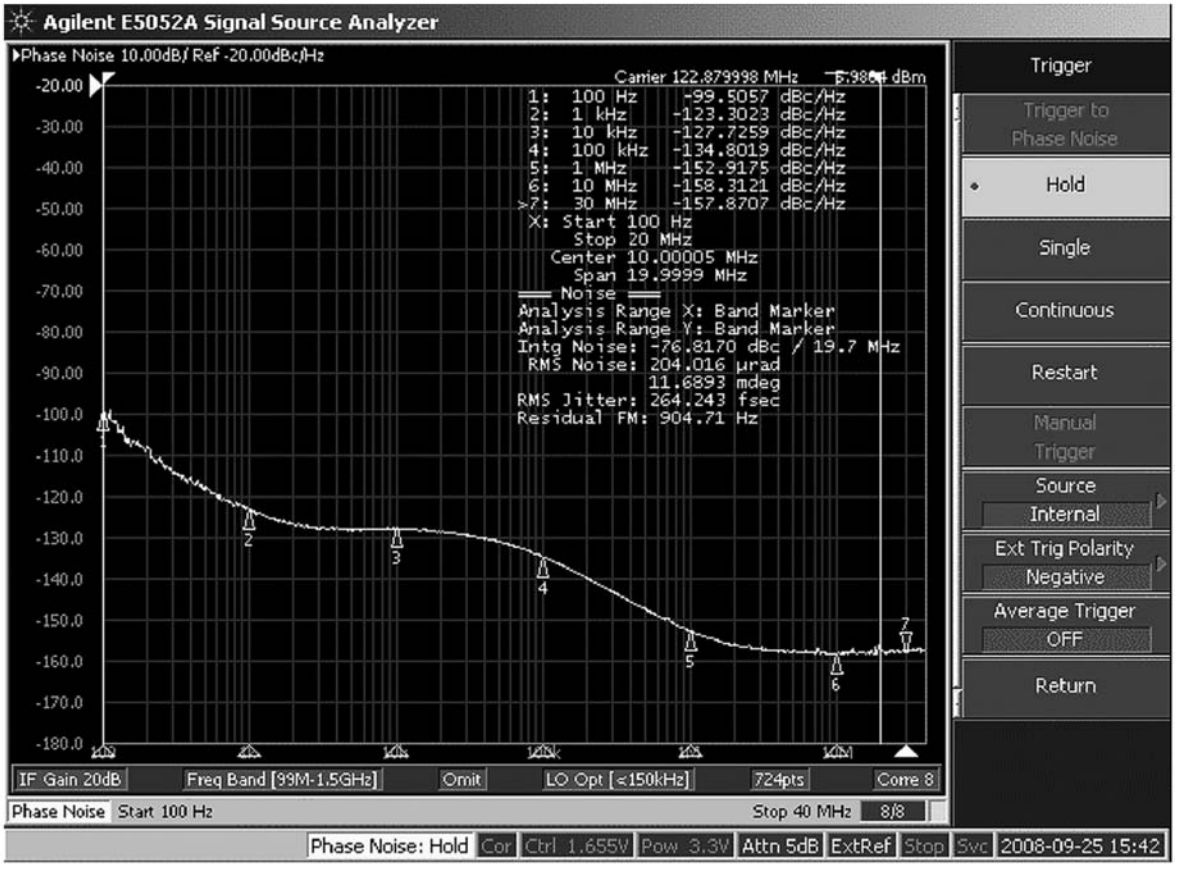

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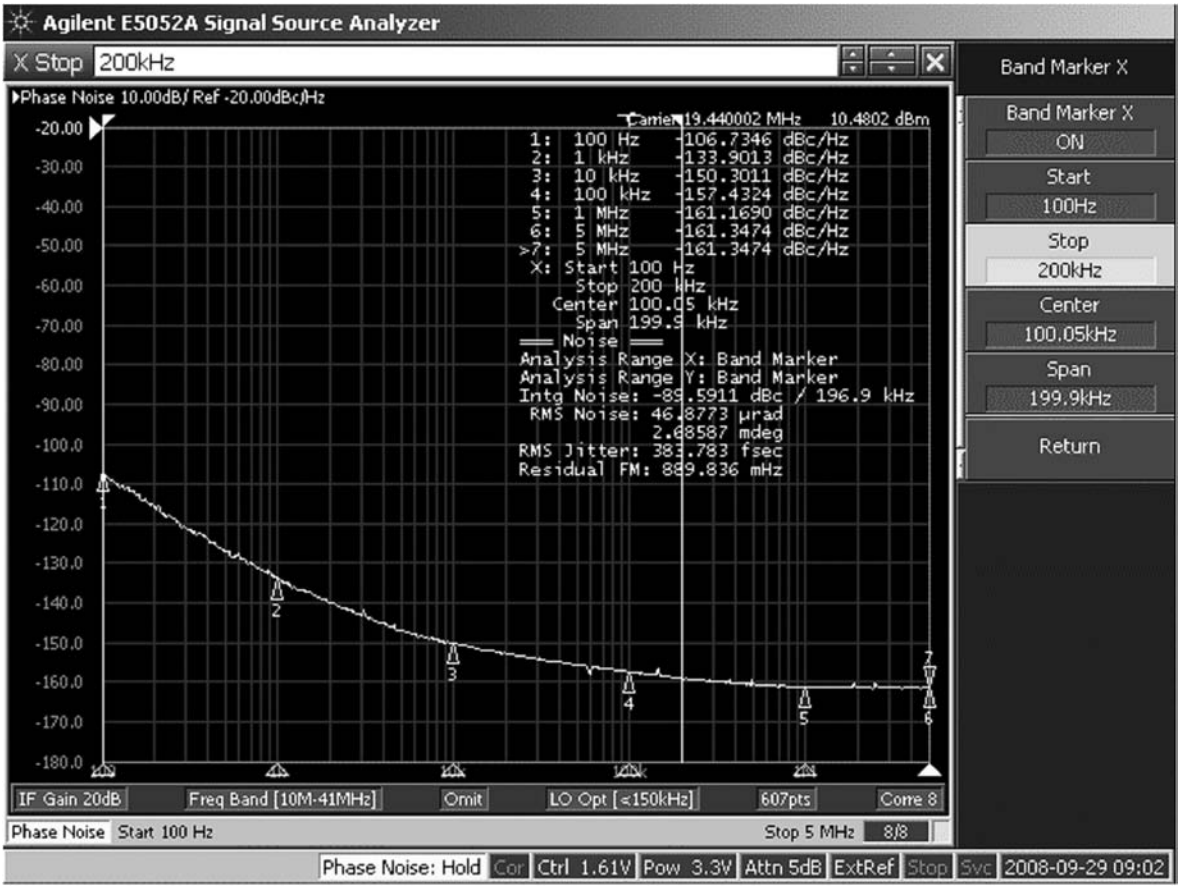
FIGURE 29. LMK04031 LVPECL Phase Noise, Epson Toyocom VG-4501 VCXO

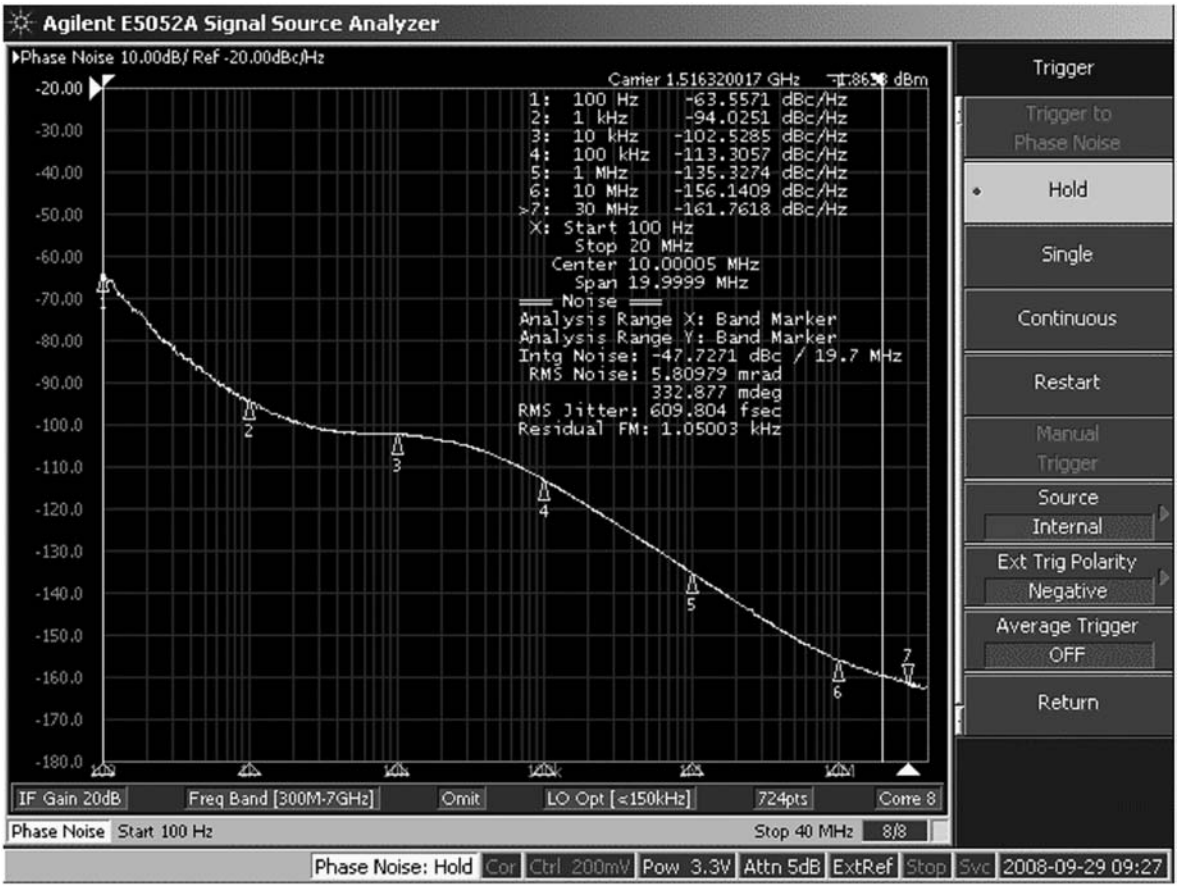
TABLE 8. Epson-Toyocom VG-4231, 19.44 MHz

Reference Clock (MHz)	F_{comp1} (MHz)	PLL1 Loop BW (Hz)	F_{comp2} (MHz)	PLL2 Loop BW (kHz)
19.44	1.08	20	19.44	59



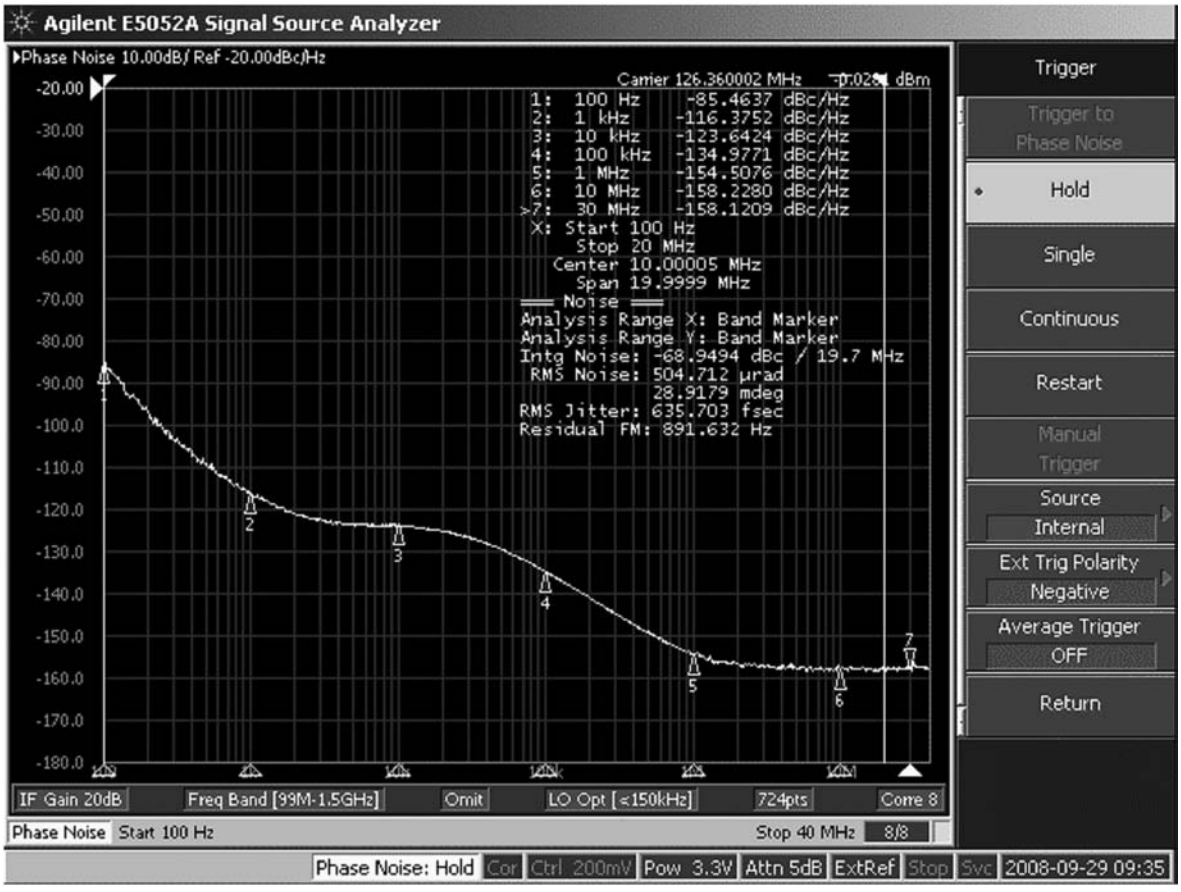
30082830

FIGURE 30. Epson Toyocom VG-4231 VCXO, 19.44 MHz, Open Loop Phase Noise



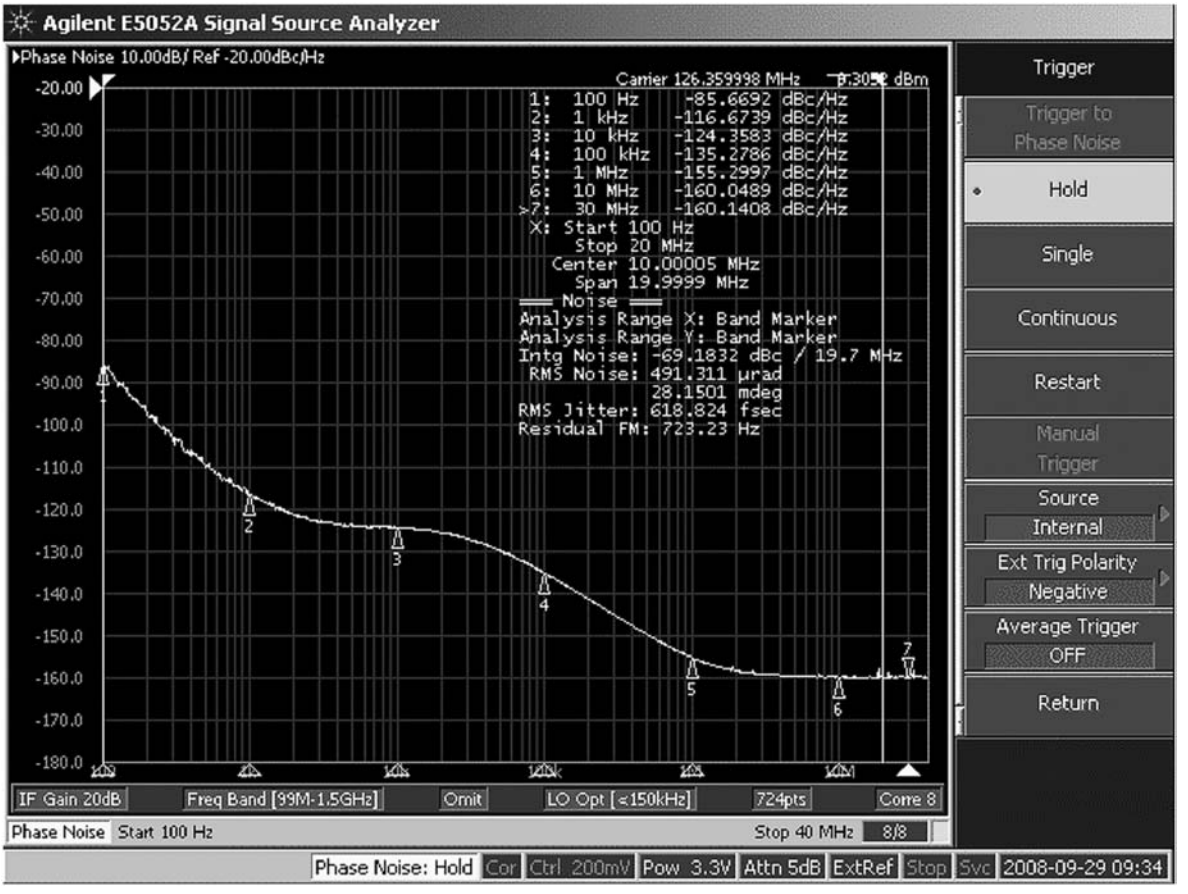
30082831

FIGURE 31. LMK04031 Fout Phase Noise, Epson Toyocom VG-4231 VCXO



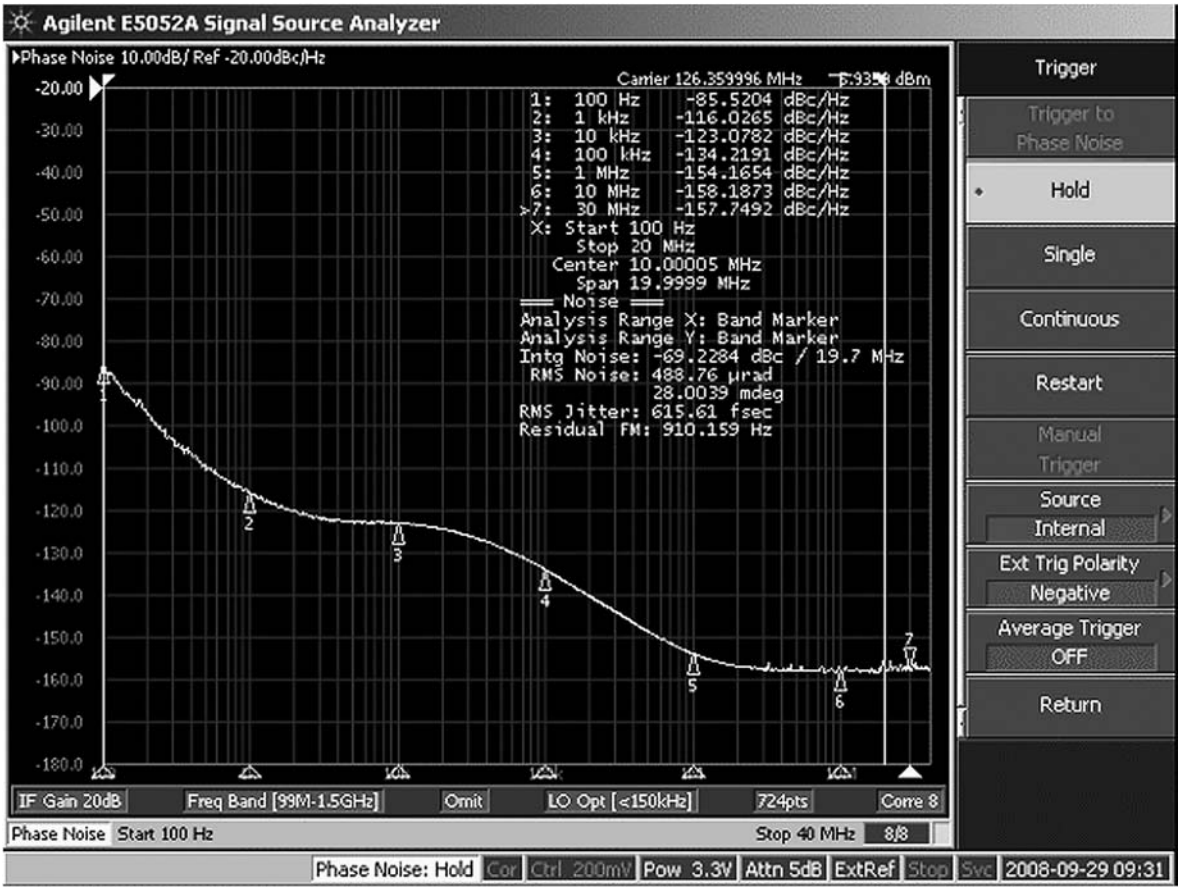
30082832

FIGURE 32. LMK04031 LVDS Phase Noise, Epson Toyocom VG-4231 VCXO



30082833

FIGURE 33. LMK04031 LVCMOS Phase Noise, Epson Toyocom VG-4231 VCXO

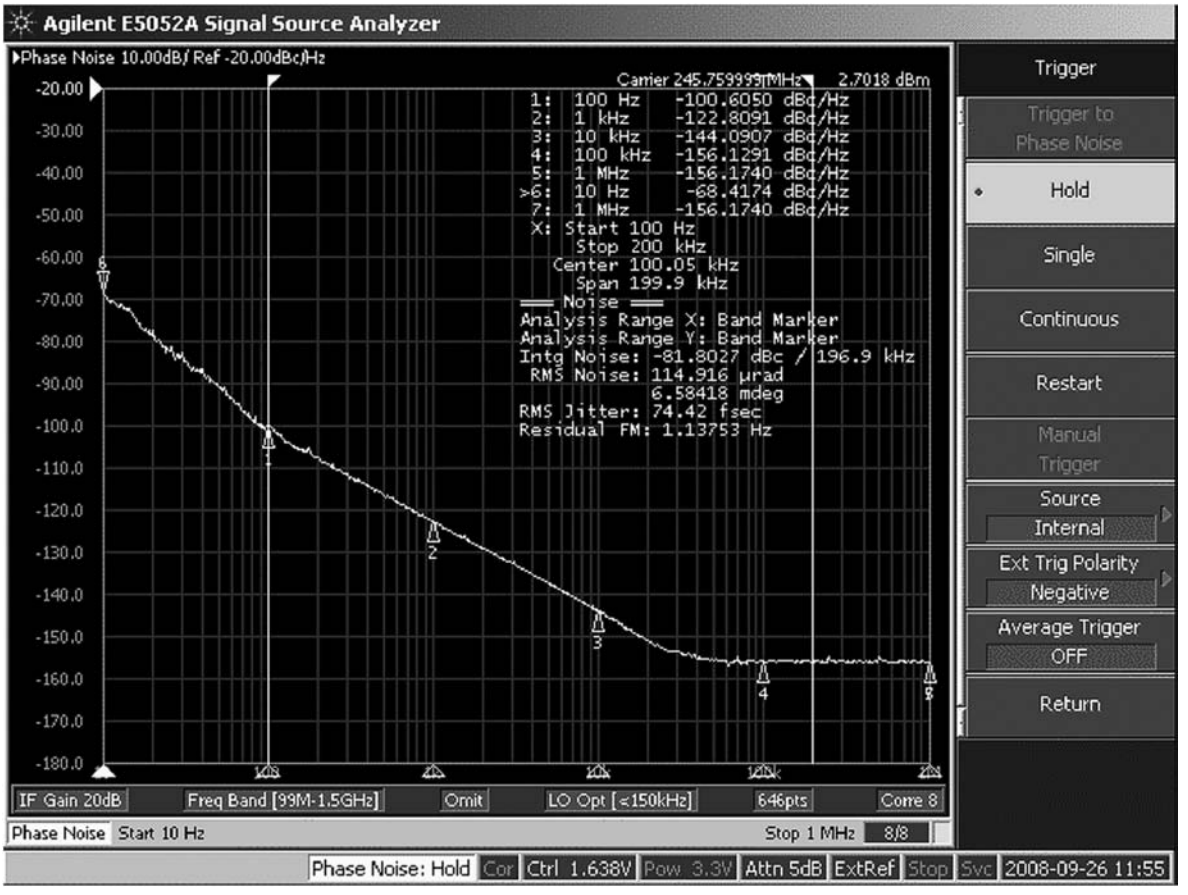


30082834

FIGURE 34. LMK04031 LVPECL Phase Noise, Epson Toyocom VG-4231 VCXO

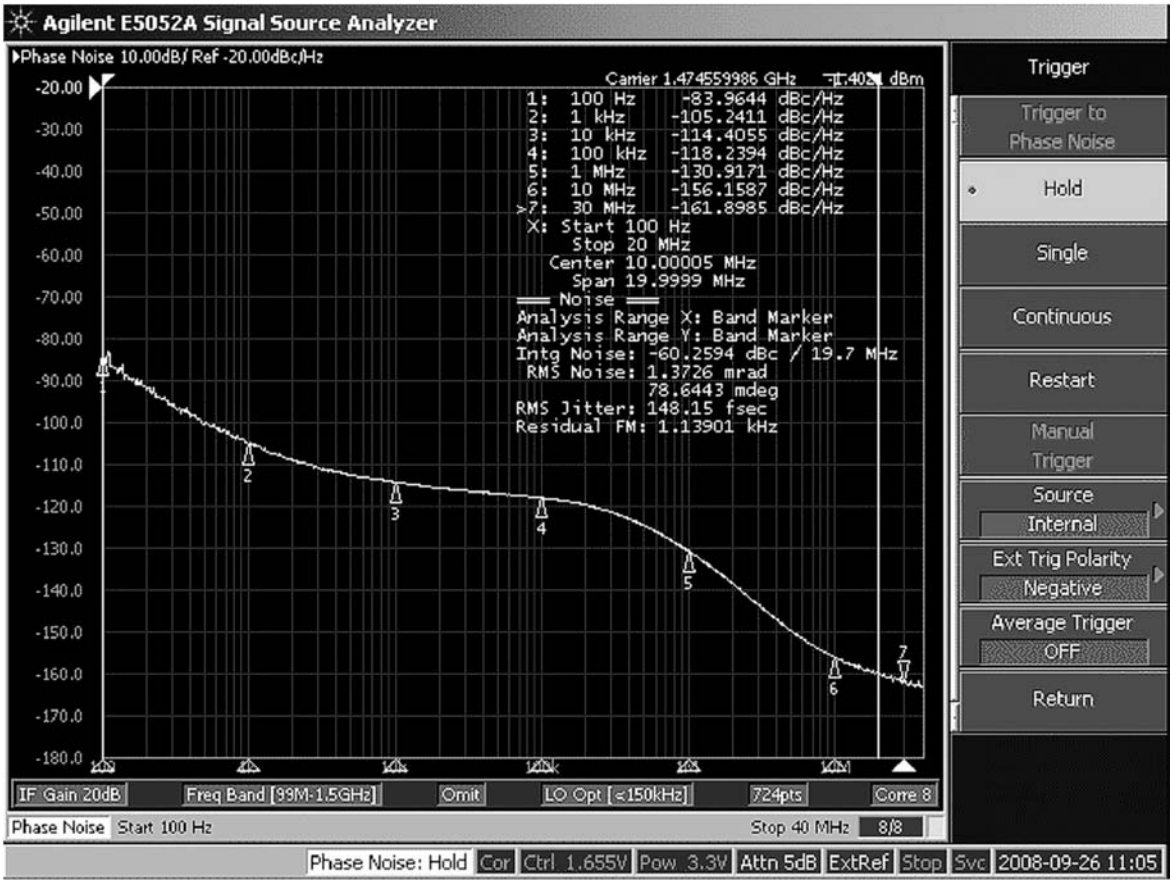
TABLE 9. Epson-Toyocom TCO-2111-A 245.76

Reference Clock (MHz)	F_{comp1} (MHz)	PLL1 Loop BW (Hz)	F_{comp2} (MHz)	PLL2 Loop BW (kHz)
122.88	1.024	20	61.44	189.7



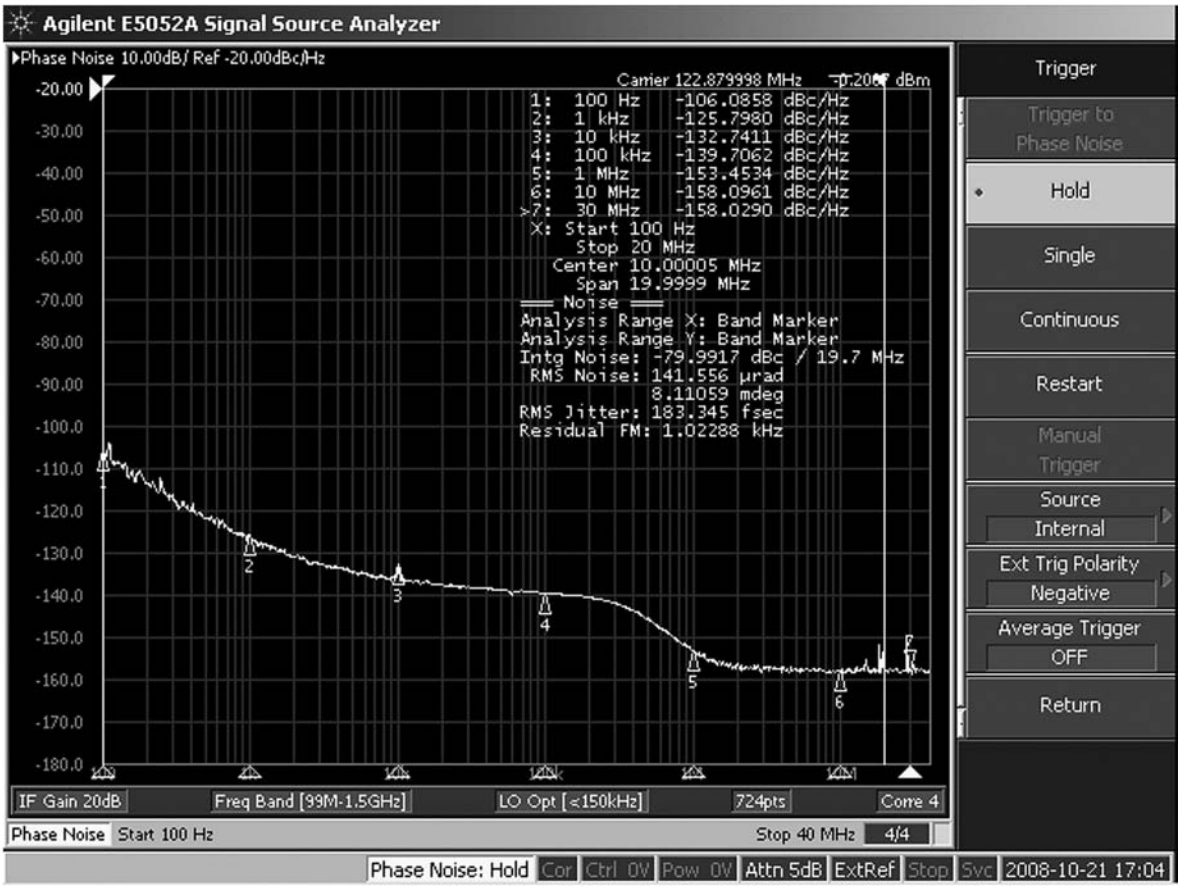
30082835

FIGURE 35. Epson Toyocom TCO-2111-AA VCXO, 245.76 MHz, Open Loop Phase Noise



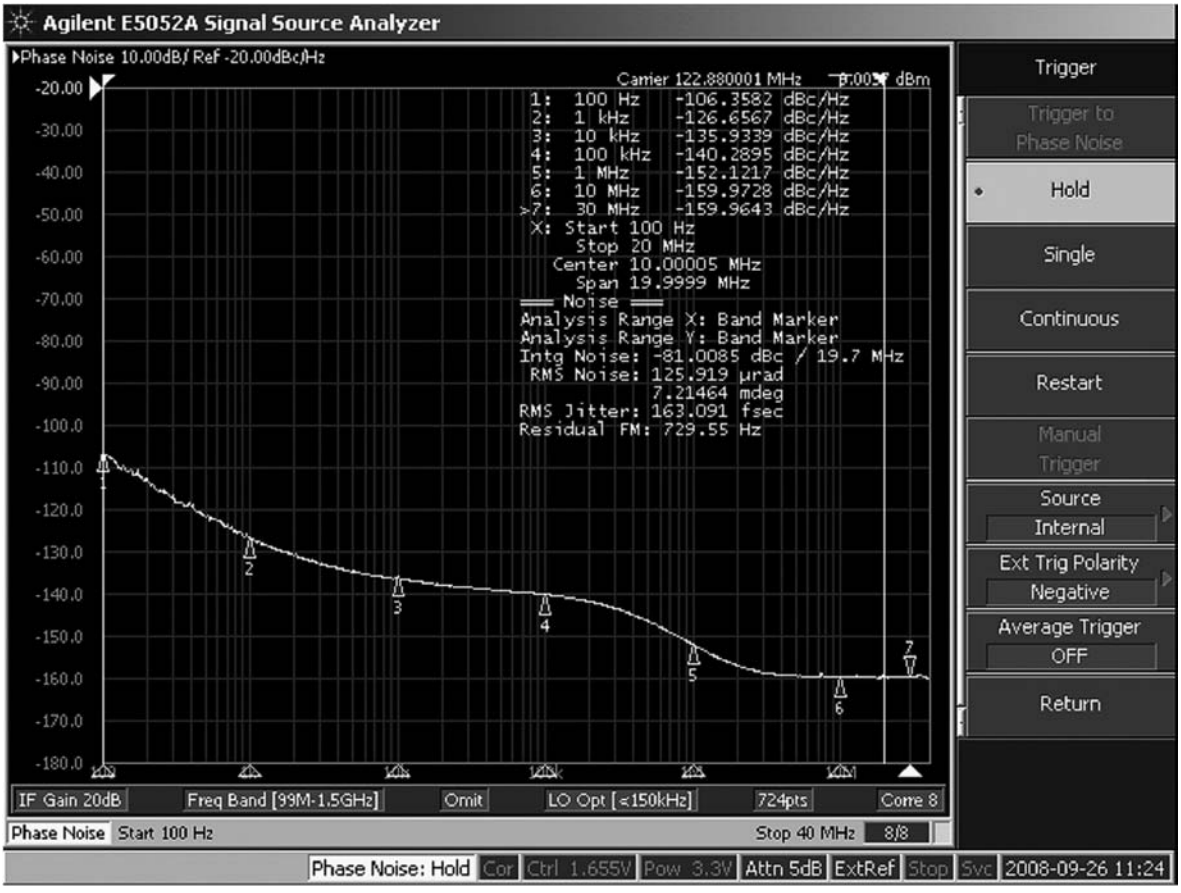
30082836

FIGURE 36. LMK04031 Fout Phase Noise, Epson Toyocom TCO-2111-AA VCXO



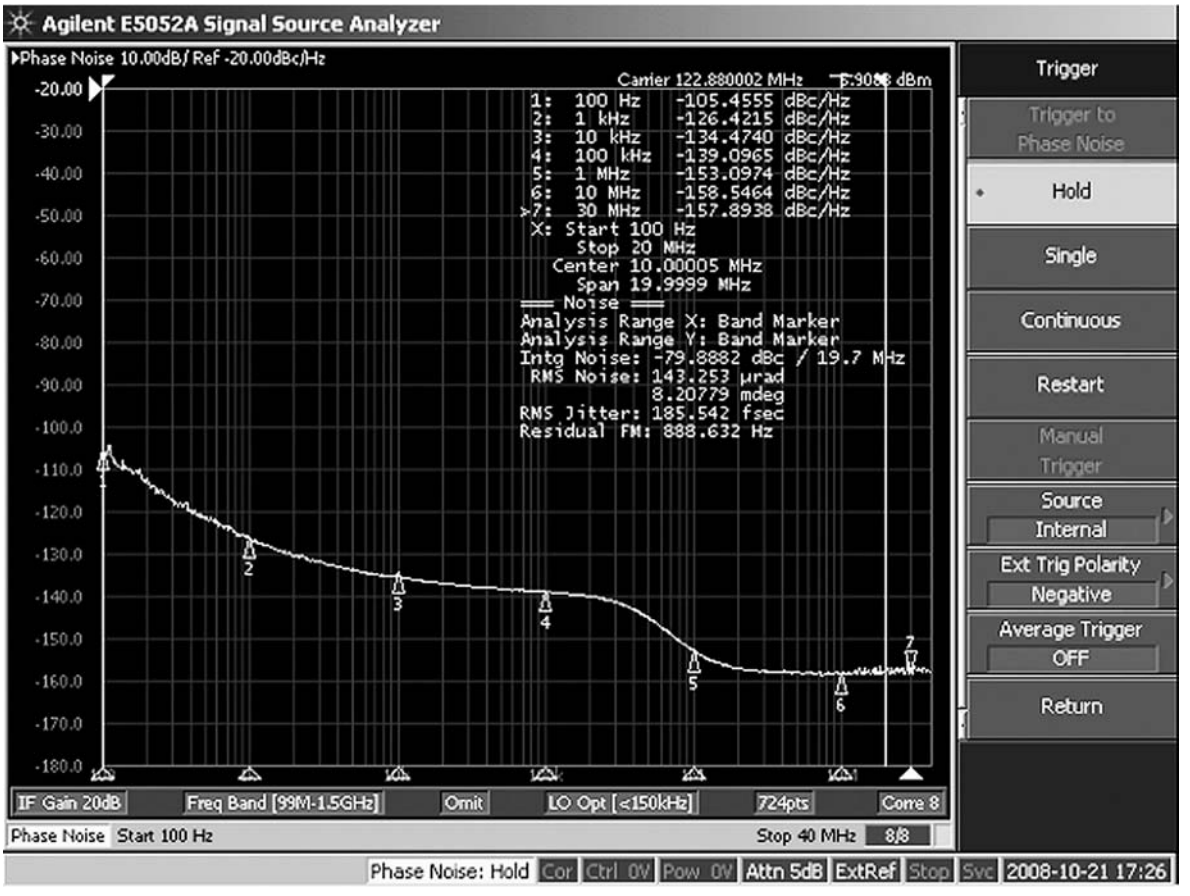
30082863

FIGURE 37. LMK04031 LVDS Phase Noise, Epson Toyocom TCO-2111-AA VCXO



30082864

FIGURE 38. LMK04031 LVCMOS Phase Noise, Epson Toyocom TCO-2111-AA VCXO

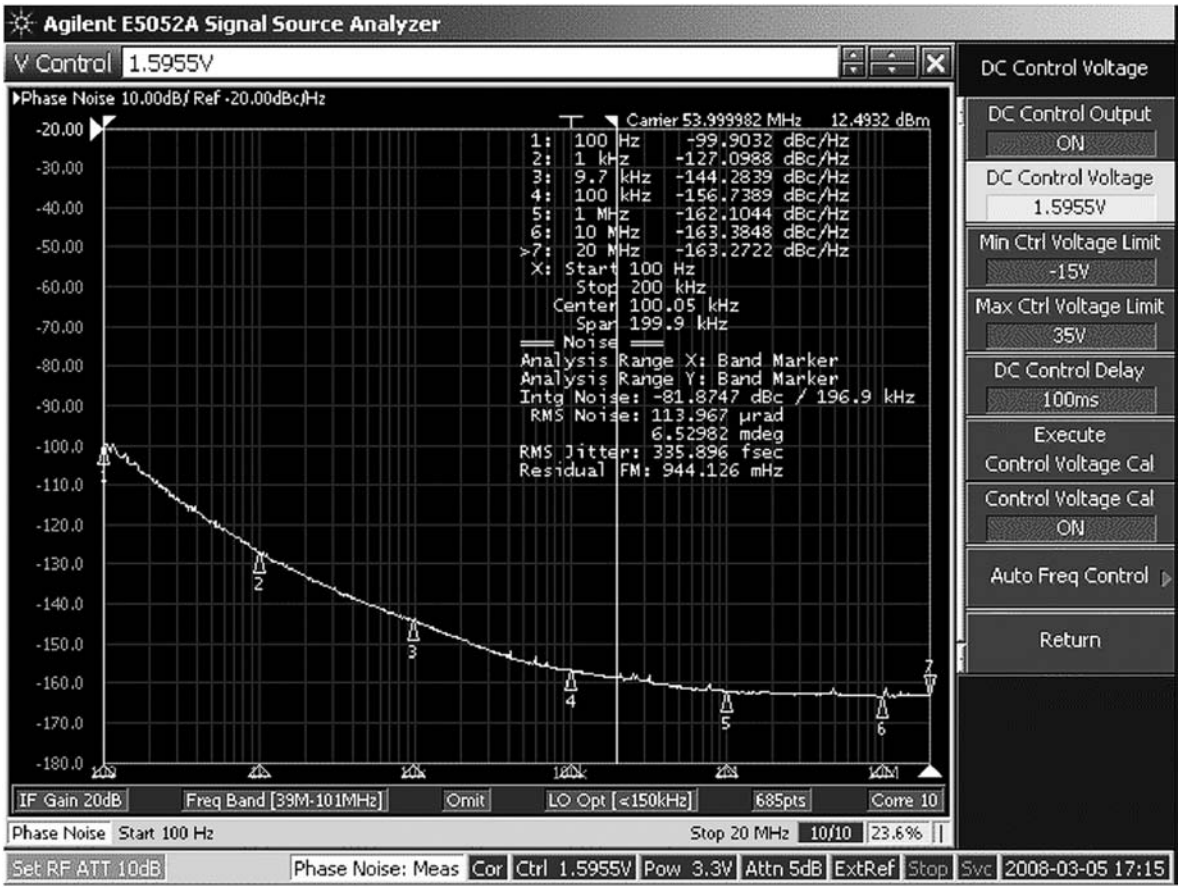


30082865

FIGURE 39. LMK04031 LVPECL Phase Noise, Epson Toyocom TCO-2111-AA VCXO

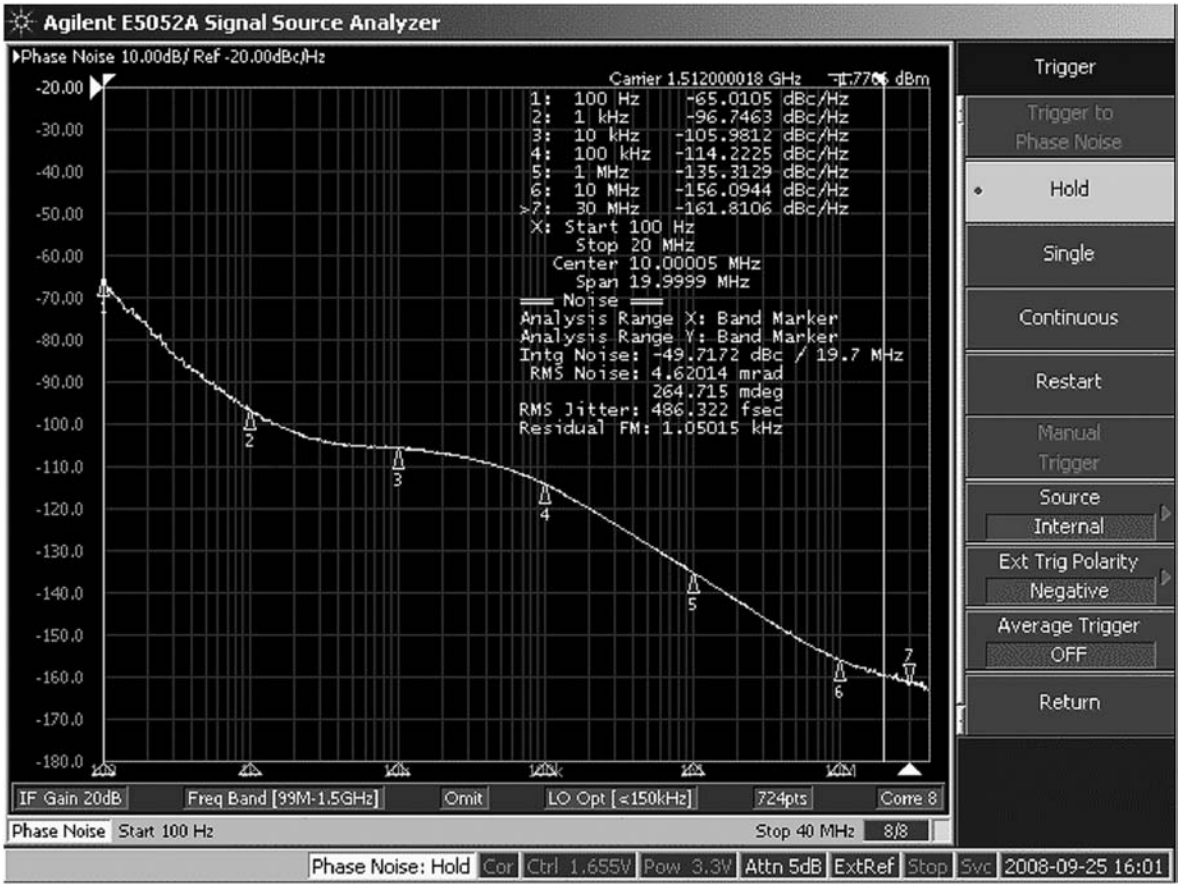
TABLE 10. Suntsu SVD Series, 54 MHz

Reference Clock (MHz)	F_{comp1} (MHz)	PLL1 Loop BW (Hz)	F_{comp2} (MHz)	PLL2 Loop BW (kHz)
27	1.0	30	27	81.9



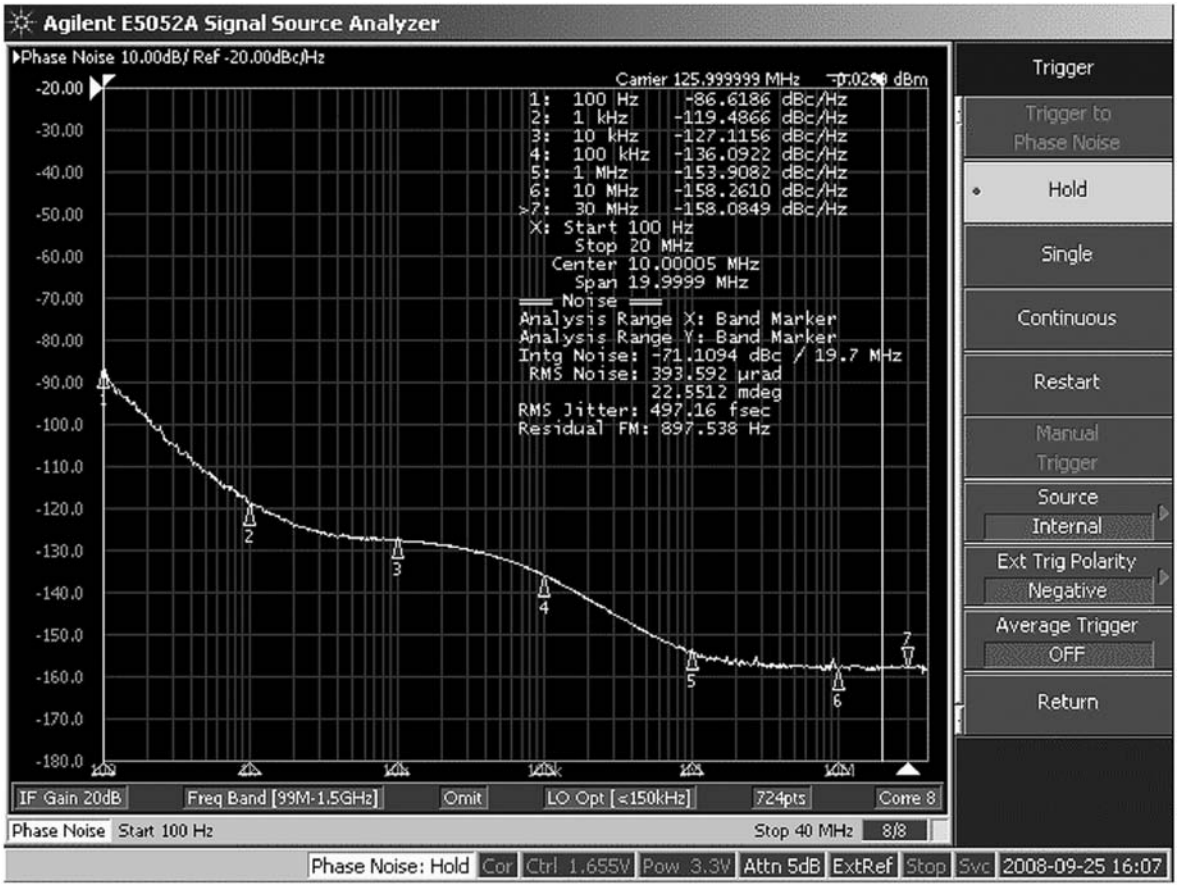
30082839

FIGURE 40. Suntsu SVD Series VCXO, 54 MHz, Open Loop Phase Noise



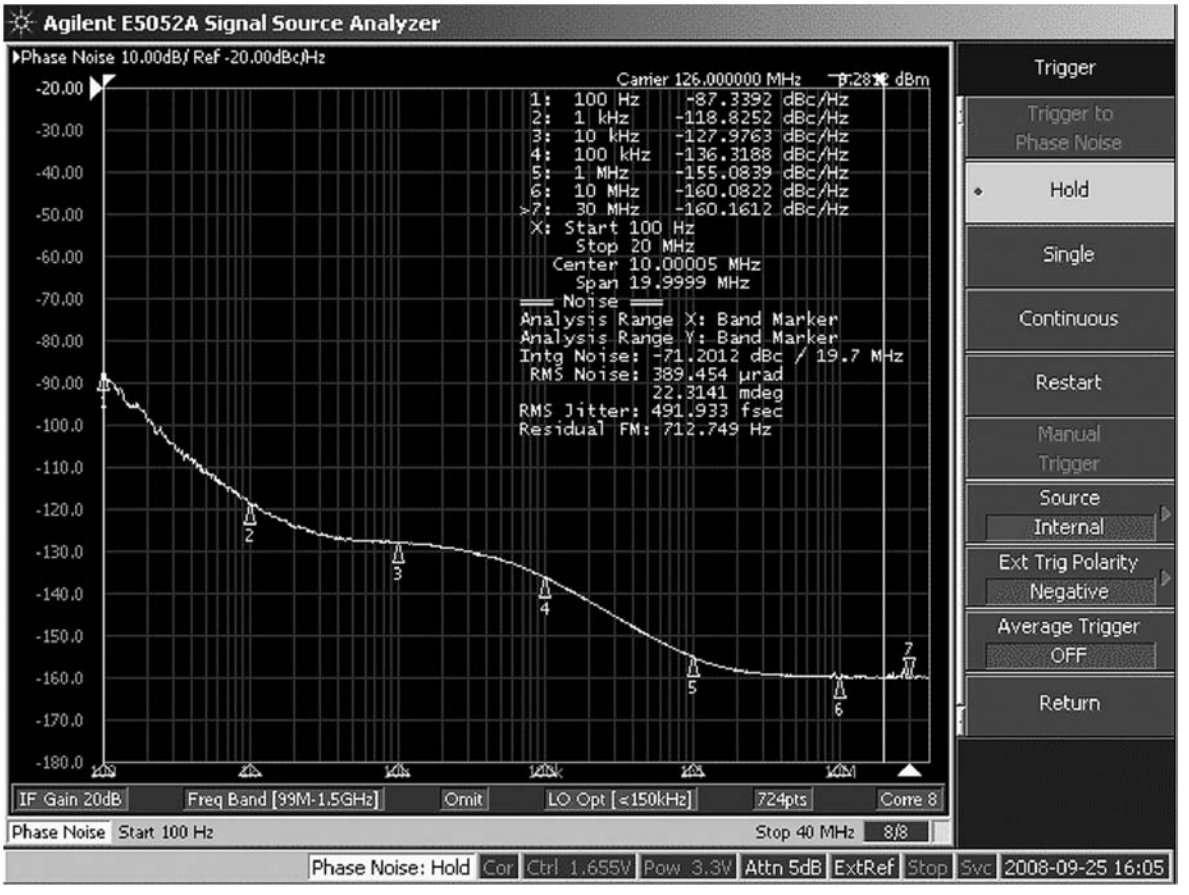
30082840

FIGURE 41. LMK04031 Fout Phase Noise, Suntsu SVD Series VCXO, 54 MHz



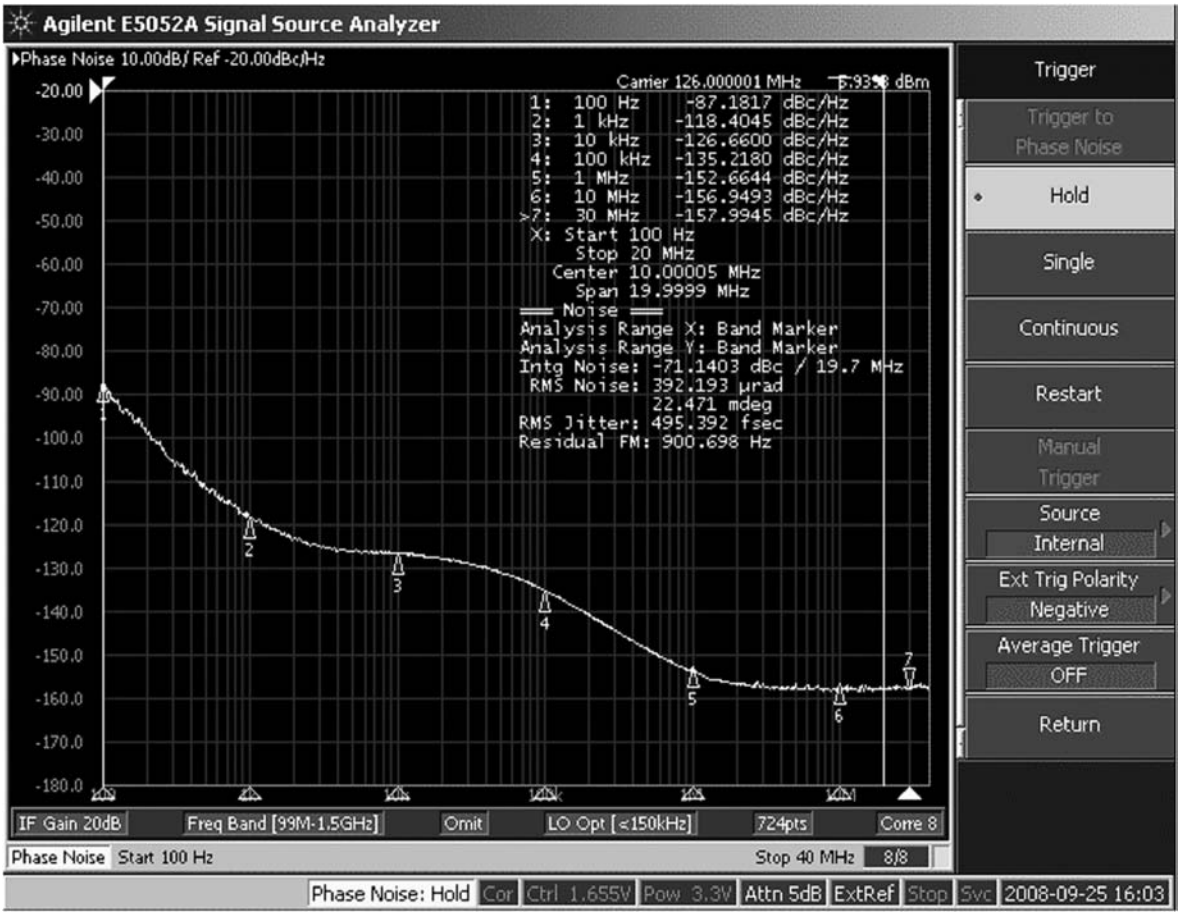
30082841

FIGURE 42. LMK04031 LVDS Phase Noise, Suntsu SVD Series VCXO, 54 MHz



30082842

FIGURE 43. LMK04031 LVCMOS Phase Noise, Suntsu SVD Series VCXO, 54 MHz

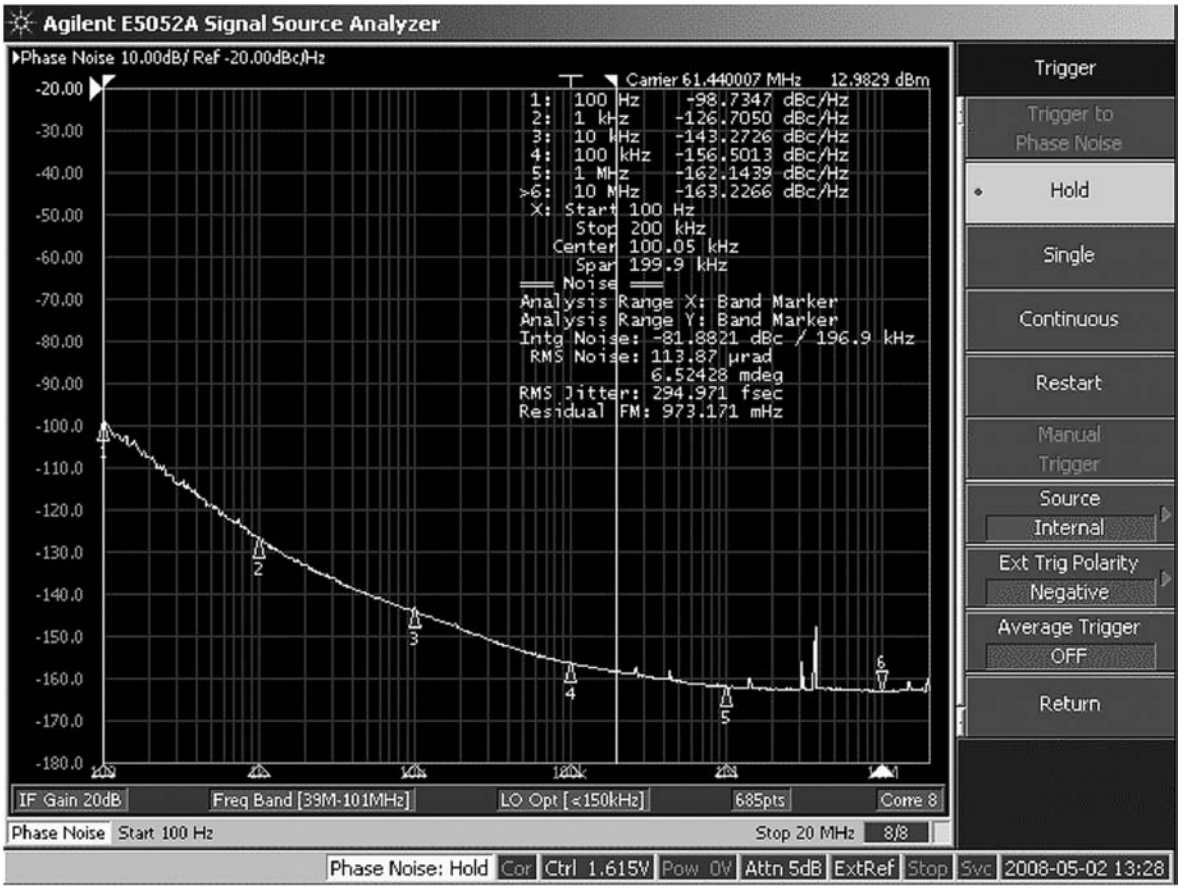


30082843

FIGURE 44. LMK04031 LVPECL Phase Noise, Suntsu SVD Series VCXO, 54 MHz

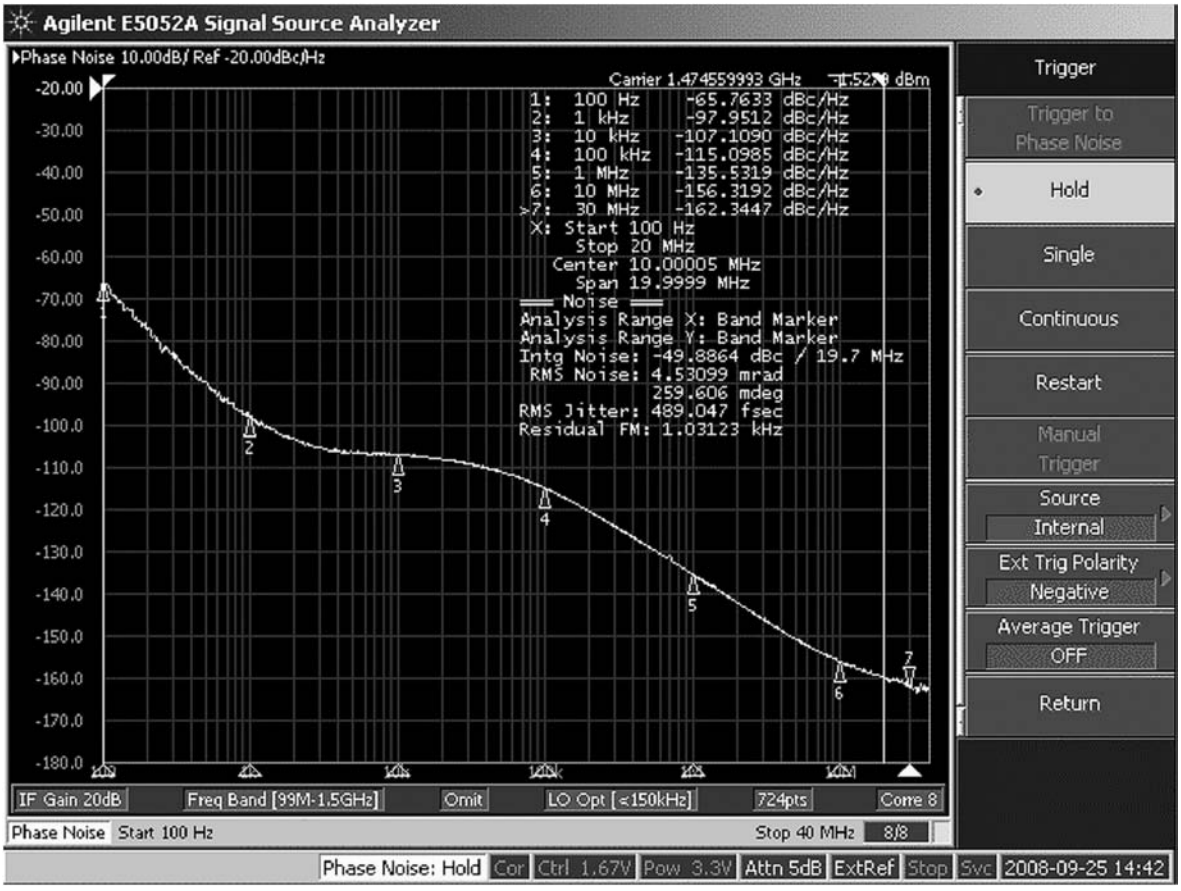
TABLE 11. Suntsu SVD Series, 61.44 MHz

Reference Clock (MHz)	F_{comp1} (MHz)	PLL1 Loop BW (Hz)	F_{comp2} (MHz)	PLL2 Loop BW (kHz)
30.72	1.024	30	30.72	95.4



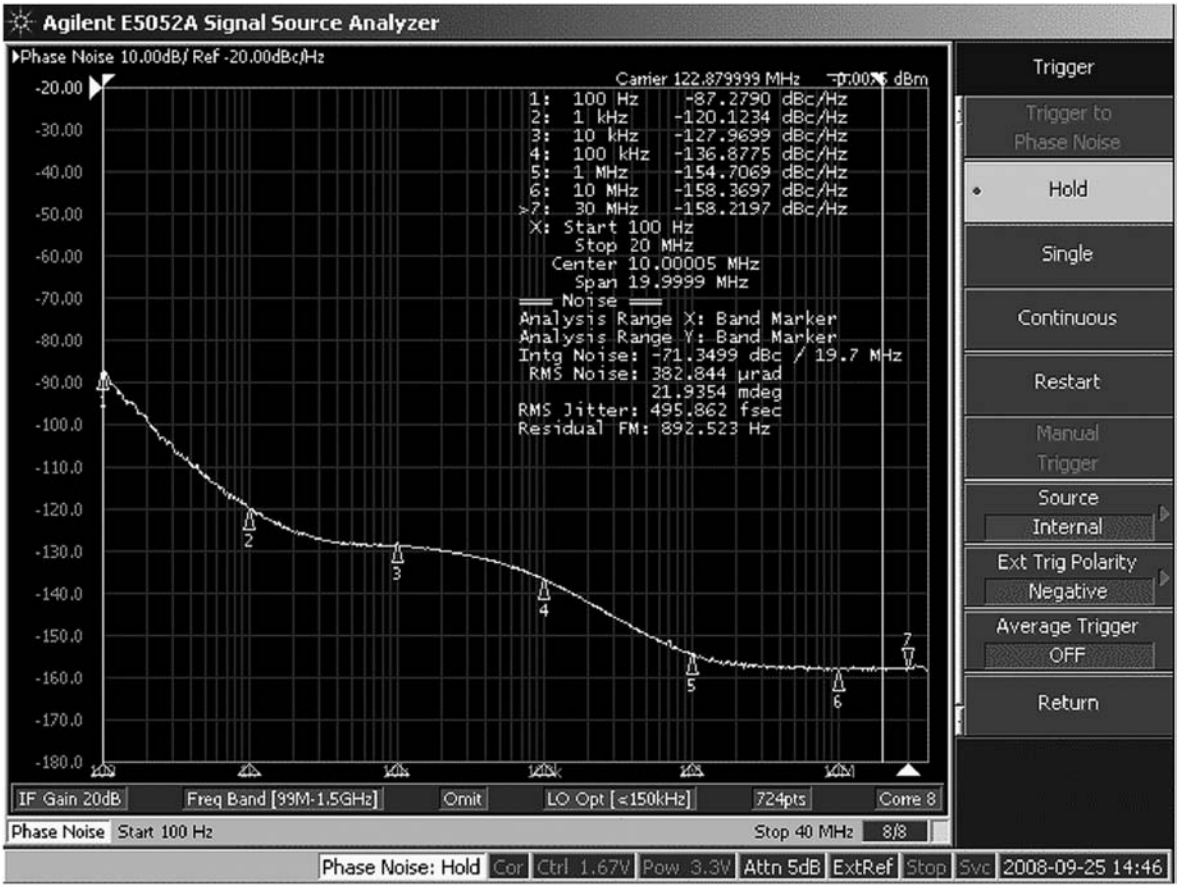
30082844

FIGURE 45. Suntsu SVD Series VCXO, 61.44 MHz, Open Loop Phase Noise



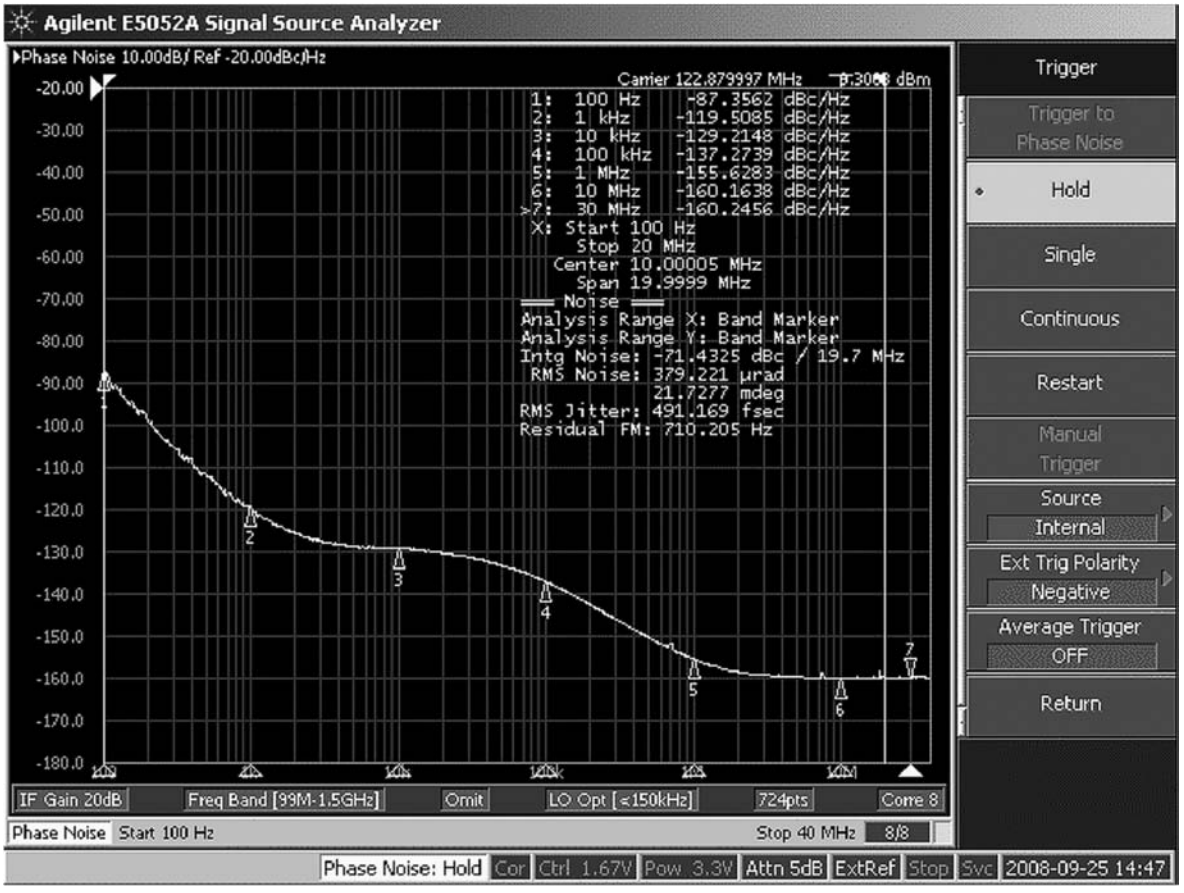
30082845

FIGURE 46. LMK04031 Fout Phase Noise, Suntsu SVD Series VCXO, 61.44 MHz



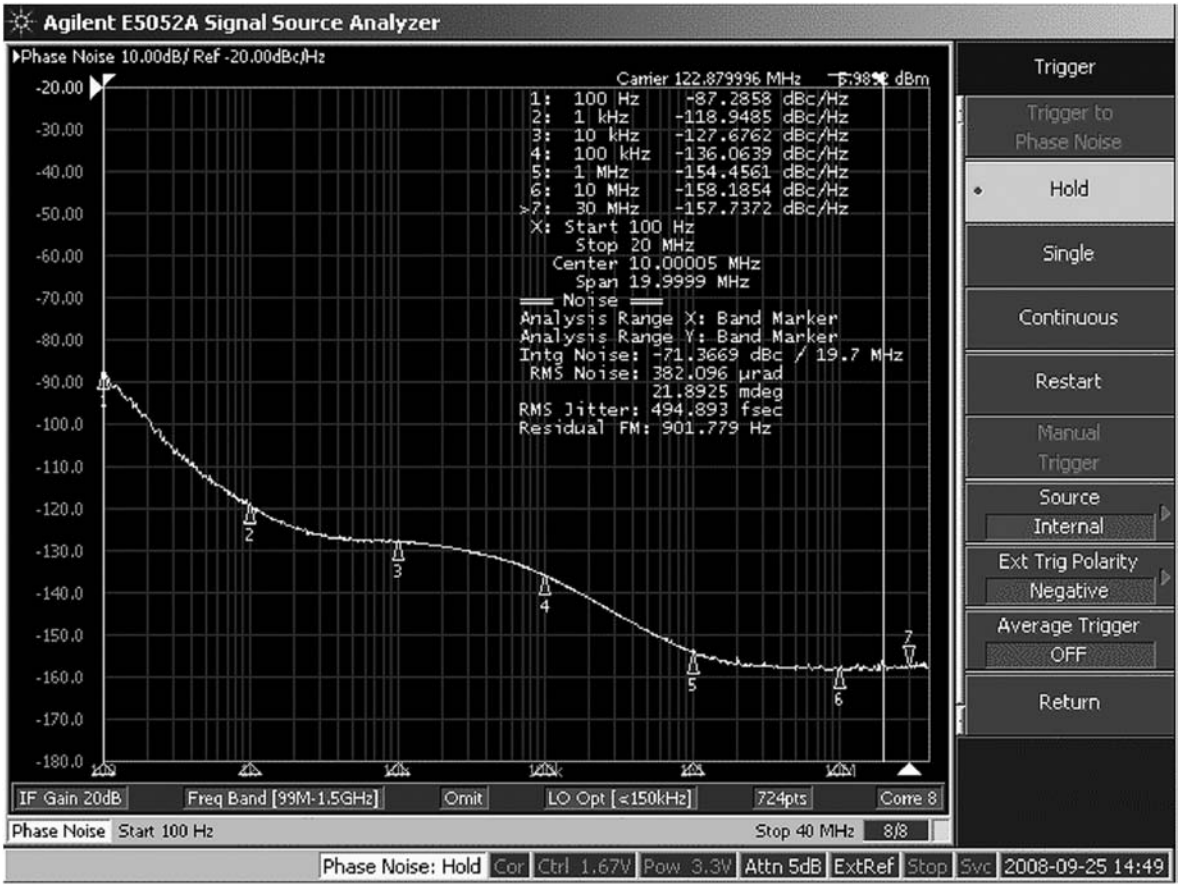
30082846

FIGURE 47. LMK04031 LVDS Phase Noise, Suntsu SVD Series VCXO, 61.44 MHz



30082847

FIGURE 48. LMK04031 LVCMOS Phase Noise, Suntsu SVD Series VCXO, 61.44 MHz

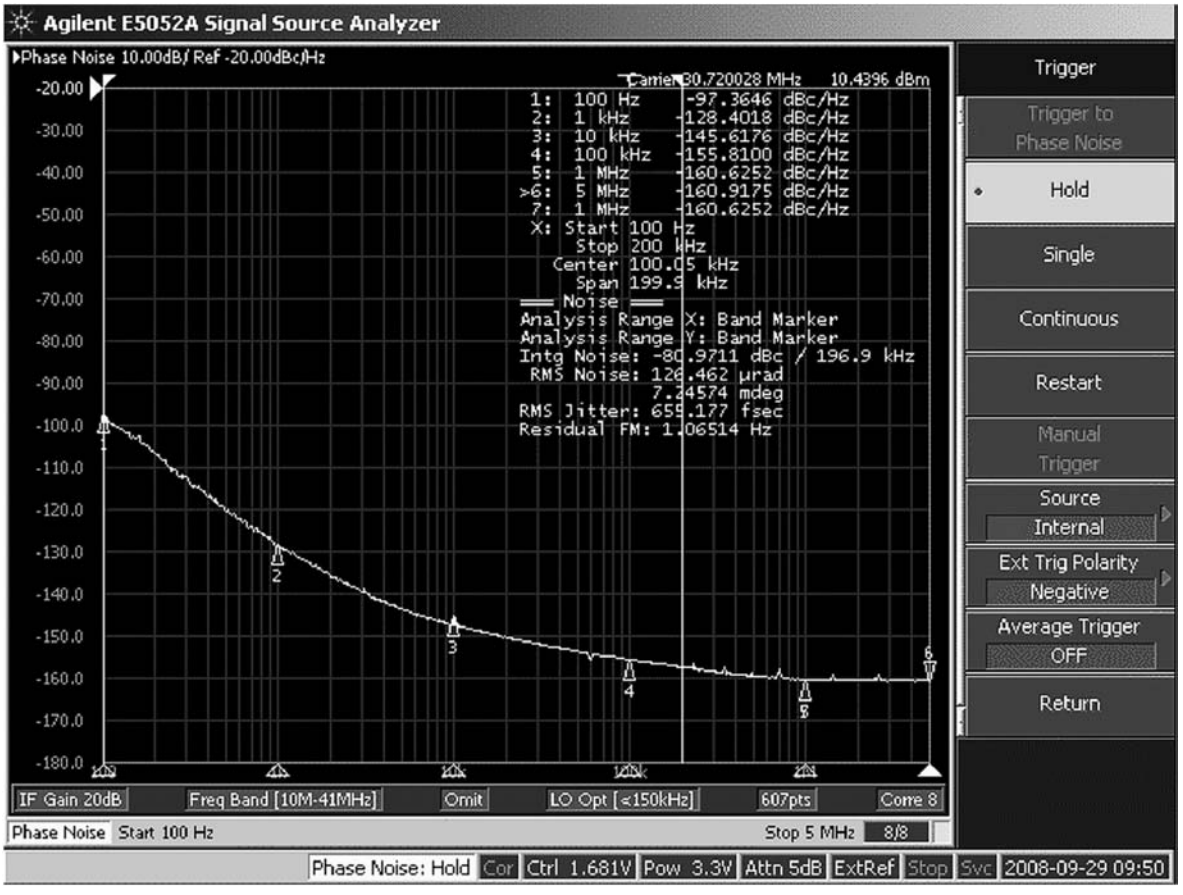


30082848

FIGURE 49. LMK04031 LVPECL Phase Noise, Suntsu SVD Series VCXO, 61.44 MHz

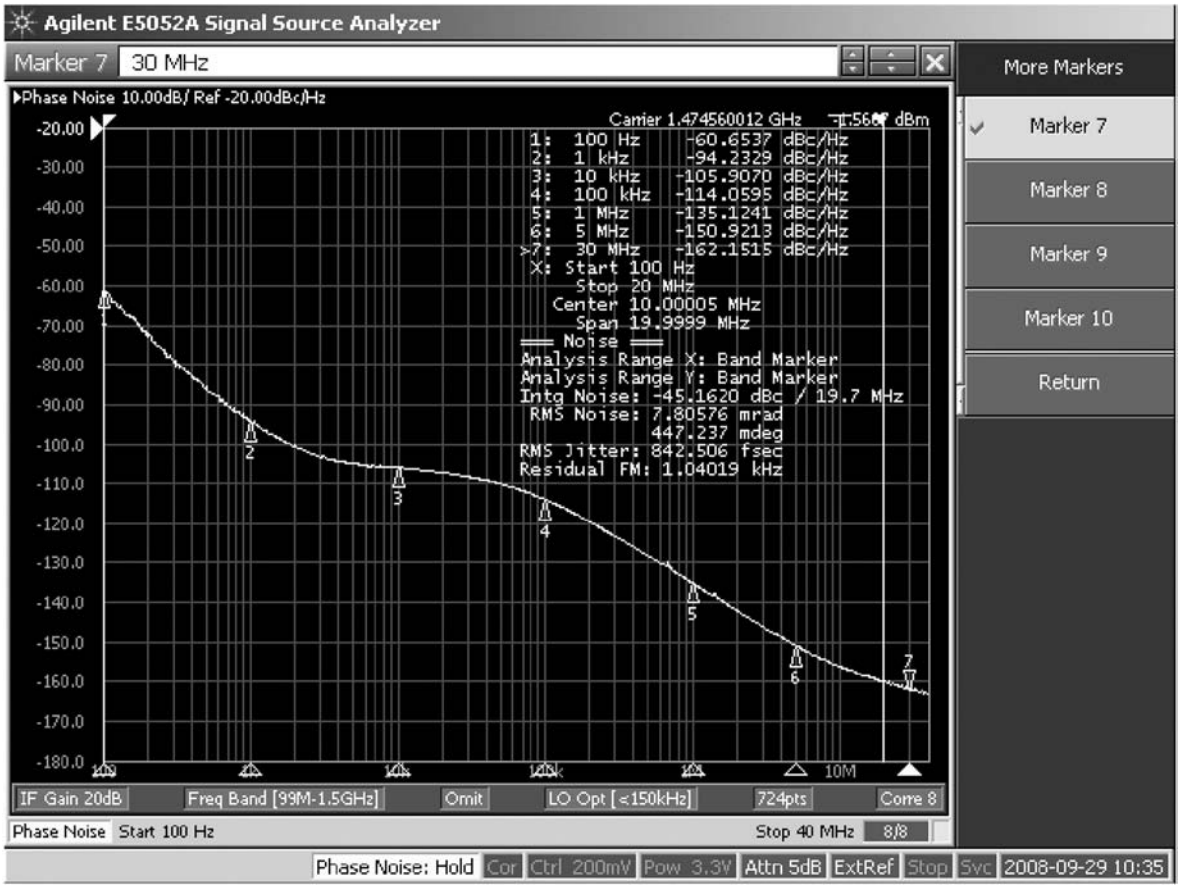
TABLE 12. Suntsu SVD Series, 30.72 MHz

Reference Clock (MHz)	F_{comp1} (MHz)	PLL1 Loop BW (Hz)	F_{comp2} (MHz)	PLL2 Loop BW (kHz)
30.72	1.024	20	30.72	95.4



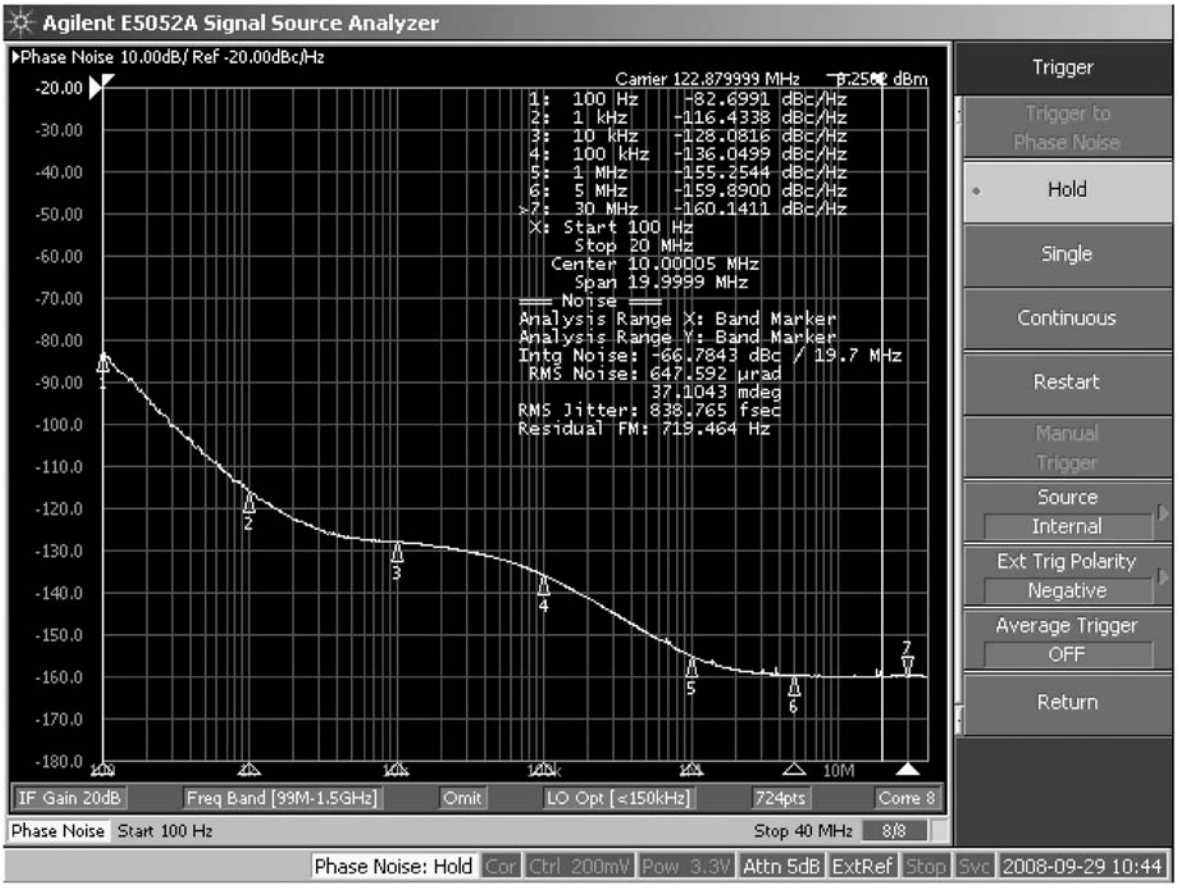
30082849

FIGURE 50. Suntsu SVD Series VCXO, 30.72 MHz, Open Loop Phase Noise



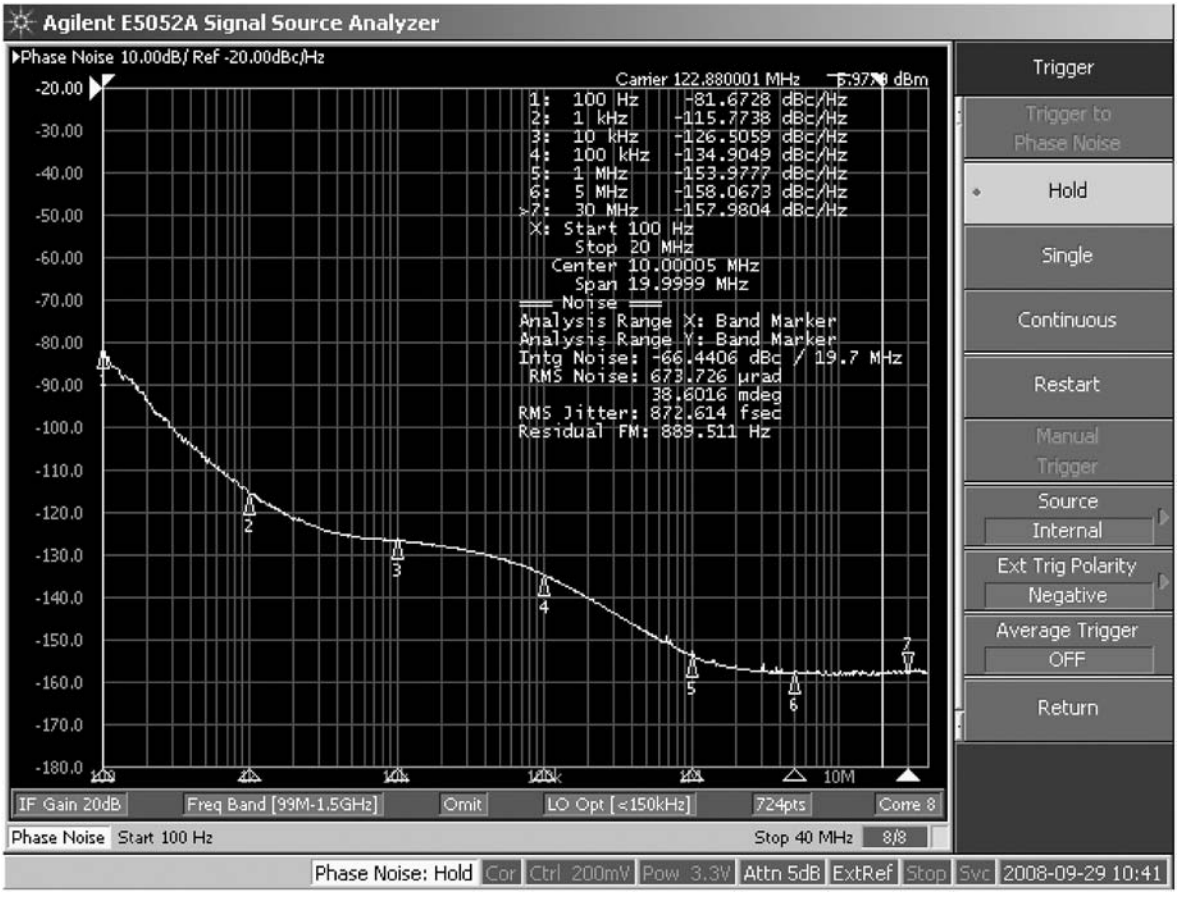
30082866

FIGURE 51. LMK04031 Fout Phase Noise, Suntsu SVD Series VCXO, 30.72 MHz



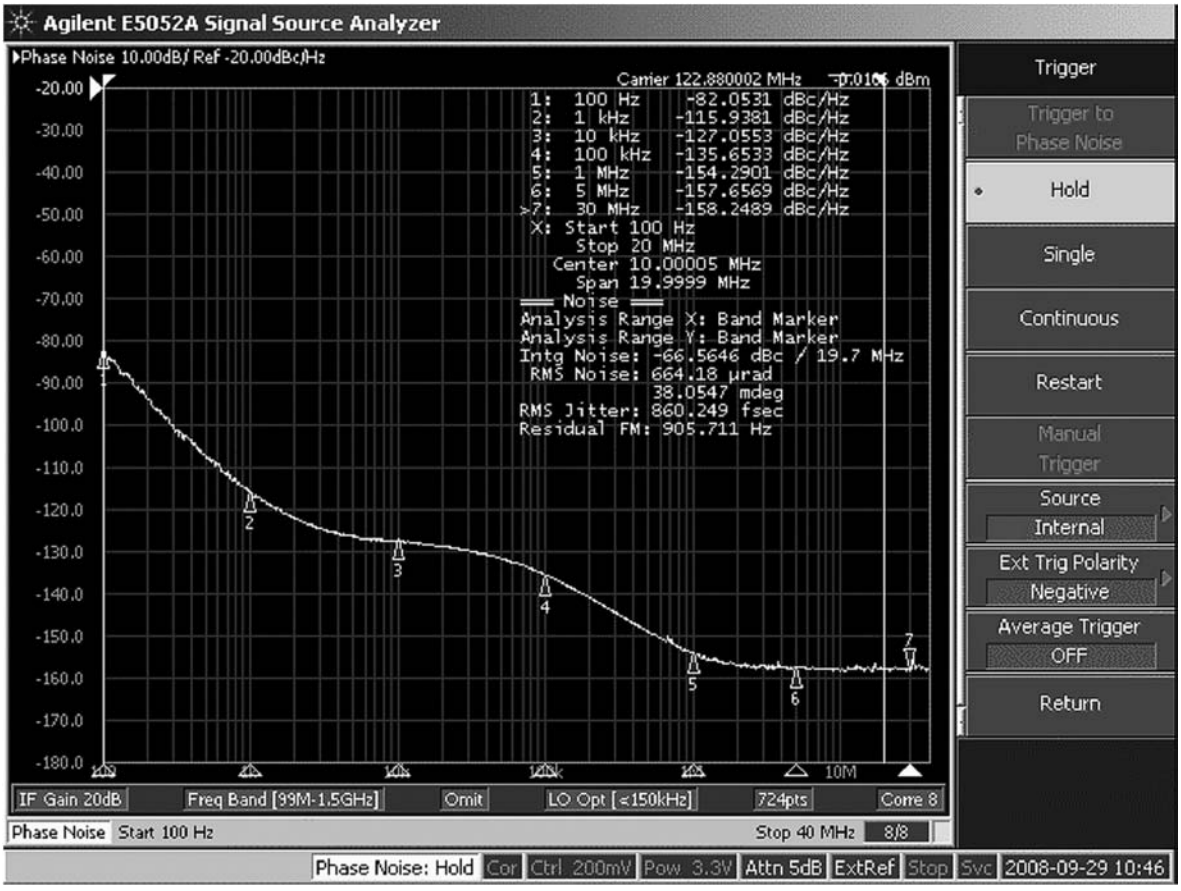
30082867

FIGURE 52. LMK04031 LVCMOS Phase Noise, Suntsu SVD Series VCXO, 30.72 MHz



30082850

FIGURE 53. LMK04031 LVPECL Phase Noise, Suntsu SVD Series VCXO, 30.72 MHz

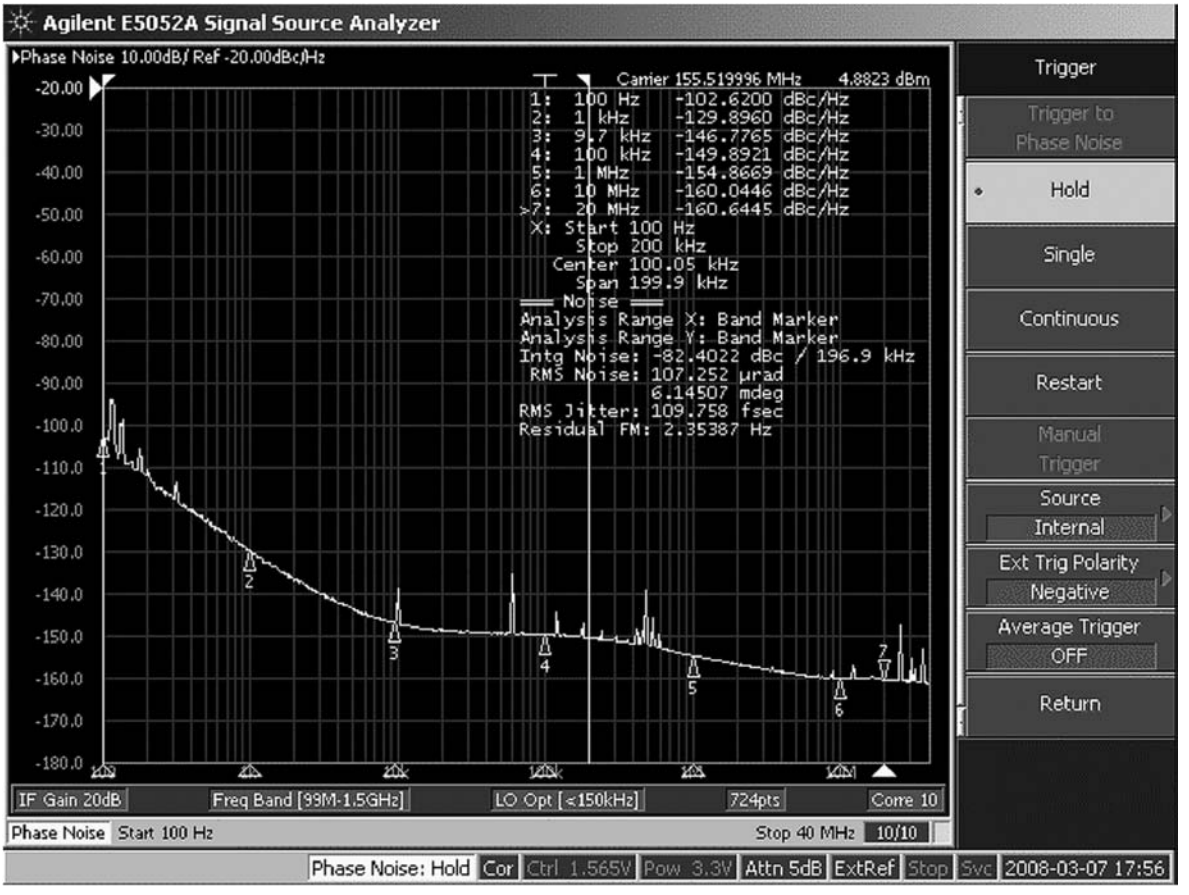


30082851

FIGURE 54. LMK04031 LVDS Phase Noise, Suntsu SVD Series VCXO, 30.72 MHz

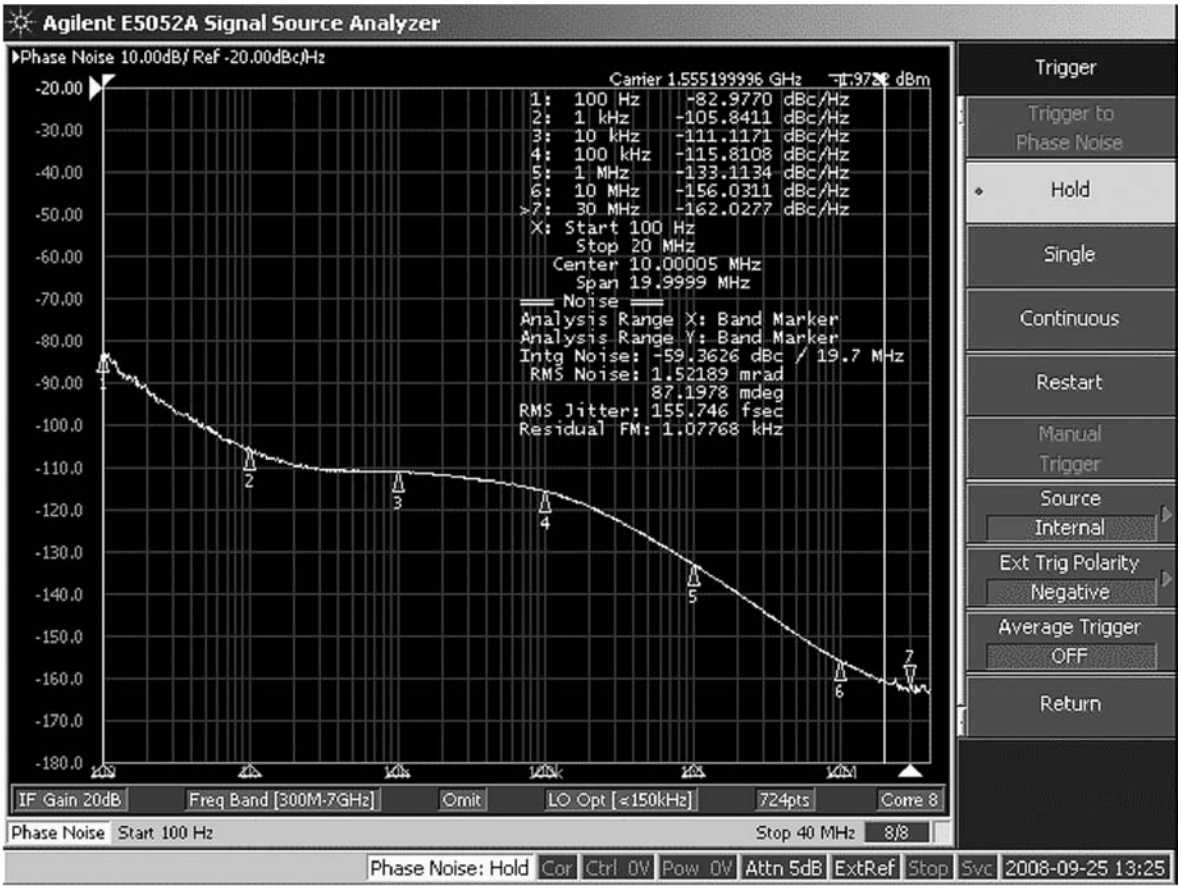
TABLE 13. Vectron Model 5310, 155.52 MHz

Reference Clock (MHz)	F_{comp1} (MHz)	PLL1 Loop BW (Hz)	F_{comp2} (MHz)	PLL2 Loop BW (kHz)
38.88	1.08	30	51.84	152



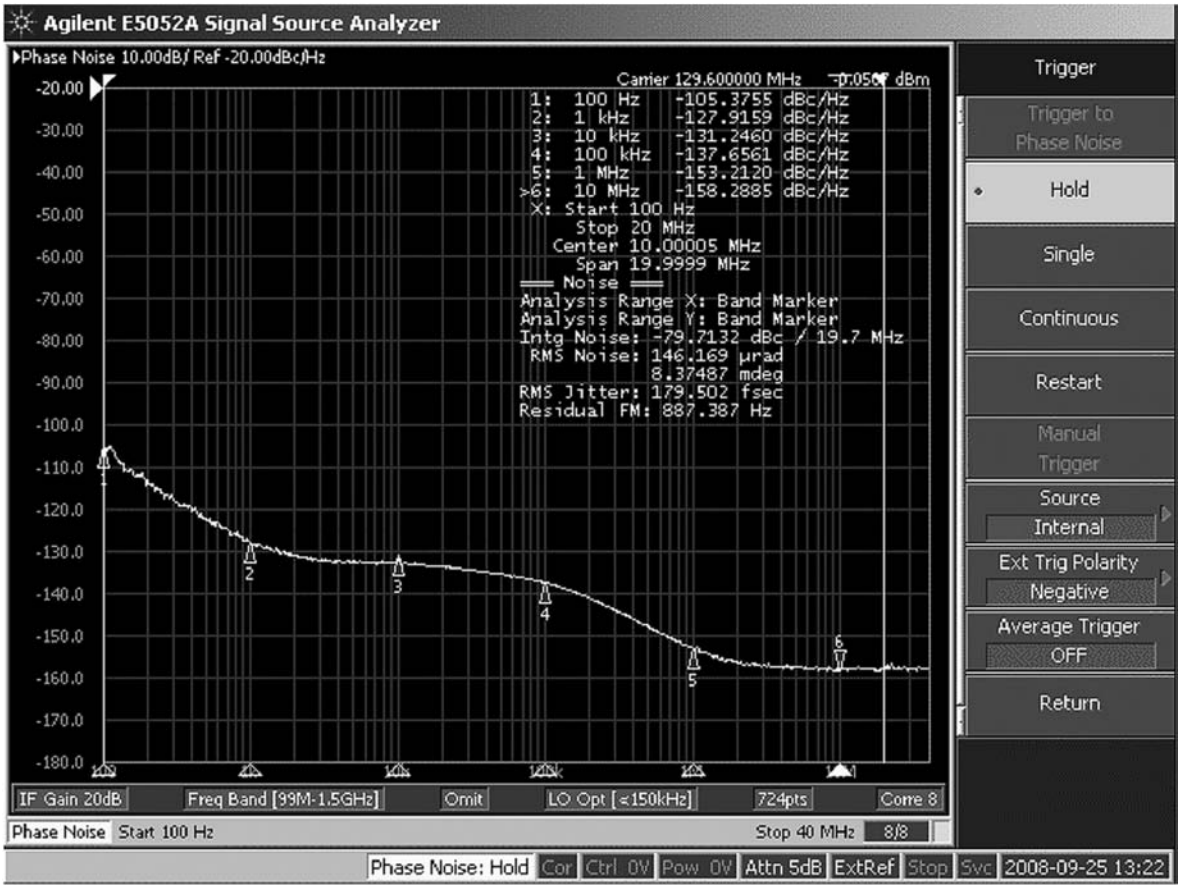
30082852

FIGURE 55. Vectron Model 5310 VCXO, 155.52 MHz, Open Loop Phase Noise



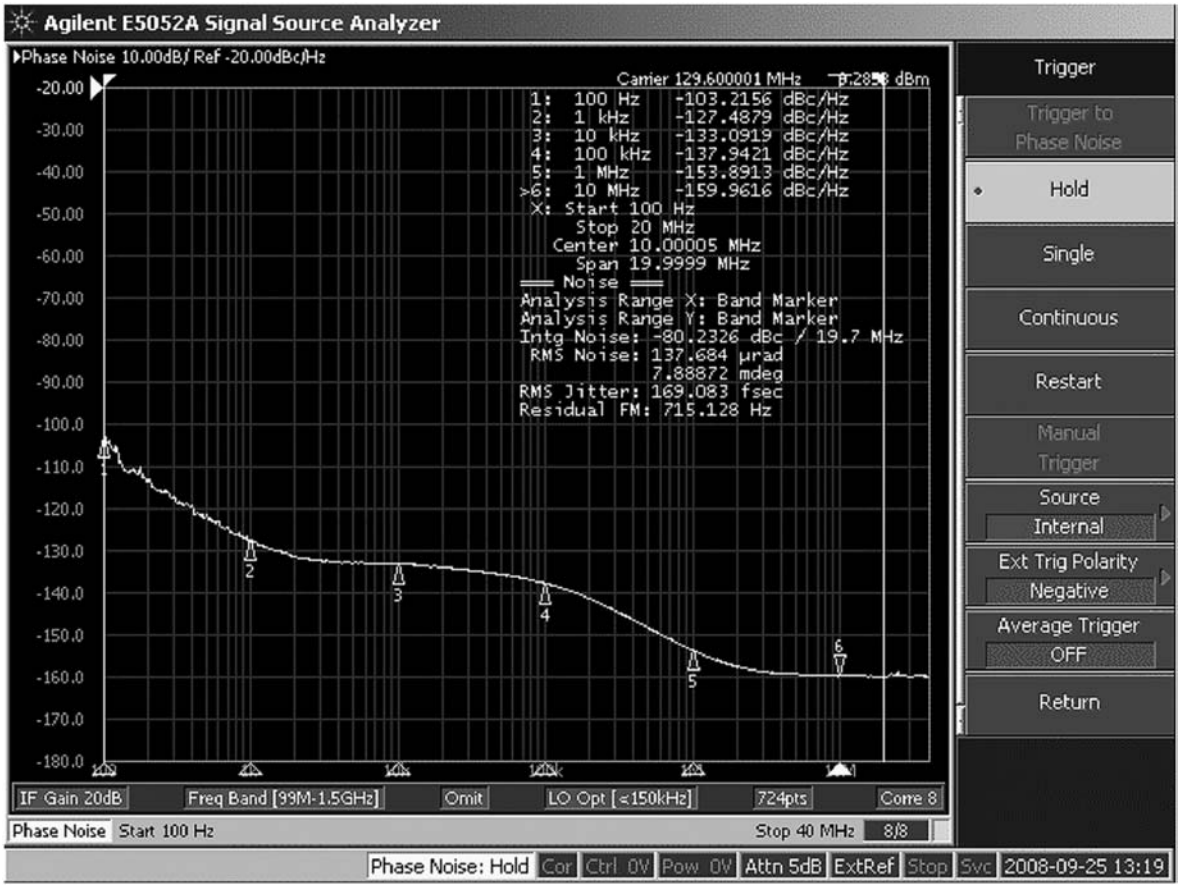
30082853

FIGURE 56. LMK04031 Fout Phase Noise, Vectron Model 5310 VCXO, 155.52 MHz



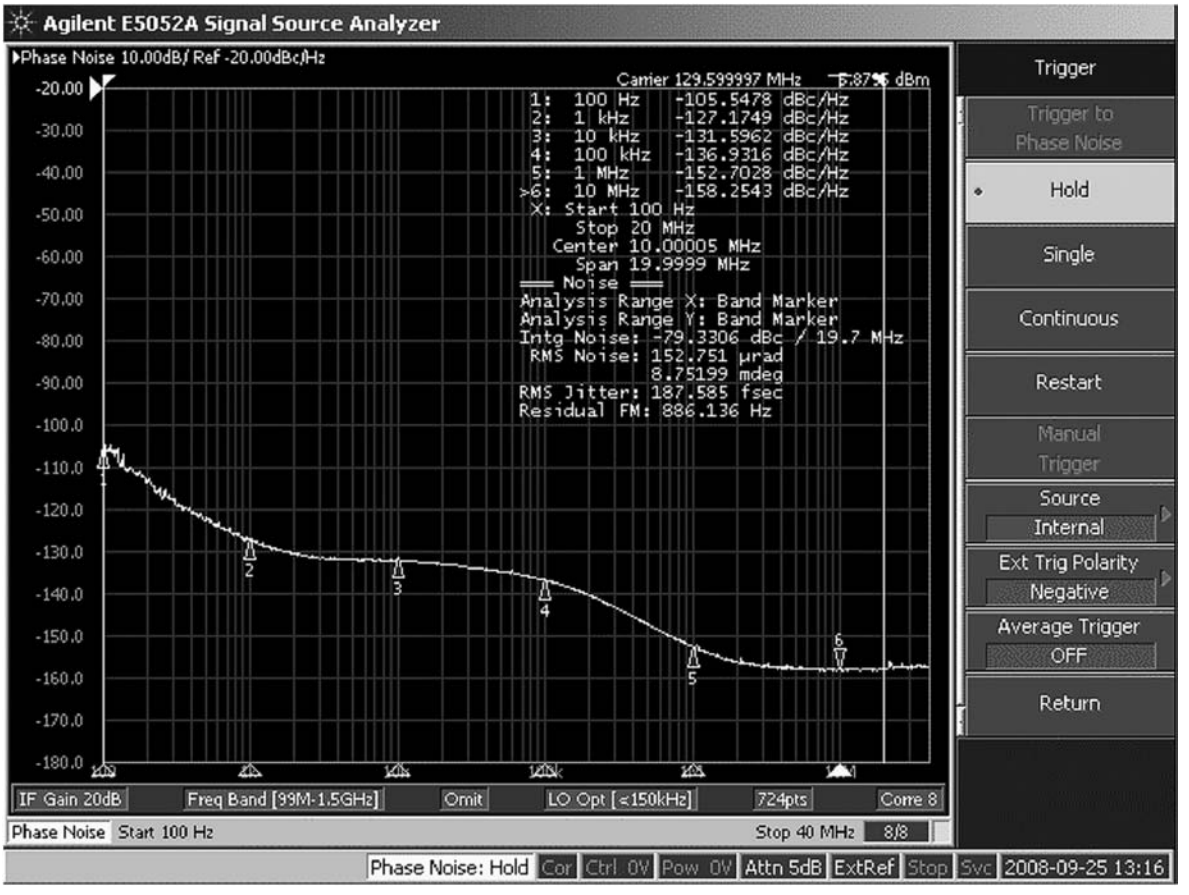
30082854

FIGURE 57. LMK04031 LVDS Phase Noise, Vectron Model 5310 VCXO, 155.52 MHz



30082855

FIGURE 58. LMK04031 LVCMOS Phase Noise, Vectron Model 5310 VCXO, 155.52 MHz

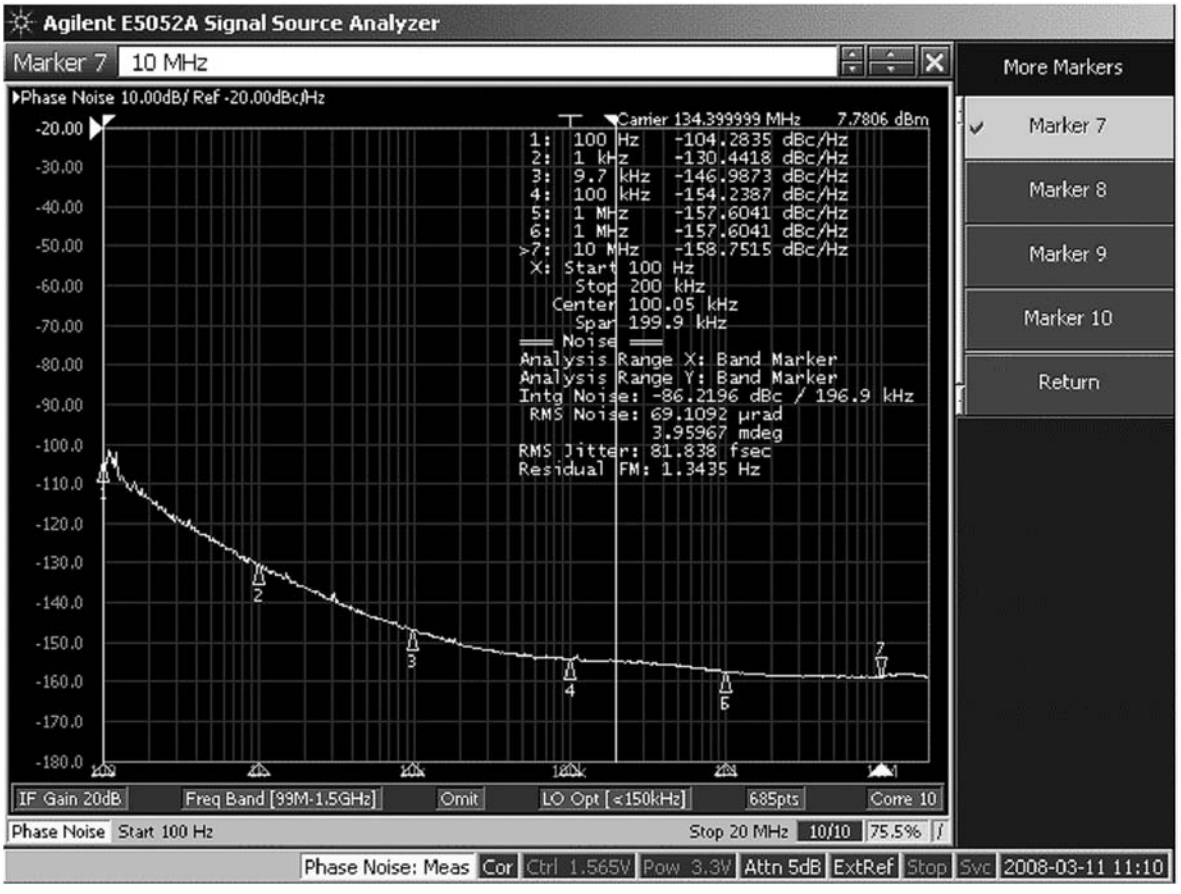


30082856

FIGURE 59. LMK04031 LVPECL Phase Noise, Vectron Model 5310 VCXO, 155.52 MHz

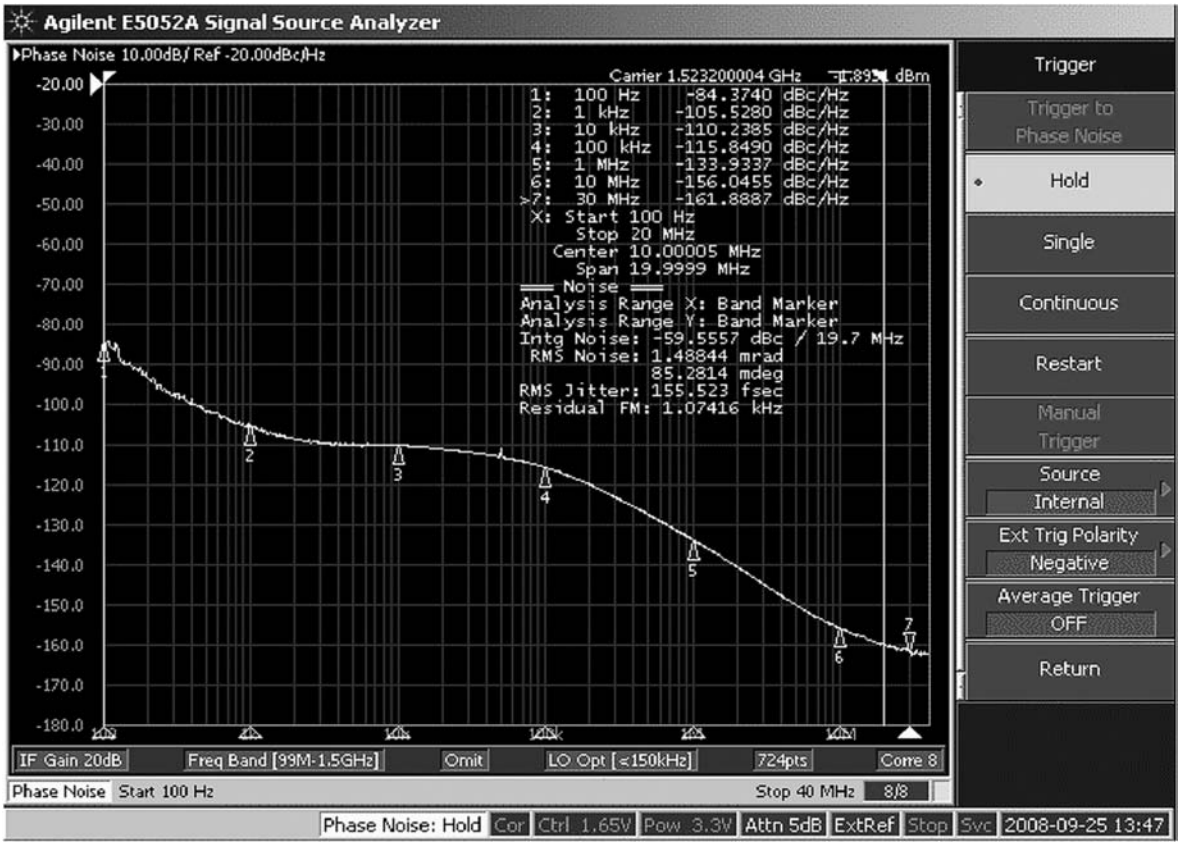
TABLE 14. Vectron Model 5310, 134.4 MHz

Reference Clock (MHz)	F_{comp1} (MHz)	PLL1 Loop BW (Hz)	F_{comp2} (MHz)	PLL2 Loop BW (kHz)
33.6	1.05	30	44.8	134.3



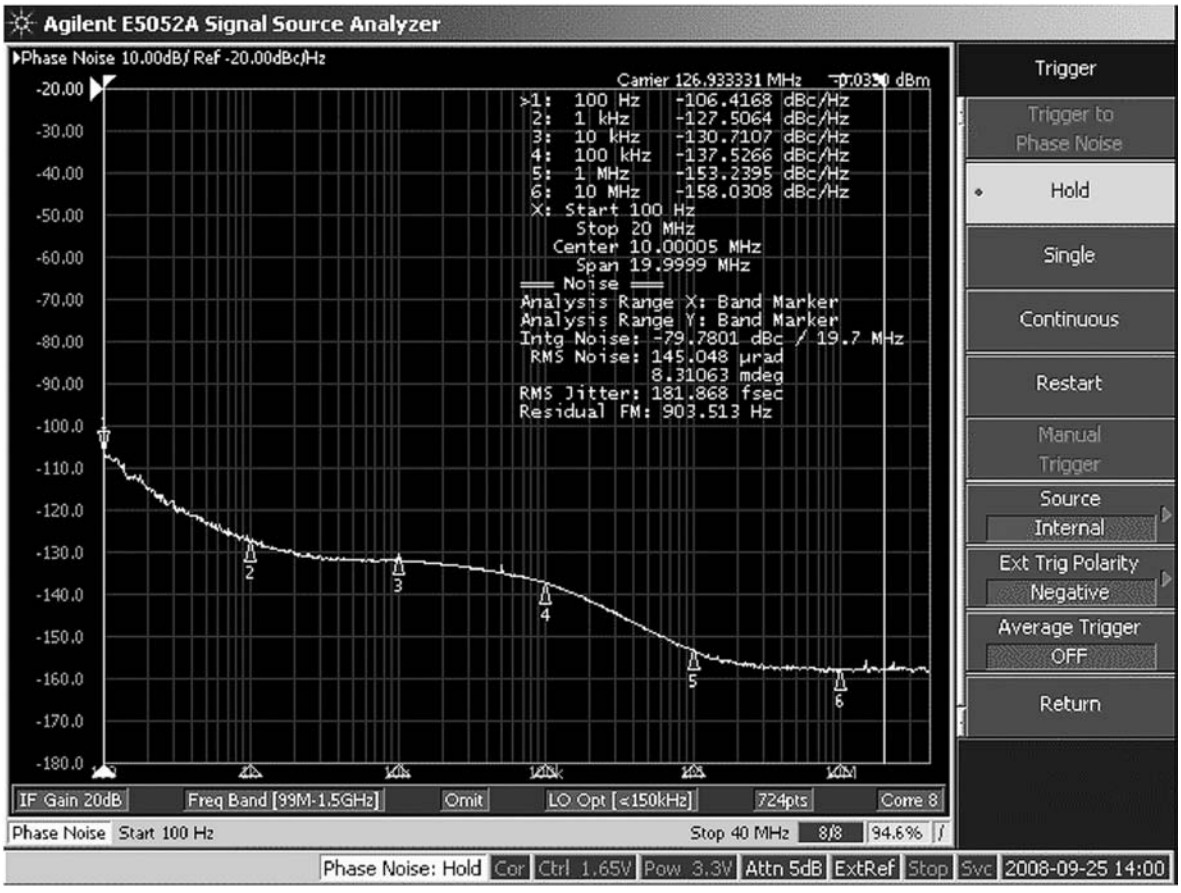
30082857

FIGURE 60. Vectron Model 5310 VCXO, 134.4 MHz, Open Loop Phase Noise



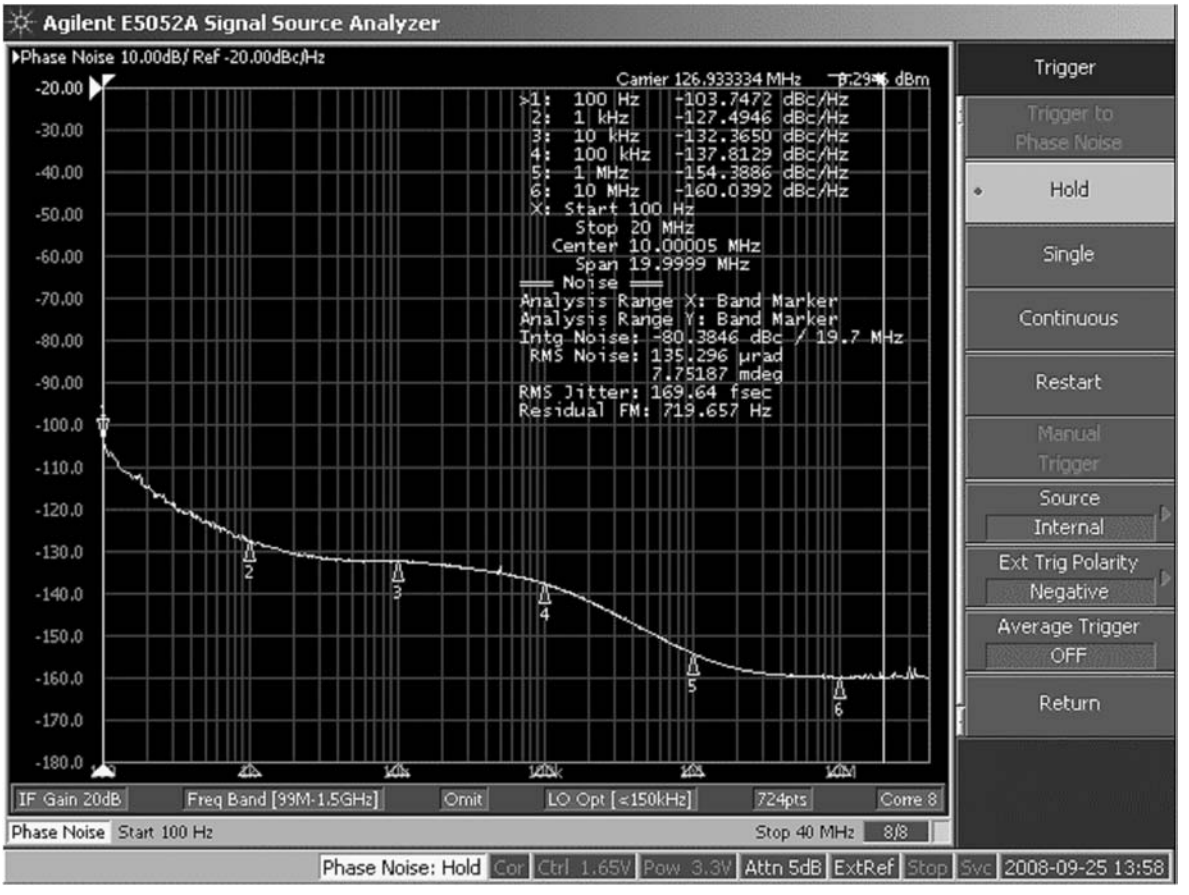
30082858

FIGURE 61. LMK04031 Fout Phase Noise, Vectron Model 5310 VCXO, 134.4 MHz



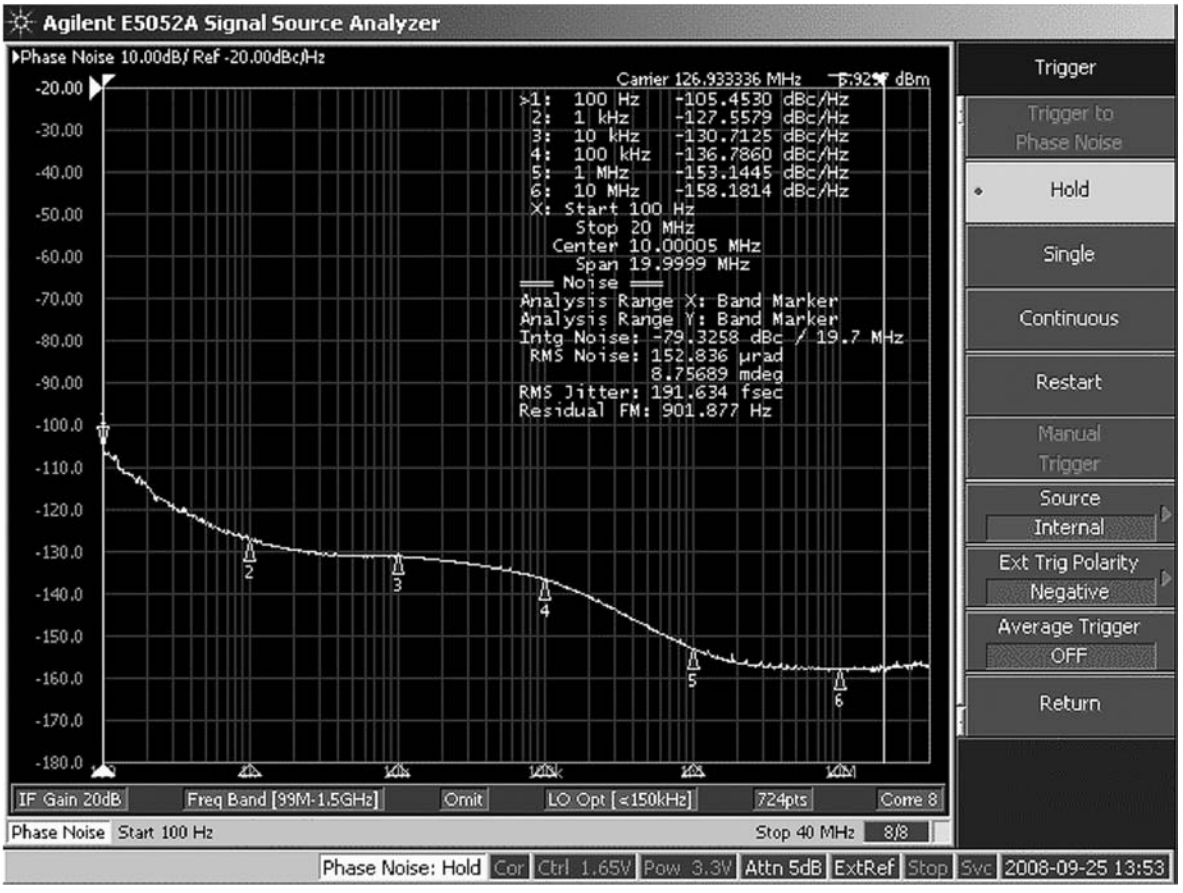
30082859

FIGURE 62. LMK04031 LVDS Phase Noise, Vectron Model 5310 VCXO, 134.4 MHz



30082860

FIGURE 63. LMK04031 LVCMOS Phase Noise, Vectron Model 5310 VCXO, 134.4 MHz



30082861

FIGURE 64. LMK04031 LVPECL Phase Noise, Vectron Model 5310 VCXO, 134.4 MHz

Notes

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