Circuit Applications of Multiplying CMOS D to A Converters

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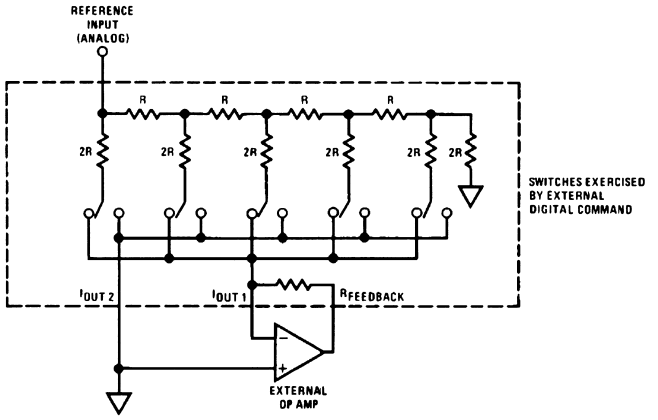
The 4-quadrant multiplying CMOS D to A converter (DAC) is among the most useful components available to the circuit designer. Because CMOS DACs allow a digital word to operate on an analog input, or vice versa, the output can represent a sophisticated function. Unlike most DAC units, CMOS types permit true bipolar analog signals to be applied to the reference input of the DAC (see shaded area for CMOS DAC details). This feature is one of the keys to the CMOS DAC's versatility. Although D to A converters are usually thought of as system data converters, they can also be used as circuit elements to achieve complex functions.

Some CMOS DACs contain internal logic which makes interface with microprocessors and digital systems easy. In circuit oriented applications, however, the "bare bones" DACs will usually suffice. As an example, *Figure 1* shows a 0 kHz–30 kHz variable frequency sine wave generator which has essentially instantaneous response to digital commands to change frequency. This capability is valuable in automatic test equipment and instrumentation applications and is not readily achievable with normal sine wave generation techniques. The linearity of output frequency to digital code input is within 0.1% for each of the 1024 discrete output frequencies the 10-bit DAC can generate.



Details (Simplified) of CMOS DAC1020—Last 5 Bits Shown

Other CMOS DACs are similar in the nature of operation but also include internal logic for ease of interface to microprocessor based systems. Typical is the DAC1000 shown below.

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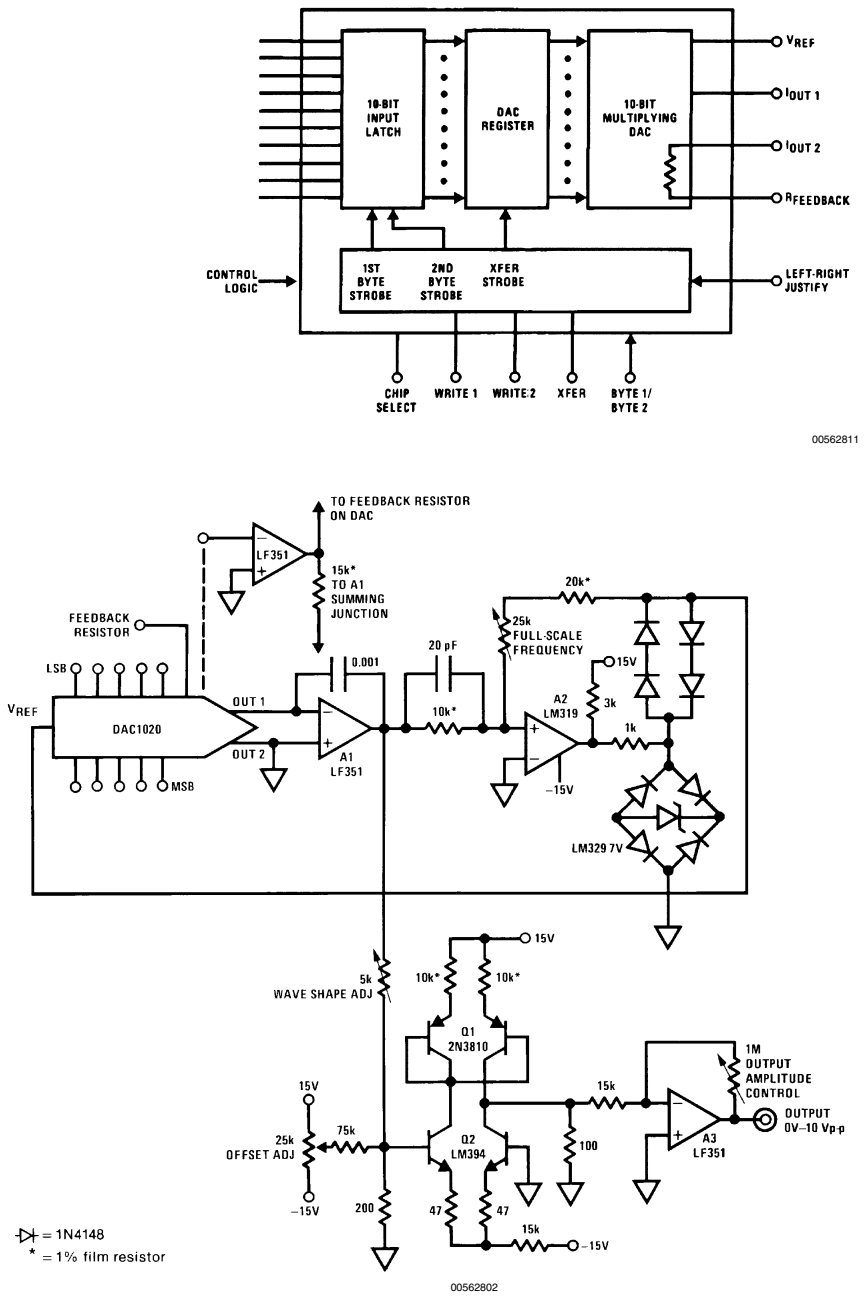


FIGURE 1.

To understand this circuit, assume A2's output is negative. This means that its zener bounded output applies –7V to the DAC's reference input. Under these conditions, the DAC pulls a current from A1's summing junction which is directly proportional to the digital code applied to the DAC. A1, an integrator, responds by ramping in the positive direction. When A1 ramps far enough so that the potential at A2's "+" input just goes positive, A2's output changes state and the potential at the DAC's reference input becomes +7V. The DAC output current reverses and the A1 integrator is forced to move in the negative direction. When the negative-going output of A1 becomes large enough to pull A2's "+" input

slightly, negative A2's output changes state and the process repeats. The resultant amplitude stabilized triangle wave at A1's output will have a frequency which is dependent on the digital word at the DAC. The 20 pF capacitor provides a slight leading response at high operating frequencies to offset the 80 ns response time of A2, aiding overall circuit linearity. The triangle wave is applied to the Q1–Q2 shaper network, which furnishes a sine wave output. The shaper works by utilizing the well known logarithmic relationship between V_{BE} and collector current in a transistor to smooth the triangle wave.

To adjust this circuit, set all DAC digital inputs high and trim the 25k pot for 30 kHz output. Next, connect a distortion analyzer to the circuit output and adjust the 5k and 75k potentiometers associated with the shaper network for minimum distortion. The output amplifier may be adjusted with its potentiometer to provide the desired output amplitude.

This circuit permits rapid switching of output frequency which is not possible with other methods. *Figure 2* shows the clean, almost instantaneous response when the digital word is changed. Note that the output frequency shifts immediately by more than an order of magnitude with no untoward dynamics or delays. If operation over temperature is required, the absolute change in resistance in the DAC's internal ladder network may cause unacceptable errors. This can be corrected by reversing A2's inputs and inserting an amplifier (dashed lines in schematic) between the DAC and A1. Because this amplifier uses the DAC's internal feedback resistor, the temperature error in the ladder is cancelled and more stable operation results.

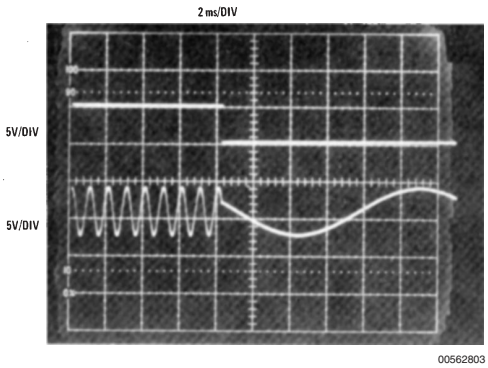


FIGURE 2.

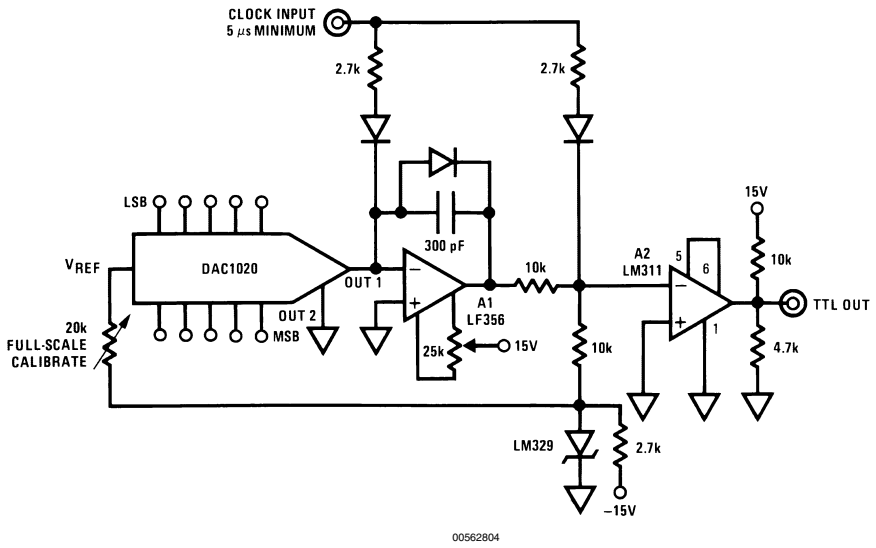


FIGURE 3.

Digitally Programmable Pulse Width Modulator

The circuit of *Figure 3* allows the DAC inputs to control a pulse width. This capability has been used in automatic testing of secondary breakdown limits in switching transistors. The high resolution of control the DAC exercises over the pulse width is useful anywhere wide range, precision pulse width modulation is necessary. In this circuit, the length of time the A1 integrator requires to charge to a reference level is determined by the current coming out of the DAC. The DAC output current is directly proportional to the digital input code. Both the DAC analog input and the reference trip point are derived from the LM329 voltage reference. During the time the integrator output (*Figure 4*, Trace A) is below the trip point, the A2 comparator output remains high (*Figure 4*, Trace B). When the trip point is exceeded, A2's output goes low. In this fashion, the DAC input code can vary the output pulse width over a range determined by the DAC resolution. Traces C, D and E show the fine detail of the resetting sequence (note expanded horizontal scale for these traces). Trace C is the 5 μs clock pulse. When this pulse rises, the A1 integrator output (Trace D) is forced negative until it bounds against the diode in its

Digitally Programmable Pulse Width Modulator (Continued)

feedback loop. During the time the clock pulse is high, the current through the 2.7k diode path forces A2's output low. When the clock pulse goes low, A2's output goes high and remains high until the A1 integrator output amplitude exceeds the trip point. To calibrate this circuit set all DAC bits high and adjust the "full-scale calibrate" potentiometer for the desired full-scale pulse width. Next, set only the DAC LSB high and adjust the A1 offset potentiometer for the appropriate length pulse, e.g., 1/1024 of the full-scale value for a 10-bit DAC. If the 2.2mV/°C drift of the clamp diode in A1's feedback loop is objectionable it can be replaced with an FET switch.

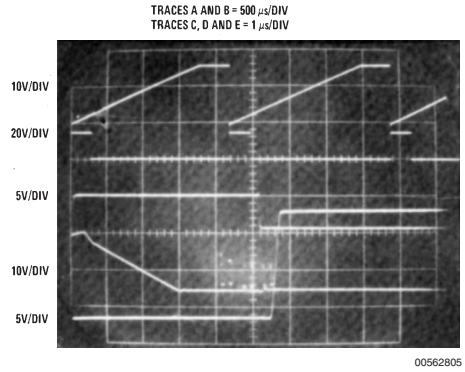


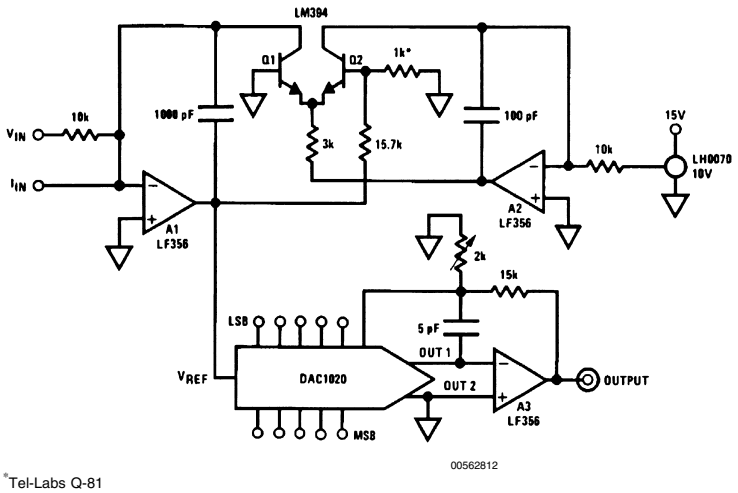
FIGURE 4.

Digitally Controlled Scale Factor Logarithmic Amplifier

Wide dynamic measurement range is required in many applications, such as photometry. Logarithmic amplifiers are commonly employed in these applications to achieve wide measurement range. In such applications it is often required to be able to set the scale factor of the logarithmic amplifier. A DAC controlled circuit permits this to be done under digital control. *Figure 5* shows a typical logarithmic amplifier circuit. Q1 is the actual logarithmic converter transistor, while Q2 and the 1 kΩ resistor provide temperature compensation. The logarithmic amplifier output is taken at A3. The digital code applied to the DAC will determine the overall scale factor of the input voltage (or current) to output voltage ratio.

Digitally Programmable Gain Amplifier

Figure 6 shows how a CMOS DAC can be used to form a digitally programmable amplifier which will handle bipolar input signals. In this circuit, the input is applied to the amplifier via the DAC's feedback resistor. The digital code selected at the DAC determines the ratio between the fixed DAC feedback resistor and the impedance the DAC ladder presents to the op amp feedback path. If no digital code (all zeros) is applied to the DAC, there will be no feedback and the amplifier output will saturate. If this condition is objectionable, a large value (e.g. 22 MΩ) resistor can be shunted across the DAC feedback path with minimal effect at lower gains. It is worth noting that the gain accuracy of this circuit is directly dependent on the open loop gain of the amplifier employed.



*Tel-Labs Q-81

FIGURE 5.

Digitally Programmable Gain Amplifier (Continued)

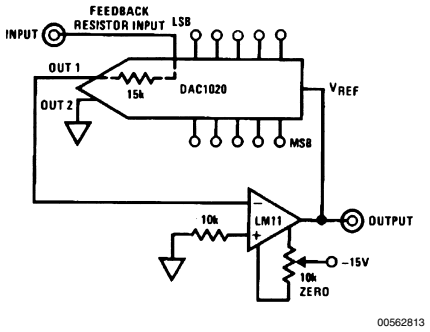


FIGURE 6.

Digitally Controlled Filter

In *Figure 7* the DAC is used to control the cutoff frequency of a filter. The equation given in the figure governs the cutoff frequency of the circuit. In this circuit, the DAC allows high resolution digital control of frequency response by effectively varying the time constant of the A3 integrator. *Figure 8* dramatically demonstrates this. Here, the circuit is driven from the test circuit shown in *Figure 7*.

As each input square wave is presented to the filter the one-of-ten decoder sequentially shifts a "one" to the next DAC digital input line. Trace A is the input waveform, while Trace B is the waveform at A1's output (the reference input of the DAC). The circuit output at A3 appears as Trace C. It is clearly evident that as the decoder shifts the "one" towards the lower order DAC inputs the circuit's cutoff frequency decays rapidly.

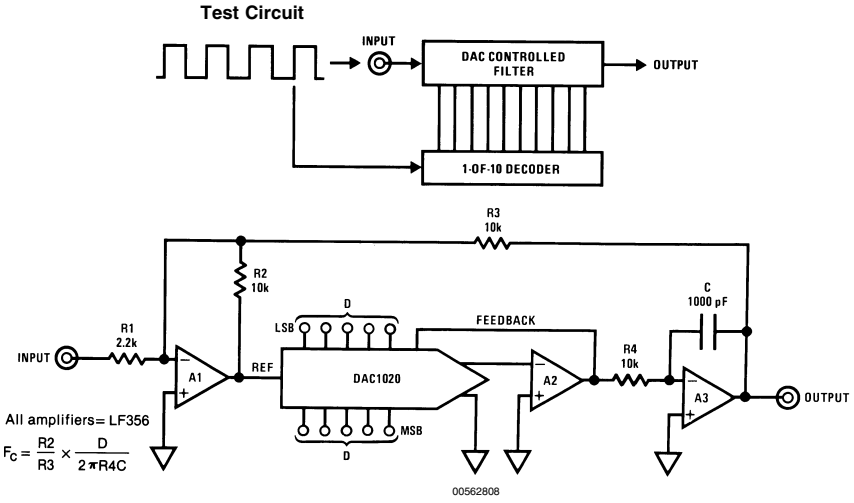


FIGURE 7.

Digitally Controlled Filter (Continued)

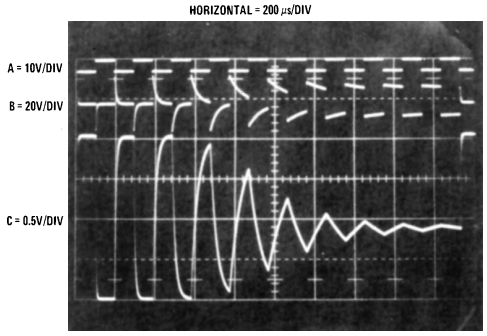


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FIGURE 8.

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