Interfacing National's DS90CR218A and LM98714

National Semiconductor
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1.0 Introduction

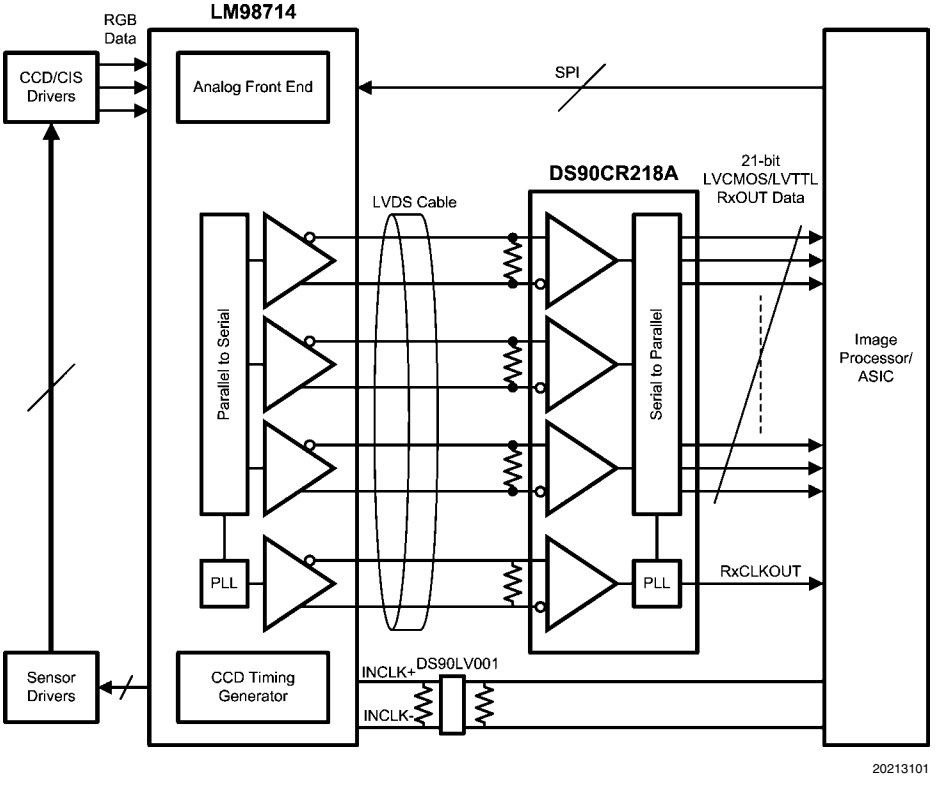
Digital image processing systems like color copier, scanner etc. involve moving large amount of data between the sensor controller unit to the image processor across a 60 to 150 cm cable in an EMI efficient fashion.

National Semiconductor's DS90CR218A, a LVDS channel-link receiver together with LM98714, a 16-Bit, 45 MSPS signal processing AFE (Analog Front End) provide a high performance solution to digitize the CCD/CIS sensor outputs, process it and make it available to the image processor. The LVDS signaling and serialization of the LM98714 output solve the EMI and cable size problems associated with wide, high-speed LVCMOS/LVTTL interfaces operating from 12MHz to 45MHz.

While operating in LVDS mode, the LM98714 serializes the ADC output to 3 data channels with an additional line for the output clock. The DS90CR218A de-serializes the three input LVDS data streams into 21 bits of CMOS/TTL output data. The receiver supports an input clock frequency of 12 to 85 Mhz.

This application note examines the issues that system designers may face when interfacing the DS90CR218A and LM98714. It also offers guidance and solutions on solving these issues that will deliver for a reliable and cost effective LVDS data link.

2.0 System Block Diagram



3.0 Advantages of LVDS

LVDS (Low Voltage Differential Signaling) is a low swing, differential signaling technology which allows high speed data transmission while consuming significantly less power than conventional single ended technologies. In addition, LVDS is less susceptible to common-mode noise, and it also tends to radiate less noise than single-ended signals due to the canceling of magnetic fields. The current-mode driver used in LVDS is also less prone to ringing and switching spikes (switching noise), further reducing noise.

The current-mode, low swing, low noise nature of LVDS technology means data can be switched very quickly without creating noise and power consumption issues, which are common trade-offs for high-speed data transmission applications.

Both the LM98714 and DS90CR218A support LVDS signaling and together enable a low EMI system that is less prone to signal quality issues.

4.0 System Adjustment

4.1 SETUP AND HOLD TIME ADJUSTMENT

When designing for the parallel clock LVDS receiver, such as the DS90CR218A, the system designer must pay close attention to the relationship between the device's clock and its data. The DS90CR218A is a rising edge data strobe LVDS receiver. The rising edge refers to the internal shift clock that is used to strobe the incoming serial data and the outgoing parallel data. It is important to note that the setup time (RSRC) and hold time (RHRC) found on the device datasheet are referred to the rising edge of the clock, as shown on Figure 1. Hence, when interfacing the DS90CR218A output to an image processor/ASIC or any device, system designer must adjust the downlink device to allow for rising edge data strobe.

For the LVDS receiver input, no adjustment is needed because all of the National's LVDS parallel clock transmitter and receiver, including the DS90CR218A and LM98714, use the rising edge of the clock as the reference edge for the LVDS link.

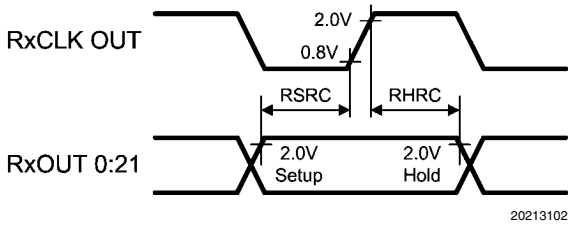


FIGURE 1. DS90CR218A (Receiver) Setup and Hold Time

4.2 RECEIVER SKEW MARGIN CALCULATION

Receiver Skew Margin (RSKM) is defined as the valid data sampling region at the receiver inputs. It is one of the more important parameters that a system designer has to be aware of when designing with Channel-Link receivers. If the margin is less than the total sum of cable skew and jitter, it will limit the performance of the LVDS link and can lead to data sampling errors.

The RSKM specification consists of the receiver's internal PLL strobe positions (RSPOS), and the variation of Transmitter's output data pulse position relative to the output clock (TPPOS). The total margin after accounting for the minimum RSPOS and maximum TPPOS is the receiver input skew margin (RSKM), as shown on Figure 2.

RSKM can be calculated from the following equations:

$$RSKM = Rspos\ (min) - Tppos\ (max)$$

RSKM indicates how much skew and jitter the receiver can tolerate. RSKM must be greater than the sum of clock-to-data skew and all data and clock jitter to achieve error free operation.

$$RSKM > \text{Clock-to-data skew} + \text{Input Clock Cycle-to-cycle jitter} + \text{data jitter}$$

• **Clock-to-data Skew.** Clock-to-data skew should include skew found within the cable pairs and skew from PCB trace.

• **Cycle-to-Cycle Jitter**. It is important to account for the input clock cycle-to-cycle jitter because the receiver uses the previous clock cycle to define the sampling window of the current data cycle. Therefore, the receiver sampling window may vary depending on the amount of cycle-to-cycle jitter present on the clock. The LM98714 and all of National's Channel-Link Transmitters have been designed to help reduce cycle-to-cycle jitter; hence the cycle-to-cycle jitter at the Transmitter's input clock will not pass directly to the receiver. However, to optimize performance when designing with Channel-Link devices, cycle-to-cycle jitter on the clock should be minimized.

• **Data Jitter, ISI, Cross-talk.** When RSKM is specified for a chipset, then the data jitter from the transmitter outputs is already accounted for; therefore, only jitter contributed by the interconnect, such as ISI, and crosstalk induced by the cable and connector should be considered. When the RSKM specification references "Ideal" transmitter pulse positions, then the calculation for the remaining margin should include variances in the transmitter pulse position (typically the worst case number is used), data jitter, ISI, and crosstalk from the cable/connector fixture.

For more information on Channel-Link's RSKM calculation, please refer to National's AN-1059 and the Channel Link Design Guide.

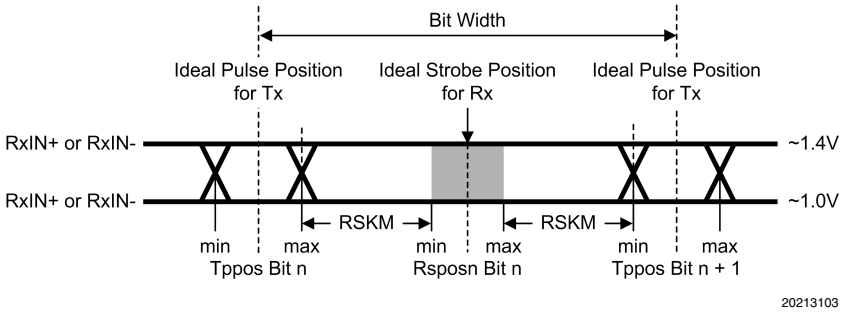


FIGURE 2. DS90CR218A (Receiver) Skew Margin

4.3 TIMING MARGIN

Note that the DS90CR218A datasheet's RSKM specification references Ideal Pulse Positions (Tppos Ideal), so when calculating for RSKM, the Transmitter's pulse position and data jitter must be included.

The following table shows the typical RSKM of the DS90CR218A when using the LM98714 as a Transmitter at 12MHz.

Symbol	Parameter	Typ
RSKM	Receiver Skew Margin with LM98714 as Transmitter	0.968 ns

5.0 PCB Layout Guideline

To optimize the performance of the DS90CR218A and LM98714, good high-speed PCB layout techniques should be used. This section provides the system designer some general design recommendations and guidelines for PCB layout.

5.1 GENERAL GUIDELINE

• Place the components so that PCB traces do not take a lot of turns, corners, and pass through PCB vias when going from one component to another.

• For LVDS or any other high-speed differential signaling device, keep transmitters and receivers as close to the connector as possible.

• Separate high frequency or high level inputs and outputs to minimize unwanted stray noise pickup, feedback, and interference. It is best to put any fast edge rate CMOS/TTL and LVDS signals on a different layer(s).

• Use at least 4 PCB board layers: LVDS signals, ground, power, TTL/CMOS signals. Dedicating planes for power and ground are typically required for high-speed system design.

• Power system performance may be greatly improved by using thin dielectrics (4 to 10 mils) for power/ground sandwich; this will create an excellent high frequency bypass capacitance, making the value and placement of external bypass capacitors less critical.

• External bypass capacitors should be placed as close as possible to the power pins to minimize parasitic effect. One or two multi-layer ceramic (MLC) surface mount capacitors (0.1uF or 0.01uF) in parallel should be used between each power pin and ground pin for best results.

• Good power supply design practice also includes a bulk capacitor at the point of power entry. This is typically in the range of 50uF to 100uF and will smooth low frequency noise.

5.2 DEVICE SPECIFIC RECOMMENDATION

General device-specific bypassing recommendations are provided below.

5.2.1 DS90CR218A

• **Pair-to-Pair Skew.** Always minimize pair-to-pair skew on LVDS inputs; particularly, the skew between LVDS data and clock lines. Large skew between LVDS clock and data pairs can cause mis-sampling of data. Make sure pair-to-pair skew meets RSKM requirements.

• **LVDS Traces.** LVDS pairs should be closely coupled and designed for 100Ω differential impedance. Route the differential pair traces as close together as possible and as soon as they leave the IC. This helps to eliminate reflections and ensures that the majority of common-mode noise is rejected.

• **LVDS Termination.** LVDS termination is required for DS90CR218A. Choose the termination resistor value to match the loaded differential impedance of the transmission line. The value of the termination is typically 100Ω. Place termination resistors as close as possible to the receiver inputs or end of the transmission lines.

• **PLL Supply.** The DS90CR218A requires a clean power supply – less than 100mV noise peak-to-peak. PLL VCC noise in the frequency range of 200 kHz to 3 MHz can increase jitter and reduce noise margin; therefore, a CRC or CLC notch filter may be required to filter out noise in this spectrum.

• **LVDS Supply.** Typically, a 0.1uF capacitor is sufficient for the LVDS power supply pins. If space is available, a 0.01 uF capacitor (Place smaller value capacitors closer to the device) may be used in parallel for additional high-frequency filtering. Connect the LVDS ground to the cable ground to provide a return path for any common (even) mode currents.

• **Digital Supply.** Good digital supply filtering is critical for the DS90CR218A when multiple outputs switch at the same time (simultaneous switching noise). An estimate of local capacitance required indicates a minimum of 34nF is required. Rounding up to a standard value, 0.1uF is selected for each Digital power pin.

5.2.2 LM98714

• **PLL Setting.** The default settings for the LM98714's PLL is optimized around the middle of its operating frequency range. This can be tuned to better match the operating frequency of the application in order to improve the system skew margin. So, while operating at the 12 Mhz frequency the PLL setting register (Page 0, Main Configuration Register 3, Bit[2:0]) can be set to low frequency mode (3'b000). The default for this register is 3'b111. Please refer to LM98714 datasheet for additional details on this setting.

6.0 References

1. Channel Link Design Guide, National Semiconductor, June 2006, www.national.com/appinfo/lvds/files/channellink_design_guide.pdf

2. AN-1059, High Speed Transmission with LVDS Link Devices, June 1998, http://www.national.com/an/AN/AN-1059.pdf

3. LM98714 3 Channel, 16Bit 45MSPS AFE with LVDS output and Sensor Timing Generator Datasheet, June 2006, www.national.com

4. DS90CR218A +3.3V Rising Edge Data Strobe LVDS 21-Bit Channel Link Receiver Datasheet, September 2006, http://www.national.com/appinfo/lvds/

Notes

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