USB I²C Interface Board Reference Manual

National Semiconductor
Application Note 1840
Jose Escobar
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Introduction

The USB I²C Interface board interacts with your application hardware via an USB port in a PC. The Microcontroller with flash memory enables to control your application hardware and develop specific application functions via software. (*National Semiconductor does not provide interaction software, which networks both application board and I²C board.*)

USB I²C Interface Board Key Features

- National's COP8CBE9 microcontroller in a TSSOP package
- National's USBN9604 IC in a 28-pin CSP package
- USB 2.0 compatible
- Bus Powered
- 24 MHz clock from crystal
- 8–pin Analog inputs for A/D converter

Block Diagram

Figure 1 shows basic connections between the PC, USB I²C Interface Module, and application board.

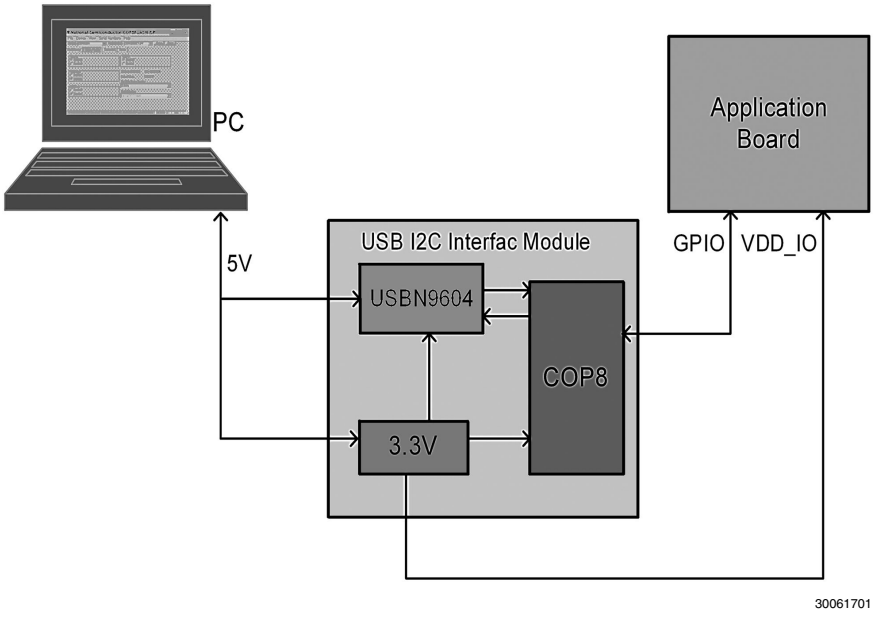

FIGURE 1. Block Diagram

System Requirements

The following requirements are vital in order to use the USB I²C Interface Module:

SYSTEM REQUIREMENTS

- Windows Operating System (Win98/ME/2000/XP)
- 32 MB RAM (Minimum)
- 2 MB available for disk space

HARDWARE REQUIREMENTS

- 5-Pin Mini-B USB 2.0 cable (sold separately)

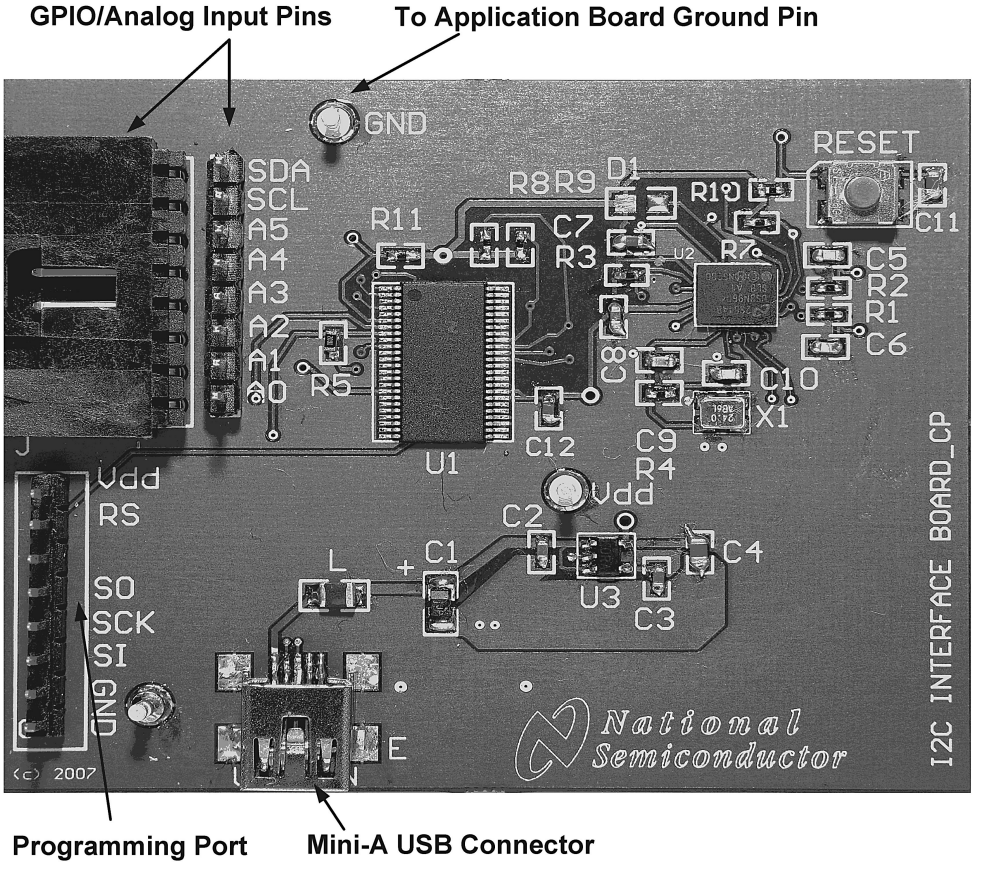

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FIGURE 2. USB I²C Interface Module

Serial Interface and Programming Connectors

SERIAL INTERFACE "J"

The table below shows the pin configuration for the COP8 controller for all interface modes.

TABLE 1.

Pin Name	I2C Board Pin/COP8 Pin	Comment
SDA (Data out)	SDA / 40	R = 2 kΩ (Note 1)
SCL (Clock)	SCL / 39	R = 2 kΩ (Note 1)
Analog Ch. 6/GPIO	A5 / 38	*
Analog Ch. 5/GPIO	A4 / 37	*
Analog Ch. 4/GPIO	A3 / 36	*
Analog Ch. 3/GPIO	A2 / 35	*
Analog Ch. 2/GPIO	A1 / 34	*
Analog Ch. 1/GPIO	A0 / 33	*

Note 1: Must have a pull-up resistor on application hardware for SCL and SDA lines.

Note 2: Do not use any of A5 - A0 pins as a ground connection. Connect both application and I²C grounds together to make a good ground connection between the two boards. (Refer to I²C picture for GND pin.)

ELECTRICAL CHARACTERISTICS OF I²C

The USB I²C board requires 5V from a computer to function correctly. The maximum current that the I²C board will draw from the computer is 500 mA. This I²C board will function within the temperature range of $0°C \leq T_A \leq 70°C$.

For further information about the devices on the I²C board, refer to the following links:

- COP8CBE0 — http://www.national.com/ds/CO/COP8CBE9.pdf
- USBN9694 — http://www.national.com/opf/US/USBN9604.html
- LP2985 — http://www.national.com/mpf/LP/LP2985.html

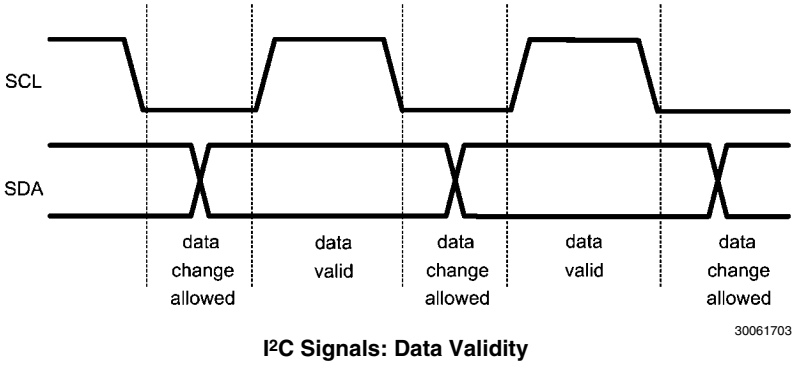
I²C Compatible Interface

I²C SIGNALS

In I²C-compatible mode, the SCL pin is used for the I²C clock and the SDA pin is used for the I²C data. Each of these signals need a pull-up resistor according to I²C specification. The values of the pull-up resistors are determined by the capacitance of the bus (typ. ~2k). See I²C specification from Phillips for further details. Signal timing specifications are according to the I²C bus specification. Maximum frequency is 400 KHz.

I²C DATA VALIDITY

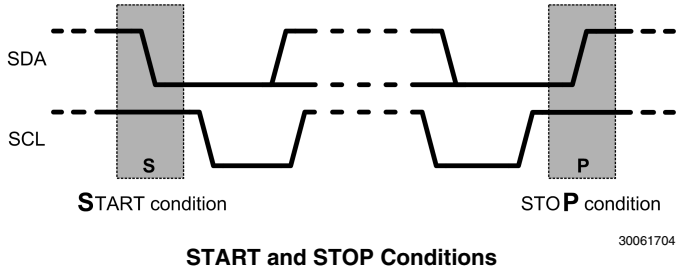
The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.



I²C Signals: Data Validity

I²C START AND STOP CONDITIONS

START and STOP bits signify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.



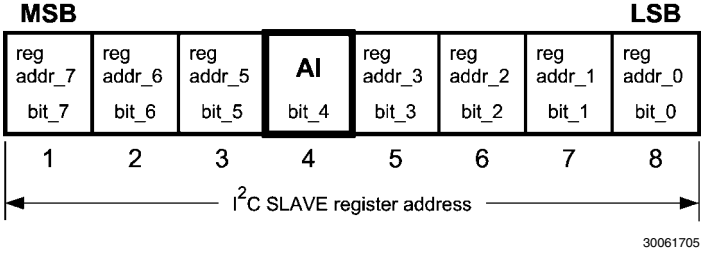
START and STOP Conditions

TRANSFERRING DATA

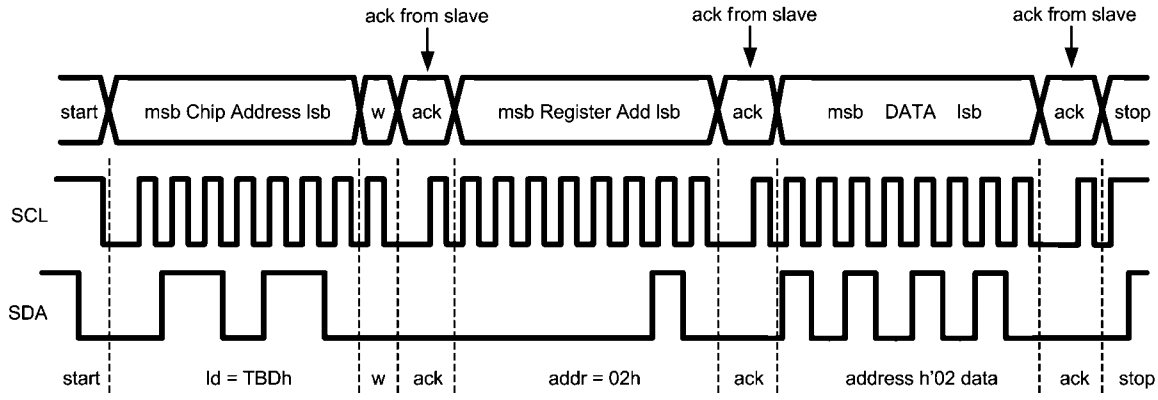
Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data has to be followed by an acknowledge bit. All clock pulses are generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

I²C Chip Address



I²C Write Cycle



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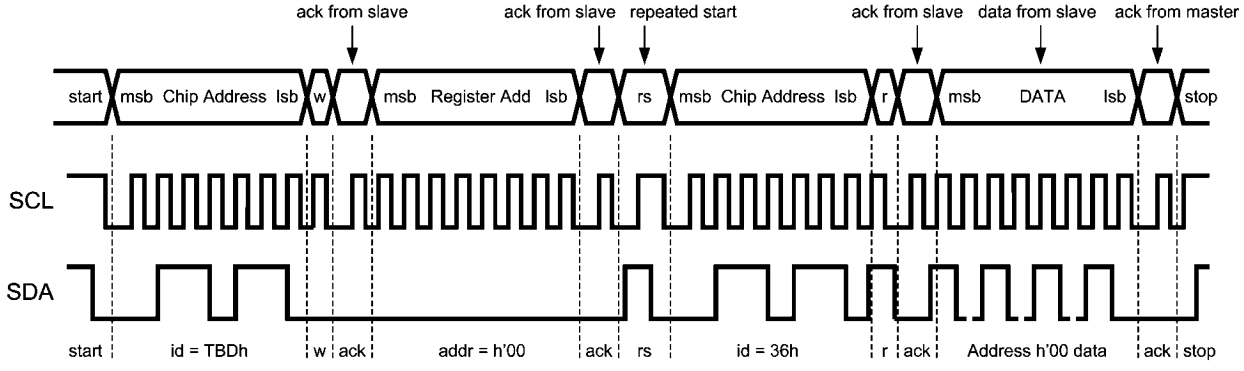
w = write (SDA = '0')
r = read (SDA = '1')
ack = acknowledge (SDA pulled down by either master or slave)
rs = repeated start
id = chip address

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Read Cycle waveform.

I²C Read Cycle



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Notes

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

Products		Design Support	
Amplifiers	www.national.com/amplifiers	WEBENCH	www.national.com/webench
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Clock Conditioners	www.national.com/timing	App Notes	www.national.com/appnotes
Data Converters	www.national.com/adc	Distributors	www.national.com/contacts
Displays	www.national.com/displays	Green Compliance	www.national.com/quality/green
Ethernet	www.national.com/ethernet	Packaging	www.national.com/packaging
Interface	www.national.com/interface	Quality and Reliability	www.national.com/quality
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Tel: 1-800-272-9959

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Email: europe.support@nsc.com
German Tel: +49 (0) 180 5010 771
English Tel: +44 (0) 870 850 4288

National Semiconductor Asia Pacific Technical Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Technical Support Center
Email: jpn.feedback@nsc.com