The LM507X Family of PoE Devices: Frequently Asked Questions (FAQs)

General PoE FAQs

1. How much power can a PD draw?

The IEEE 802.3af specification requires the PSE to supply 15.4W to the cable at 44V minimum (350 mA minimum). The resistance of the 100m cable may be as high as 20Ω. Consequently, 2.45W is lost in the cable which leaves 12.95W for the PD.

It is important to note that the PD load may not consume the entire 12.95W delivered to the PD. Elements within the PD, like the input diode bridges, hot swap MOSFET, IC bias current, and DC-DC converter components, all dissipate power and decrease the power delivered to the load. Most cost-effective power supplies will be approximately 80% efficient, which decreases the deliverable power to about 10.4W. If the input diode bridge consumes 2V x 350mA = 0.7W, the maximum power delivered to the load is 9.7W.

2. Why is it important to have low inrush currents in PoE applications?

The Ethernet cable may be as long as 100m. With two conductors transmitting and two conductors returning the current, the total effective resistance of the cable could be as high as 20Ω, as outlined in the IEEE 802.3 specification. Under-voltage Lockout (UVLO) release for PoE PD applications is typically around 38V nominal. If 400 mA (for example) is pulled from the PSE at the instant of turn on, the PD input voltage will instantaneously drop by 8V. This drop will exceed the UVLO hysteresis and the part will cycle in and out of UVLO. This oscillation will continue until the PSE voltage reaches a level high enough such that the resistive voltage drop no longer crosses the UVLO threshold. If the UVLO threshold is 32V, this would be 32V + 8V = 40V.

If the inrush current is reduced to 150 mA, for example, the total cable voltage drop is reduced to 3V and no oscillation will occur. The IEEE 802.3af specification requires that startup occur cleanly on the first try.

The LM5070 inrush current should be programmed to a lower value. The LM5071 and LM5072 feature inrush current levels that are low by default.

3. How much current can be drawn from the VCC regulator for external use? This FAQ applies to the entire family of PoE devices (including LM5070, LM5071, and the LM5072).

Several internal loads are present including the internal bias current for the DC-DC controller section of the IC, and the external MOSFET gate charging current. The bias current can be as high as 2-3 mA, depending on the operating conditions. Gate charging current can be as high as 10 mA depending on the MOSFET and switching frequency selected. The minimum current limit for the VCC regulator is 15 mA. Consequently, only 2-3 milliamps remain for an external load, like an LED indicator. Any external load on VCC will increase the VIN voltage required to startup the VCC regulator.

4. Why is soft-start so important with PoE devices?

During startup, the DC-DC converter tends to overcompensate for the low output voltage by attempting to operate at maximum duty cycle. This is prevented by the soft-start circuit which slowly increases the peak current of the current mode DC-DC converter. However, if the soft-start capacitor is inadequate and significant current overshoot occurs, the input current to the DC-DC Converter may exceed the current limit threshold of the hot swap MOSFET. If this occurs, the power good condition may be violated which will subsequently shut off the DC-DC Converter, preventing startup. Load conditions during start-up should also be considered when selecting the soft-start capacitor; the regulator should start cleanly over all loading conditions.

5. What happens when a higher voltage auxiliary supply is hot swapped in through the PD front end (through the hot swap MOSFET)?

The main concept behind power good is to ensure the DC-DC converter does not start up until its input capacitors are fully charged, otherwise the current available to charge the capacitors is reduced. This may cause excessive inrush time, high power dissipation, thermal limit, and failure to startup.

Connecting a higher voltage auxiliary supply at the front end presents a new hot swap condition, and unless the power good signal is delayed, the DC-DC converter will be shut down. The internal delay may be too short to be effective. A 5 µs delay is used on the LM5070, the LM5071 has a 100 µs delay, and only the LM5072 allows an external timing capacitor to be added. Even with the power good delay, the DC-DC converter may shut down because of excessive power dissipation or other transient condition. Continuity of power delivery is not guaranteed.

Note that the PSE may remove power if AC or DC Maintain Power Signature (MPS) are not present.

6. Why is the 0.1 µF signature capacitor sometimes placed directly across the PoE input terminals and other times across the internal hot swap MOSFET (from RTN to VEE)? This FAQ does not apply to the LM5070.

By connecting the capacitor across the hot swap MOSFET, any current that charges the capacitor when rear auxiliary is applied is prevented from flowing through the IC.

A rear auxiliary supply can cause the hot swap MOSFET of the LM5072 to turn off (or remain off), and in this case the capacitor must be across the hot swap MOSFET to maintain a low AC impedance at VEE, which is connected to the substrate of the IC.

For the LM5071, the hot swap MOSFET is always on, during PoE or auxiliary operation, so a low impedance path for substrate noise is already present. It may be beneficial to leave it across the input terminals for VIN transient bypassing.

As seen from the PSE, the total capacitance during signature mode is almost identical because the 5 µF (or greater) filter capacitor is in series with the 0.1 µF capacitor. Any time the capacitor is placed across the MOSFET, an additional 0.1 µF capacitor from VIN to RTN should be used for VIN bypassing.

General PoE FAQs (Continued)

7. I need to add differential mode filtering to solve some EMI issues caused by the DC-DC converter, how do I correctly add it to an LM507X based PoE module?

The input filter should be placed between the VIN pin and the input of the DC-DC converter at the transformer. A capacitor is required on both sides of the inductor. The capacitor at the VIN pin is required to provide a path, other than through the IC, for the inductive energy of the filter inductor to re-circulate. Re-circulation occurs whenever there is an abrupt change in the inductor current, such as disconnection of PoE or a load step. The other capacitor, at the input to the DC-DC converter, provides the current pulses to the converter. A 0.1 µF capacitor should be added from VIN to RTN or from VIN to VEE (if not already present) for VIN bypassing.
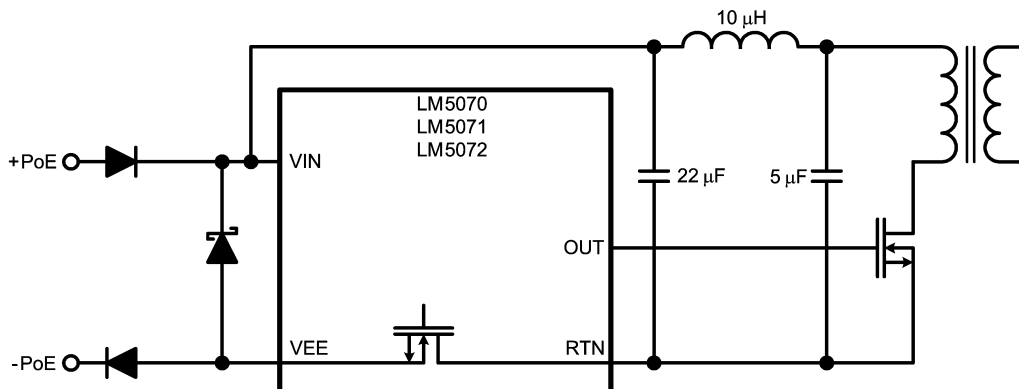
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8. Do I need to ballast the Ethernet transformer currents in my PD?

The PDI load current is shared between the 2 conductors of the twisted pairs. Imbalances in the cable, connectors, and transformer can result in unequal currents flowing. The imbalance will produce a DC offset in the transformer that may cause the transformer to saturate, resulting in data errors. This problem is outlined in the Appendix of the IEEE 802.3af specification.

The condition is usually worse with a short cable, as longer cables provide self ballasting. Most data transformers can tolerate up to 8-12 mA of DC offset current. If a ballast resistor is required, it should be placed in series with each winding at the transformer center tap, with a decoupling capacitor located as close as possible to the transformer to avoid affecting the data performance.

When running higher current levels with the LM5072, a ballast resistor will likely be needed even when using Ether-net transformers that can handle greater than 12 mA of DC offset current. There is currently great debate over this topic, though, and only by careful analysis can one decide that ballasting is unnecessary.

9. How much capacitance is needed on the input to the DC-DC converter?

The IEEE 802.3af requires a minimum of 5 µF, it also specifies a maximum ripple voltage of 150 mV over the frequency range 150 kHz to 500 kHz. A larger value is usually required to reduce the input voltage ripple. The value will depend upon the DC-DC converter design, its switching frequency, and inductor values. To further reduce input ripple and EMI, an input filer can be added using an inductor and a second capacitor (see appropriate FAQ). Be careful in selecting capacitors, as capacitance may drop significantly with variation in voltage, temperature, or time.
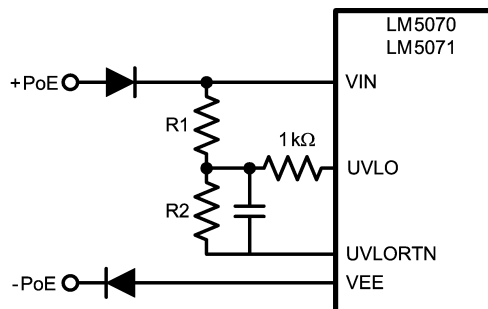
10. How are the UVLO thresholds calculated for the LM5070 and LM5071?

These equations are valid at the pins of the IC, not at the input to the module!

$$V_{IN} \text{ UVLO Release} = \frac{2.0V \times (R1 + R2)}{R2}$$

$$\text{UVLO Hysteresis} = 10\,\mu A \times R1$$

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The easiest way to calculate the UVLO thresholds is to start at the LM5070 or LM5071 and work your way out to the module terminals. The nominal UVLO threshold is 2.0V, with 10 µA of hysteresis current. The hysteresis current is injected into the resistor divider to provide hysteresis. The 1 kΩ resistor can be neglected in the calculation. Use the equations shown above to calculate the UVLO thresholds at the pins of the IC. The final thresholds observed at the module interface are simply the thresholds previously calculated plus two diode drops to account for the input steering diode bridges required in all PoE designs.

General PoE FAQs (Continued)

11. Why are small value resistors placed in series with auxiliary supplies?

Some configurations of auxiliary supply do not have the benefit of hot swap protection. For instance, in rear auxiliary supplies the input voltage is coupled directly to the input of the DC-DC converter. Under such conditions, series resistors limit the inrush current, thus saving board traces and components from extremely high stresses (both current and voltage). The resistors should be made as large as is possible for the application to ensure adequate protection.

12. Can my PoE PD be non-isolated?

Yes, PoE PD's can be non-isolated, but not without serious consideration. The IEEE 802.3af specifications regarding isolated / non-isolated are very confusing, and are in the process of being clarified as of late 2005. It is not the intent of this FAQ to re-write those directives, but it should be known that it is possible.

13. Why aren't the auxiliary supplies inserted before the differential mode filter?

Auxiliary supplies are usually lower voltage supplies that consequently run significantly higher current levels than PoE. The differential mode filter inductor has been sized for 400mA or less, so it would be inappropriate to insert auxiliary at the input to the filter.

FAQ's Specific To The LM5070

1. Why are there small spikes of current on the leading and trailing edges of the inrush current limit when programmed, and are they a problem?

The small spike ($\approx$10 μs) at the beginning is caused because the current programming amplifier on the RCLP pin is not turned on until UVLO release, so a small transient of default current limit is observed until the RCLP amplifier wakes up.

The small spike at the end is the transition from inrush current limit to DC current limit as the internal "power good" signal is asserted. This occurs when the drain to source voltage of the hot swap MOSFET drops below 1.5V.

Neither glitch is an issue because any transient voltage drop on the VIN line is filtered out with the external UVLO capacitor on the UVLO resistor divider. Both of these glitches were removed on both the LM5071 and LM5072 devices.

2. Why can't UVLO be released any lower than 23V?

The LM5070 was not designed for use with low voltage auxiliary supplies, and there is internal logic that disallows classification mode and normal operating mode from occurring at the same time. Therefore, when classification mode is engaged at 23V, UVLO is forced. This cannot be over-ridden no matter what the UVLO pin voltage is, even if it is over the 2.0V threshold. To operate below 23V, use the LM5071 or LM5072 device.

3. Why filter UVLO with an external capacitor?

An internal glitch filter of 10 μs was found to be inadequate in some instances, so external filtering is used to ensure proper operating conditions through transient events. The filter is only needed for the LM5070 and LM5071 devices, as the LM5072 has internal UVLO thresholds and a much longer delay filter (300 μs nominal).

4. The LM5070 datasheet states that VIN can be as high as 1.8V for starting signature mode, will this be a problem for signature startup?

The 2.7V (2.8V at the PSE) minimum allowable signature voltage stated in IEEE 802.3af is quite frankly an oversight in the specification. The high voltage MOSFET in series with the signature resistor has a relatively high turn on voltage that could be as high as 1.8V over process and temperature variation. Because two series input diodes are present, it appears there is not enough voltage left with a 2.7V input to achieve signature mode. In reality, most PSE's place a voltage higher than the bare minimum, so it will not be an issue. The forward drop of the input diodes should be low at such low current levels. If a conservative, extremely robust design is required, simply place the signature resistor directly across the terminals of the input rather than into the switched RSIG pin of the LM5070.

5. Why does the current limit fall off at extreme temperatures, and will this affect my application?

At extreme ambient temperatures, the internal IC bias current drops. This can be observed in both the UVLO hysteresis current and the hot swap MOSFET's current limit, as they are both based on the same internal current. The drop in current limit may limit the power draw in some instances. The minimum PSE output voltage is specified as 44V in the IEEE 802.3af specification. Considering a 6.5V drop in the voltage (325 mA x 20Ω), a maximum of 12.2W (325 mA x 37.5V) may be delivered to the module, which is below the maximum allowable draw of 12.95W. So, modules that are attempting to pull absolute maximum power may have difficulty doing so below 0° and above 85° Celsius. This is outside the range for the majority of PD applications.

The overwhelming majority of installations are on AWG 24 cable or better, and power draw will not be limited in these installations.

6. Many PoE devices have 100V capability, will I be able to protect the LM5070 against transients?

A 58V clamp (SMAJ58A) at the input, along with the required 0.1 μF capacitor, should provide adequate protection if placed near the IC in the layout. Any stray inductance between the protection point on the PC board and the pins of the IC could be a problem, as is the case with any IC bypassing. The LM5072 provides additional margin by having a 100V maximum rating.

FAQ's Specific To The LM5071

1. Why can't UVLO be released any lower than 23V using the UVLO pin?

There is internal logic that prevents classification mode and normal operating mode from occurring at the same time. Therefore, when classification mode is re-engaged at 23V (VIN potential decreasing), UVLO is forced. This cannot be over-ridden no matter what the UVLO pin voltage is, even if it is over the 2.0V threshold. In this case, the AUX pin must be used to force UVLO release. Enabling the LM5071 via the AUX pin automatically disables classification.

2. Many PoE devices have 100V capability, will I be able to protect the LM5071 against transients?

A 58V clamp (SMAJ58A) at the input, along with the required 0.1 μF capacitor, should provide adequate protection if placed near the IC. Any inductance between the protection and the pin of the IC could be a problem, as is the case with any IC bypassing. The LM5072 provides additional margin by having a 100V maximum rating.

Input voltage transients often occur when rear auxiliary supplies are connected. Since auxiliary supplies may not be

FAQ's Specific To The LM5071

(Continued)

current limited, a large inrush current flowing in the auxiliary supply cables will result in voltage ringing at the PDI. A 1 to 2 ohm resistor in series with the auxiliary supply will help filter dangerous transients. See the appropriate FAQ on series limiting resistors for auxiliary supplies.

3. The LM5071 datasheet states that VIN can be as high as 1.8V for starting signature mode, will this be a problem for signature startup?

The 2.7V (2.8V at the PSE) minimum allowable signature voltage state in IEEE 802.3 is quite frankly an oversight in the specification. The high voltage MOSFET in series with the signature resistor has a relatively high turn on voltage that could be as high as 1.8V over process and temperature variation. Because two series input diodes are present, it appears there is not enough voltage left with 2.7V in to achieve signature mode. In reality, most PSE's place a voltage higher than the bare minimum, so it will not be an issue. The forward drop of the input diodes should be low at such low current levels. If a conservative, extremely robust design is required, simply place the signature resistor directly across the terminals of the input rather than into the switched RSIG pin of the LM5071. Alternatively, one could also use Schottky type input rectifier diode bridges.

4. How does the LM5071 allow operation below 25V, isn't that in the classification range?

The LM5071 has a pin called AUX that forces UVLO release and disables classification.

5. Why does the current limit fall off at extreme temperatures, and will this affect my application?

At extreme ambient temperatures, the internal IC bias current drops. This can be observed in both the UVLO hysteresis current and the hot swap MOSFET's current limit, as they are both based on the same internal current. The drop in current limit may limit the power draw in some instances. The minimum PSE output voltage is specified as 44V in the IEEE 802.3af specification. Considering a 6.5V drop in the voltage (325mA x 20Ω), a maximum of 12.2W (325mA x 37.5V) may be delivered to the module, which is below the maximum allowable draw of 12.95W. So, modules that are attempting to pull absolute maximum power may have difficulty doing so below 0° and above 85° Celsius. This is outside the range for the majority of PD applications. The overwhelming majority of installations are on AWG 24 cable or better, and power draw will not be limited in these installations.

6. What is the absolute minimum operating voltage and how do I achieve it?

The minimum VIN operating voltage of the LM5071 is 9.5V at the pins of the IC, so the voltage at the auxiliary supply needs to be one diode drop higher in addition to the drop caused by the series inrush limiting resistor(s). When operating with an auxiliary supply of 14V or less, VCC has to be supplied externally with a diode from the auxiliary supply. Note that operating at low front auxiliary voltages is not permitted with the LM5071 because the thermal protection is disabled when below PoE UVLO release. Auxiliary supplies less than PoE voltages should always be configured for rear auxiliary input, coupled directly to the DC-DC converter.

7. Why isn't thermal limit enabled during auxiliary operation, and what if both PoE and auxiliary are present?

When rear auxiliary is first applied, or during some transient conditions that may occur while the hot swap MOSFET is off,

current may flow backwards through the hot swap MOSFET body diode. This current may interact with the TLIM circuit and prevent the hot swap MOSFET from ever turning on. For this reason, the TLIM is disabled when rear auxiliary is used.

Since front auxiliary and PoE require UVLO release, the condition for disabling the TLIM is when AUX is present, the hot swap MOSFET drain is low (RTN close to VEE), and UVLO is not released (UVLO pin below 2V). If PoE is present when rear auxiliary is applied, the TLIM will remain enabled until the input supply decreases to the PoE UVLO threshold.

8. When do I have to use a diode to elevate VCC with the external auxiliary supply?

A diode is needed when the auxiliary voltage would cause the VIN voltage to be below 14V. This ensures startup of the DC-DC converter.

9. When is a clamp from the VCC pin to the VIN pin needed?

The LM5071 is not designed to carry or block current backwards from VCC to VIN. The clamp is needed to provide a path around the IC. This is needed anytime VCC could be greater than VIN, as can be the case for low voltage auxiliary power (<16V) when an auxiliary winding is used to supply VCC. Note that in this case, a higher series resistor value (≅50 ohms) is needed for the VCC auxiliary winding, as the voltage will be clamped and excess power will be dissipated in this resistor. The VCC auxiliary winding must be allowed to supply the proper cross regulated voltage based on the turns ratio of the power transformer.

10. Why can't the LM5071 be used with a lower voltage front auxiliary supply?

Below UVLO release the thermal protection is disabled, so rear auxiliary should be used. Note that for lower front auxiliary voltages, the current limit of the hot swap MOSFET will restrict the available power to a low level.

11. Why do I have to size the signature resistor as if it is in parallel with the UVLO resistors, and isn't this different from the LM5070?

The LM5070 has a switch that disables the UVLO resistors during signature. The LM5071 has UVLORTN internally grounded such that the UVLO divider is always in parallel with the signature resistor. The LM5072 has an internal signature resistor.

12. Why does the LM5071 auxiliary interface use a PNP transistor for signaling the AUX pin instead of just a resistor?

The PNP is used to detect a voltage at the auxiliary input by signaling a current to the AUX pin. The auxiliary supply references the RTN pin of the IC, while the AUX input of the IC detects a voltage relative to VEE. Consequently, the PNP transistor is used to translate the signal from one that is RTN referenced to another that is VEE referenced.

13. Why are the values of the resistor divider on the AUX pin important?

The AUX pin is pulled up by a PNP transistor whose collector-base junction is reverse biased when the auxiliary source is not present. Any significant leakage across this junction could incorrectly signal the AUX pin to change the state of the device. Although the threshold for turn on is 2.5V on the AUX pin, a threshold of about 1V signals the LM5071 to exit signature mode. The pull down resistor on the AUX pin prevents this false signaling. It should be made low enough such that any leakage prevents the AUX pin from exceeding 0.5V. A small signal (but high voltage), low leakage PNP should be used. High ambient temperatures will

FAQ's Specific To The LM5071

(Continued)

increase the leakage (leakage doubles about every 10° Celsius). It should not be assumed that the PNP transistor is off even when the hot swap MOSFET is off and RTN/ARTN are near VIN. Bias currents in the LM5071 sink enough current to turn the PNP transistor on, provided enough reverse leakage is present from the power feeding diode. Reducing the resistor from base to emitter, along with a reduction in AUX pin pull down resistance, will prevent false signals from the PNP by increasing the amount of current required to signal the AUX pin.

14. Can I filter the AUX signal with a capacitor, either at the input PNP or the AUX pin?

No, this may cause adverse operation because of the delay introduced by the capacitor. Internal filtering will ignore momentary glitches on the pin of less than 5 μs. The pin should be pulled well above the threshold for high noise immunity.

15. Is the AUX pin reverse protected?

No, if full reverse polarity protection is desired on the auxiliary input, an additional series diode is required to prevent reverse current flow to the AUX pin.

FAQ's Specific to the LM5072

1. How does the LM5072 allow operation below 25V, isn't that in the classification range?

The LM5072 has pins called FAUX and RAUX that are used to force an enable of the device and disable classification.

2. What are the limitations of front auxiliary power?

The LM5072 has a programmable DC current limit that can be programmed up to 800 mA. This makes lower voltage front auxiliary supplies practical. The limitation is for power dissipation in the IC, which will depend strongly on the thermal characteristics of the circuit board design and the ambient temperature of the operating environment. See the appropriate FAQ for a discussion of the minimum voltage that can be used.

3. What is auxiliary dominance?

Auxiliary dominance is used when power is to be off loaded from the PSE through the use of rear auxiliary power. This mode forces the hot swap MOSFET off, disconnecting the PSE. The PSE may then detect a loss of Maintain Power Signature (MPS) and remove PoE power. Note that if the PSE does not implement DC Maintain Power Signature, power may not be removed because the AC Maintain Power Signature still remains with auxiliary operation. No power is being drawn from the PoE supply, even if it remains present. This configuration is only an option when auxiliary is applied directly to the DC-DC converter (rear auxiliary).

When auxiliary power is present, the PSE will not observe a valid detection signature. When auxiliary power is removed there will be a delay before the PSE recognizes the PDI and reapplies power.

Note, auxiliary non-dominance does NOT imply PoE dominance! See the appropriate FAQ on PoE dominance.

4. Why is PoE dominance so difficult to achieve?

PoE dominance requires that the PoE voltage be higher than the auxiliary voltage. When operating from an auxiliary supply and PoE is applied, the voltage at VIN (across the filter capacitor) must be charged from the auxiliary voltage to the PoE voltage while the DC-DC converter is operating. When the auxiliary voltage is much less than PoE voltage, suffi-

cient current will likely not be available from the PSE, or the current limit of the powered device interface may be reached. This is because the current is much higher at low voltages than at high voltages, in order to supply the same load at the DC-DC converter output.

Even if there is sufficient current available, the time required to charge the filter capacitor may exceed the power good delay, or the IC power dissipation may be exceeded. Exceeding the power good delay will cause the DC-DC converter to be turned off. A thermal limit will turn off the hot swap MOSFET until the IC has cooled sufficiently.

A further problem is caused by the common substrate of the PD interface and the PWM controller, and the body diode of the hot swap MOSFET, which prevents signature detection when auxiliary power is present. Additional circuitry would be required in order for the PSE to be able to observe the signature.

These problems can be solved by using a two stage power conversion where auxiliary power is diode connected with a stepped down output from PoE. This combined voltage becomes the input to an additional DC-DC converter on the secondary side, that provides the regulated high current output. PoE will dominate over the auxiliary supply provided the stepped down voltage is greater than the auxiliary input voltage.

5. What is the absolute minimum operating voltage and how do I achieve it?

When VCC is supplied from VIN the minimum voltage is 14.5V between VIN and RTN. Note that an external load on the VCC regulator may increase this dropout voltage. By diode connecting the rear auxiliary supply to VCC, the minimum voltage is 9V (from VIN to RTN) at the pins of the IC. If an auxiliary winding is used to supply VCC, this may take over once the DC-DC converter has started up. Be careful to include diode and series current limiting resistor voltage drops when calculating the minimum operating voltage.

6. Why is a clamp from the VCC pin to the VIN pin, as seen in some LM5071 designs, no longer needed with the LM5072?

The LM5072 has a blocking 'diode' in series with the VCC output to prevent reverse current flowing from VCC to VIN, this allows VCC to be higher than VIN by up to 7V without using an external clamp.

7. Why does the LM5072 increase the default DC current limit when front auxiliary in inserted?

When the front auxiliary voltage is less than normal PoE voltage, more current is needed to provide the same power. For this reason, the current limit is increased. The current limit is not increased if there is UVLO release (VIN above 38V), or the DC current limit is programmed. A programmed DC current limit may be considered a hard limit in that it is independent of operating mode.

8. Why does the LM5072 increase the default DC current limit when "power good" is de-asserted?

Inserting front auxiliary causes a new hot swap condition if the auxiliary voltage is higher than the PoE voltage, causing de-assertion of power good. Increasing the current limit provides additional current for charging the filter capacitors while simultaneously supplying the load. This reduces the power good delay required, and hence the power dissipation in the hot swap MOSFET. The current limit is increased only if the DC-DC converter is running and the DC current limit is not programmed.

FAQ's Specific to the LM5072

(Continued)

9. What is auxiliary non-dominance?

Auxiliary non-dominance is used when rear auxiliary provides backup power. This requires the auxiliary voltage to be less than PoE voltages. This mode will only force the hot swap MOSFET off if the DC-DC converter is not already running, as is the case when there is no PoE power. When PoE power is removed, the auxiliary supply will take over the load without an interruption of power. If the auxiliary voltage is higher than UVLO then the hot swap MOSFET will remain on, otherwise it will be turned off. Note that auxiliary non-dominance is not the same as PoE dominance, see the appropriate FAQ for a discussion of the PoE dominant configuration.

10. Why are 24.9 kΩ resistors needed across the inputs of the auxiliary supplies (both front and rear)?

As noted in the LM5072 datasheet, the power feeding diodes used on the auxiliary inputs may leak reverse current when the auxiliary supply is not connected. The resistors provide a path for this current so that it does not falsely signal the ICL_FAUX or RAUX pins. Also, the selection of the series diode that pulls up the ICL_FAUX pin is very important. Leakage of this diode "looks like" inrush current programming current. Any leakage will add to the inrush current programming current that is pulled from the ICL_FAUX pin, and will corrupt ICL_FAUX programming. Inrush current is not considered programmed until the current pulled from the pin is greater than a few microamperes.

11. Are the ICL_FAUX and RAUX pins reverse protected?

No, if full reverse polarity protection is desired on the auxiliary inputs, additional series diodes are required to prevent reverse current flow for both the ICL_FAUX and RAUX pins.

Glossary Of Terms As Used In This Document

1. **AUX**, an input to the LM5071 to indicate presence of auxiliary power. Where power is applied either before or after the hot swap MOSFET.

2. **Auxiliary dominance**, a rear auxiliary supply that dominates over the PoE even if the auxiliary voltage is lower or is applied after PoE power.

3. **Auxiliary non-dominance**, a rear auxiliary supply that only dominates over the PoE if the auxiliary voltage is higher or is applied first. This is not the same as PoE dominance.

4. **Auxiliary winding**, an extra winding on the DC-DC converter transformer that supplies VCC, in order to improve efficiency.

5. **DC current limit** (DCCL) The current available to supply the load once the filter capacitor is charged and the DC-DC converter is enabled.

6. **DC-DC converter**, a switching regulator supplying a load from VIN. The controller for this converter is built into the IC.

7. **Front Auxiliary, ICL_FAUX, FAUX, or Front AUX**, the configuration where auxiliary power is applied before the hot swap MOSFET (as opposed to rear auxiliary). Also, an input to the LM5072 to indicate the presence of front auxiliary power.

8. **Filter capacitor**, the capacitor required at the input of the DC-DC converter.

9. **Hot swap MOSFET**, the current limited power MOSFET internal to the IC.

10. **Inrush current limit** (ICL) The current available to charge the filter capacitor when power is first applied.

11. **PD interface**, refers to the hot swap MOSFET and the circuits that present valid signature, classification, and under-voltage lockout conditions to the PSE.

12. **PD**, Powered Device, refers to the complete device connected to PoE, including the PDI, DC-DC converter, and loads.

13. **PoE**, Power over Ethernet, refers to power originating from the Ethernet cable.

14. **PoE dominance**, is where PoE sources power even when auxiliary power is present. This provides the best continuity of power but is difficult to implement.

15. **"Power good"**, is a signal internal to the IC that is asserted when the hot swap MOSFET is fully on. A delayed version of this signal controls the DC-DC converter.

16. **PSE** Power Sourcing Equipment, controls and sources the power on the Ethernet cable. Functions include signature detection and classification.

17. **Rear Auxiliary, RAUX, or Rear AUX**, the configuration where auxiliary power is applied directly to the DC-DC converter (as opposed to front auxiliary). Also, an input pin on the LM5072 IC used to indicate the presence of rear auxiliary power.

18. **UVLO release**, de-assertion of the under-voltage lockout (UVLO) signal when VIN exceeds 38V (VIN rising). It may be programmed on the LM5070 and LM5071 devices.

19. **UVLO, Under-Voltage Lockout**, this signal is asserted when VIN is below 32V (VIN falling). It may be programmed on the LM5070 and LM5071 devices.

Notes

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