Thermal Performance of the LM3404/04HV in SO-8 and PSOP-8 Packages

National Semiconductor
Application Note 1629
Chris Richardson
May 2007

Introduction

The LM3404/04HV is a buck-regulator designed for driving high powered LEDs at forward currents of up to 1.0A. LED drivers often experience thermal conditions that are extreme even by the standards of switching converters. For example, LED drivers are often placed on the same metal-core PCB (MCPCB) as the LEDs themselves. At 1.0A, a single-die white LED can dissipate more than 3W. The temperature of the MCPCB can easily reach 60°C or more. Even when the driver is placed on a separate PCB, the combination of high power dissipation, small, enclosed spaces, and little-to-no air flow create high ambient temperatures and even higher junction temperatures.

Thermal conditions for integrated (MOSFET on-board) LED drivers are made worse by the high duty cycles of LED drivers. For applications that use multiple LEDs, as many LEDs as possible are placed in series to match the current and voltage limitations of the regulator regulator. The result is that output voltage is just below the input voltage. A voltage regulator that provides a 5V output from a 24V input has a duty cycle of 21%, meaning that the internal MOSFET is on for 21% of the time. In contrast, a 24V input is often used to drive five series-connected white LEDs, and at 3.5V each this gives an output voltage of 17.5V, forcing the MOSFET to conduct for 73% of the time.

The first part of this application note will explore the performance of the LM3404HV in a high current, high input voltage, high duty cycle application typical of many LED drivers, using lab-tested thermal performance results and simulations. The industry standard SO-8 package and the pin-for-pin compatible PSOP-8 package with an exposed thermal pad (also called a die-attach paddle, or DAP) will be compared to help the user estimate the die temperature under various conditions, and determine which package is best for their application.

The second part of this application note uses the power dissipation calculated in the first section to estimate the LM3404HV's die temperature under two typical configurations of the LEDs relative to the LED driver. The first case is for the LM3404HV mounted on a separate PCB that is connected to the LEDs by a wiring harness. This case assumes an ambient temperature influenced by the heating of the LEDs, but no direct heating of the PCB by the LEDs themselves. The second case assumes the LM3404HV is mounted to the same MCPCB as the LEDs themselves. In this configuration the temperature of the MCPCB has a much stronger influence over the LM3404HV die temperature than the ambient temperature, and the tests assume a fixed MCPCB temperature instead of a fixed ambient temperature.

Test Circuit

The test circuit uses the LM3404HV to drive ten series-connected 3W white LEDs from an input voltage of 48V ±5%. The total forward current, I_F, is 1A ±5% at a typical forward drop of 36V (in thermal equilibrium). Output current ripple is 70 mA_{P-P} or less. Switching frequency is 550 kHz ±10% and the circuit is surge protected up to 60V. A complete BOM is listed at the back of this document, and performance waveforms are given in Application Note AN-1585. The schematic is shown in *Figure 1*.

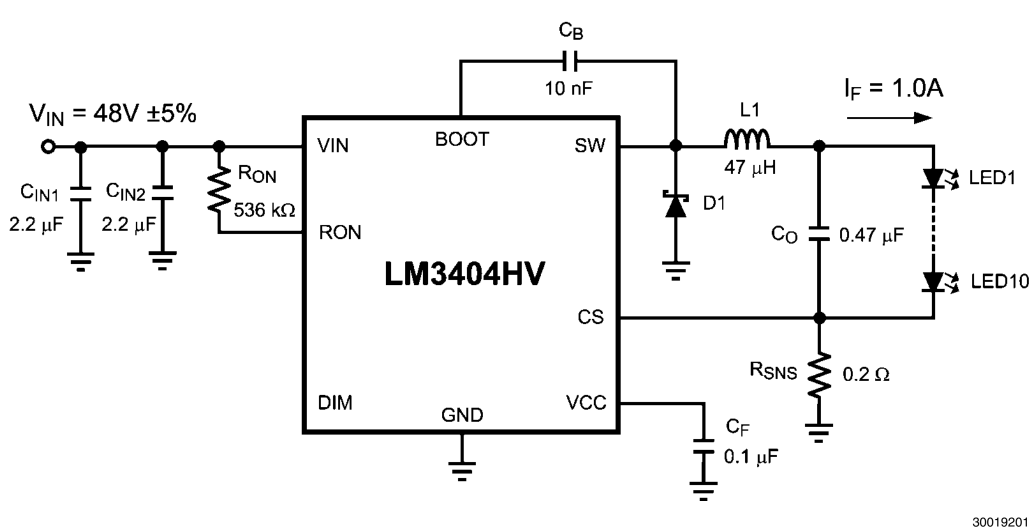


FIGURE 1.

Thermal Performance of the LM3404/04HV in SO-8 and PSOP-8 Packages AN-1629

Test PCB

The test PCB for this application note is the LM3402/04 PSOP-8 Evaluation board. The board measures 1.95” by 1.25”, with 2 layers of 1oz copper and 62mil FR4. To obtain best thermal performance, most of the top layer and the entire bottom layer are composed of large copper areas (shapes). These areas act as heatsinks for the LM3404HV. Of special importance is the pad and thermal via arrangement that connects the DAP of the PSOP-8 package to the ground plane on the bottom layer. *Figure 2* shows a detail of the pad, which is the recommended layout for best thermal performance. The LM3404HV in PSOP-8 can be used on a standard SO-8 footprint, and the LM3404HV in SO-8 can be used on the PSOP-8 Evaluation Board, however neither of these options take advantage of the enhanced thermal performance of the PSOP-8 when properly soldered to a thermal pad connected to a large (1 square inch or more) copper area. Plots of the PCB layers are shown at the end of this document.

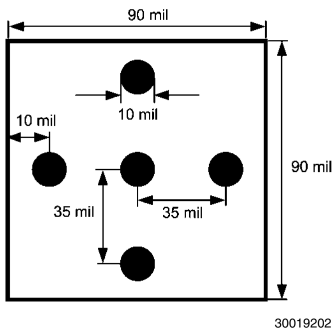


FIGURE 2. PSOP-8 Pad and Thermal Via Layout

Power Dissipation

Power dissipation inside the LM3404HV can be divided into three types: conduction (I^2R) loss, gate charge loss, and switching loss. For each calculation the maximum, worst-case values have been used. Duty cycle, D, is 0.75. The MOSFET R_{DSON} is 0.75Ω, gate charge, Q_G is 6 nC, and the rise are fall times, t_R and t_F, are 20 ns each.

Conduction loss, P_C, in the internal MOSFET

$$P_C = (I_F \times D)^2 \times R_{DSON} = (1.0 \times 0.75)^2 \times 0.75 = 420 \text{ mW}$$

Gate charging and VCC loss, P_G, in the gate drive and linear regulator:

$$P_G = (I_{IN\text{-}OP} + f_{SW} \times Q_G) \times V_{IN}$$
$$P_G = (675 \times 10^{-6} + 550000 \times 6 \times 10^{-9}) \times 48 = 191 \text{ mW}$$

Switching loss, P_S, in the internal NFET:

$$P_S = 0.5 \times V_{IN} \times I_F \times (t_R + t_F) \times f_{SW}$$
$$P_S = 0.5 \times 48 \times 1.0 \times (40 \times 10^{-9}) \times 550000 = 528 \text{ mW}$$

The total power dissipation inside the LM3404HV is then:

$$P_D = P_C + P_G + P_S = 1.14\text{W}$$

Thermal Calculations

The LM3404HV has a maximum operating junction temperature (T_J) of 125°C. Calibrated testing of the LM3404HV in both the SO-8 package (NSID LM3404HVMA) and PSOP-8 (NSID LM3404HVMR) was performed using the actual PSOP-8 evaluation PCB. The results for junction-to-ambient thermal resistance (θ_{JA}) in °C/W are summarized below:

Package	0.5W	1.0W	1.5W
SO-8	102	99	N/A
PSOP-8	50.9	49.6	48.4

To match the expected application conditions, all tests were performed with no air flow. Data for the SO-8 package at 1.5W is not available because the final T_J exceeded 125°C. θ_{JA} is as much a property of the PCB as it is of the semiconductor chip. The top layer of the PSOP-8 Evaluation board is approximately 75% copper, and the bottom (accounting for holes and traces) is approximately 90%. The estimated total copper area is therefore (0.75 + 0.9) x (1.25” x 1.95”) = 4 square inches.

With the power dissipation and thermal resistance data the maximum ambient operating temperature can be predicted or, given the ambient operating temperature, a decision can be made as to the proper package for the LM3404HV.

Maximum ambient operating temperature, $T_{A\text{-}MAX}$, can be determined with the following equation:

$$T_{A\text{-}MAX} = T_{J\text{-}MAX} - P_D \times \theta_{JA}$$
$$T_{A\text{-}MAX} \text{ (SO-8)} = 125 - 1.14 \times 99 = 12°\text{C}$$
$$T_{A\text{-}MAX} \text{ (PSOP-8)} = 125 - 1.14 \times 50 = 68°\text{C}$$

It is clear from the calculations that the PSOP-8 package must be used in this high dissipation application.

As an alternative, if the ambient temperature is known, then the die temperature of the LM3404HV can be predicted by re-arranging the previous equation:

$$T_J = T_A + P_D \times \theta_{JA}$$

For example, if the ambient temperature inside an enclosure with high power LEDs reaches 60°C, then the two package options can again be evaluated:

$$T_J \text{ (SO-8)} = 60 + 1.14 \times 99 = 173°\text{C}$$
$$T_J \text{ (PSOP-8)} = 60 + 1.14 \times 50 = 117°\text{C}$$

Again, the results show that the SO-8 package will not be able to keep the junction temperature within specification limits.

Predicting Thermals with FR4

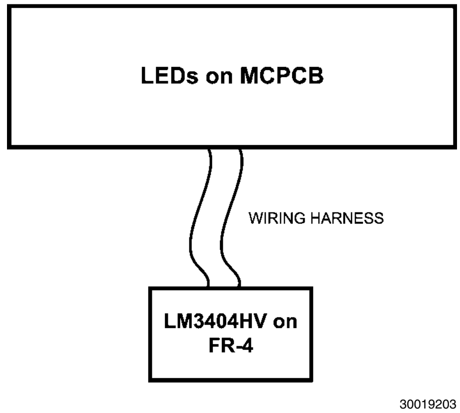


FIGURE 3. System Diagram 1

Using finite element analysis, the thermal performance of the LM3404HV in PSOP-8 and SO-8 was simulated with three different sized PCBs. These simulations assumed an ambient temperature of 22°C, a power dissipation of 1W, and a 2-layer PCB comprised of 1oz copper on top and bottom, separated by 62mil of FR4. The results are listed below:

θ_{JA} (°C/W)	PSOP-8	SO-8
1.25" x 1.95" (Eval Board)	55.1	104.8
1" x 1" (Typical Case)	73.0	120.8
0.5" x 0.5" (Worst Case)	240.2	263.7

There is good correlation between the test results and simulation results for the Evaluation Board Case. The strong influence of the PCB size can be seen by comparing the results from the demo board to those of the Typical and Worst Cases. Without enough copper area to spread and dissipate heat, the advantages of the exposed pad are reduced, and even the PSOP-8 package will be limited to low power, low ambient temperature applications.

Predicting Thermals with Metal-Core PCB

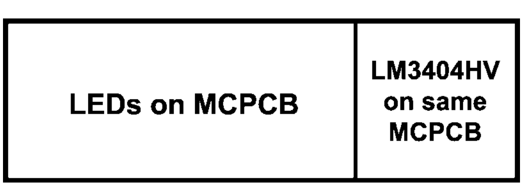


FIGURE 4. System Diagram 2

Finite element analysis was again used to simulate the performance of the LM3404HV when dissipating 1W in PSOP-8 and SO-8 packages on a 1" square section of MCPCB with the following composition:

Material	Thickness (mil)	Thermal Conductivity (W/m-K)
Metal Core (6061-T6 aluminum)	40	167
Insulator Material	3	2.4
Copper Traces (75% coverage)	1.4	377

To attain typical operating conditions, the 1" square section containing the LM3404HV was assumed to be part of a larger MCPCB measuring 1" x 6". The other 5 square inches contained 5 high power LEDs, and it was assumed that they heated the entire board to a uniform temperature, TBD, of 50°C (representing a large heatsink) and 75°C (representing a smaller heatsink.) The results for thermal impedance from the board to the LM3404HV die, Ψ_{JBd}, are listed below:

Ψ_{JBd} (°C/W)	T_{BD} = 75°C T_A = 60°C	T_{BD} = 75°C T_A = 45°C	T_{BD} = 50°C T_A = 40°C	T_{BD} = 50°C T_A = 30°C
SO-8	70.5	69.2	71.4	70.5
PSOP-8	9.8	9.2	10.5	10.1

The parameter Ψ_{JBd} can be used to calculate the LM3404HV junction temperature using the following equation:

$$T_J = \Psi_{JBd} \times P_D + T_{BD}$$

Alternatively, Ψ_{JBd} can be used to determine the maximum tolerable board temperature by working back from a $T_{J\text{-}MAX}$ of 125°C:

$$T_{BD\text{-}MAX} = 125 - \Psi_{JBd} \times P_D$$

Two main conclusions can be drawn from the results. First, the thermal impedance has little dependence on the board temperature or the ambient temperature, and instead depends highly on the package used. Second, the PSOP-8 package is again far superior to the SO-8 package when the DAP is soldered to a mass with low thermal impedance, such as an MCPCB.

Conclusion

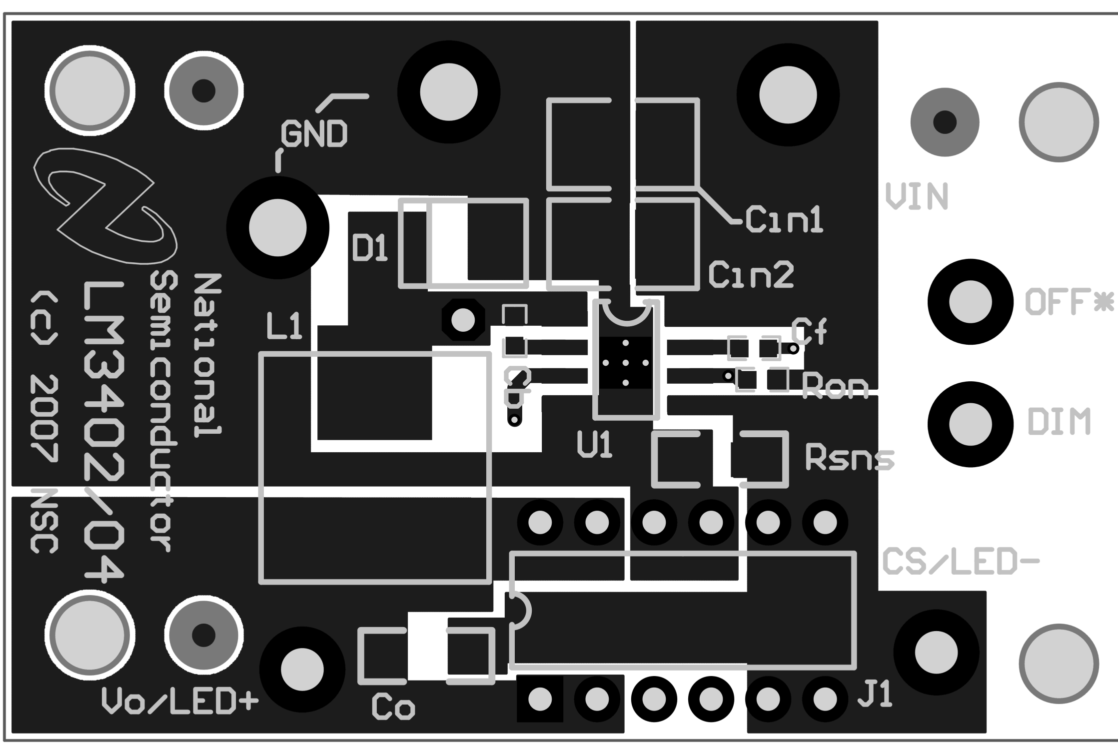
The higher the ambient temperature, the board temperature, and the power dissipation of the LM3404HV, the more likely that the PSOP-8 package will be required in order to maintain the junction temperature below T_{J-MAX}. In addition, as the thermal stress becomes greater and the PCB area becomes smaller, the more likely that the LM3404HV will need to be mounted on an MCPCB.

The results presented in this application note are intended to guide the user in selecting the correct package and configuration for a high powered LED driver such as the LM3404HV. The general trends observed are valid for other applications, but will not correlate directly to other circuits or applications.

Bill of Materials

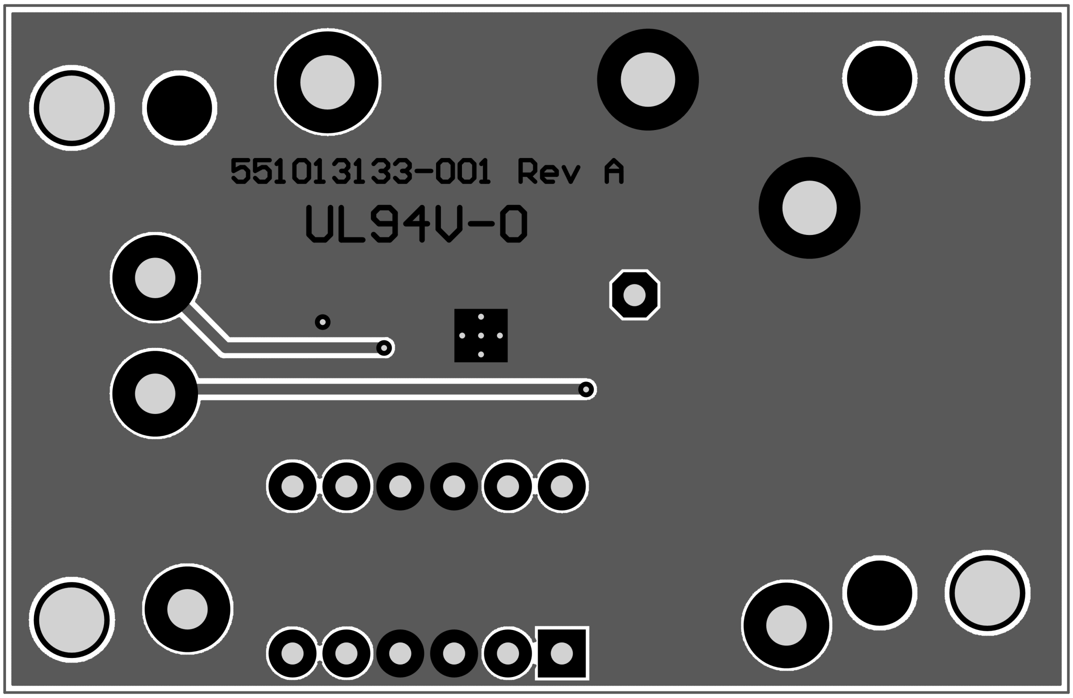
ID	Part Number	Type	Size	Parameters	Qty	Vendor
U1	LM3404HVMR	LED Driver	PSOP-8	75V 1A	1	NSC
L1	SLF10145T-470M1R4	Inductor	10.0 x 10.0 x 4.5mm	47µH, 1.4A, 0.1Ω	1	TDK
D2	CMSH2-60	Schottky Diode	SMB	60V 2A	1	Central Semi
Cf	VJ0603Y104KXXAT	Capacitor	0603	100nF 10%	1	Vishay
Cb	VJ0603Y103KXXAT	Capacitor	0603	10nF 10%	1	Vishay
Cin1, Cin2	C4532X7R2A105M	Capacitor	1812	2.2µF 100V	2	TDK
Co	C3216X7R2A474M	Capacitor	1206	0.47µF 100V	1	TDK
Rsns	ERJ8BQFR20V	Resistor	1206	0.2Ω 1%	1	Panasonic
Ron	CRCW06035363F	Resistor	0603	536kΩ1%	1	Vishay

PCB Layout



30019205

Top Layer



30019206

Bottom Layer

Notes

National Semiconductor Americas Customer Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

National Semiconductor Europe Customer Support Center
Fax: +49 (0) 180-530-85-86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +49 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor Asia Pacific Customer Support Center
Email: ap.support@nsc.com

National Semiconductor Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560