# LM5115/5025A Evaluation Board

National Semiconductor
Application Note 1368
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## Introduction

The LM5115/LM5025A evaluation board provides the design engineer with a secondary side post regulated (SSPR) output from an existing Active Clamp Forward topology. Information on the LM5025A active clamp evaluation board can be found in Application Note AN-1345. Note that other types of isolated power converters (e.g. push-pull, half-bridge, and full-bridge) can be used in the place of the LM5025A active clamp forward converter to drive the LM5115 AC evaluation board.

The evaluation board specifications are:

- Input voltage: 36V to 72V, 48V nominal on LM5025A
- Output voltage Main: 3.3V nominal
- Output current Main: 0 to 30A
- Current limit Main: ≅30A
- Output voltage Secondary: 2V
- Output current Secondary: 0 to 9A
- Current limit Secondary: ≅9A
- Measured efficiency on secondary only: 98% at 36V, Iload = 1A, 93% at 48V, Iload = 4A
- Load regulation: 2mV change from 1A-7A, 36V < Vin < 72V
- Size: 2.0 x 1.125 x 0.375 in.

The printed circuit board consists of 4 layers of 2 oz copper on FR4 material, with a thickness of 0.050 in. It is designed for continuous operation at rated load with a minimum airflow of 200 LFPM.

## Theory of Operation

The LM5115 controller contains all of the features necessary to implement multiple output power converters utilizing the Secondary Side Post Regulation (SSPR) technique. The SSPR technique develops a highly efficient and well regulated auxiliary output from the secondary side switching waveform of an isolated power converter.

Synchronization of the LM5115 comes from the main pulsed signal of the transformer secondary winding. Resistor R2 and R4 sense the pulsing signal to form an internal synchronization signal and an internal current to charge the RAMP of the LM5115. The LM5115 controls the buck power stage with leading edge pulse width modulation (PWM) to hold off the high side driver until the necessary volt*seconds is established for regulation. Representative waveforms are shown in Figure 4.

Bias to the part comes from a rectified pulse signal. Note that the pulse signals vary from 6Vpp to 12Vpp, with Vin varying from 36V to 72V, respectively. Therefore, the Vcc regulator will not regulate at 7V until the peak to peak voltage is slightly higher than 7.5V (accounting for the diode drop to the bias). The intention was to show that with non-regulation on Vcc the LM5115 is still capable of providing the secondary voltage of 2V from the main 3.3V. Adaptive deadtime control delays the top and bottom drivers to avoid shoot through currents (Figure 7 & 8).

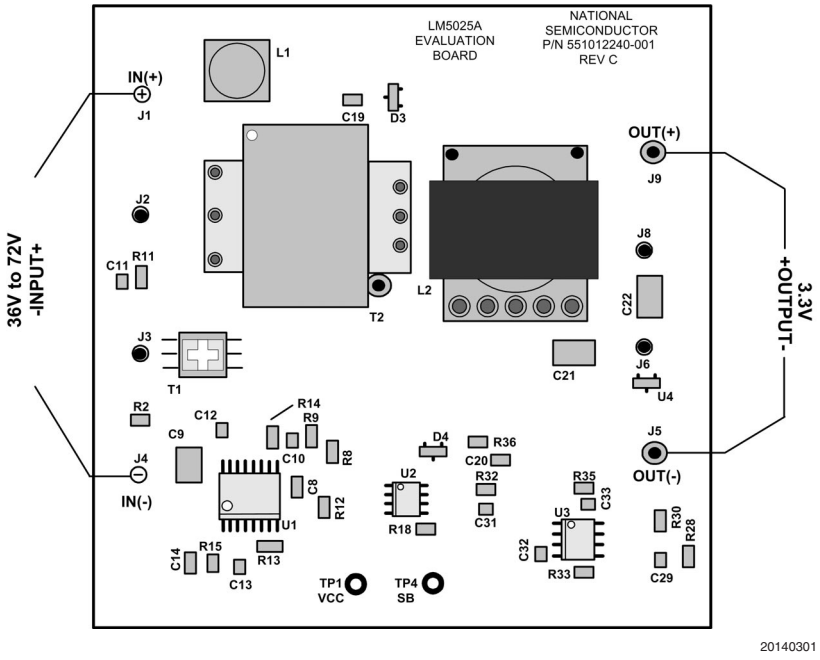



**FIGURE 1. LM5025A Evaluation Board Top Side**



## Theory of Operation (Continued)

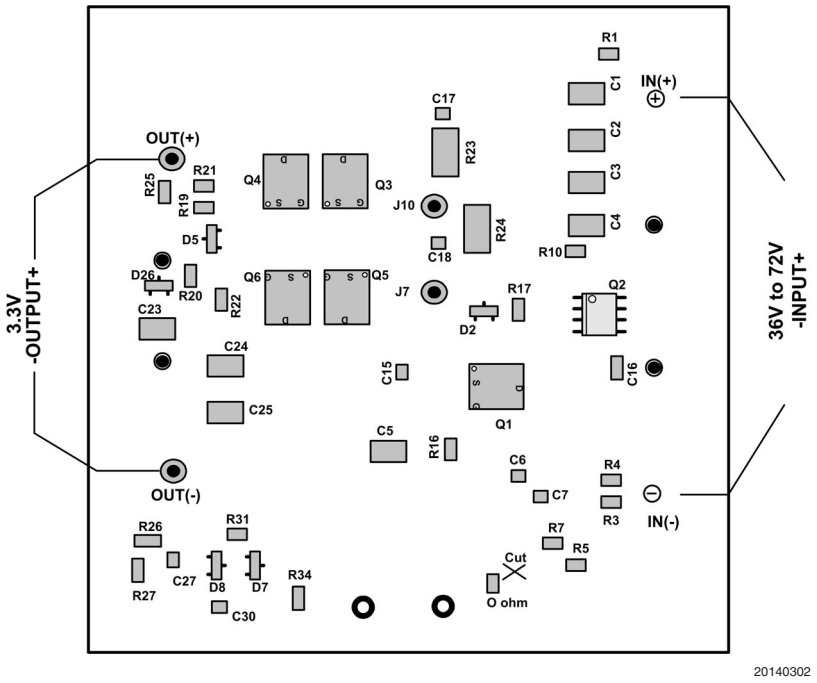



**FIGURE 2. LM5025A Evaluation Board Bottom Side**

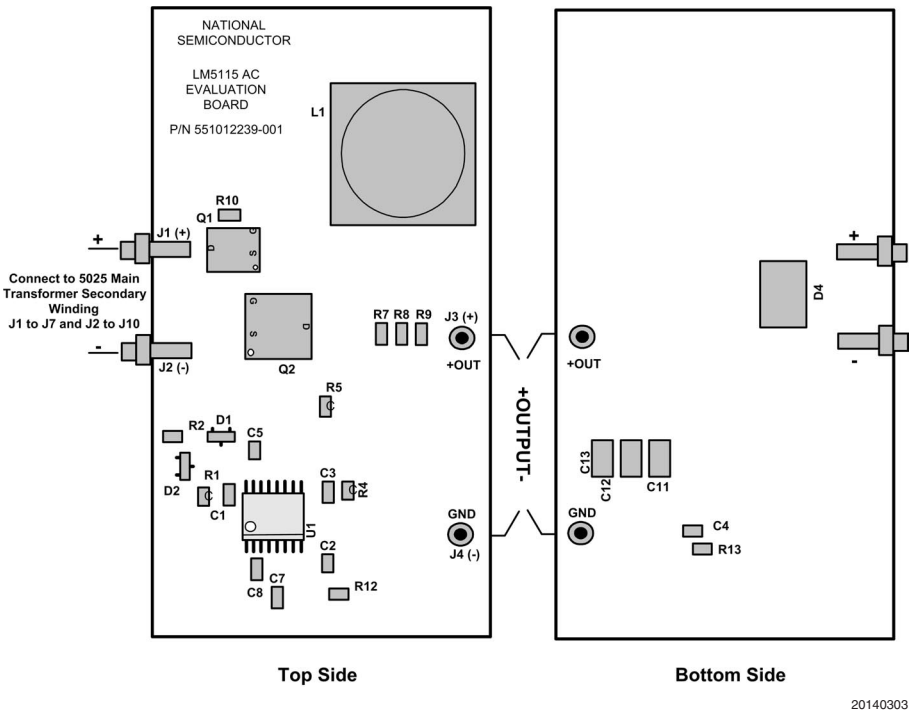



**FIGURE 3. LM5115 Evaluation Board**

## Board Layout and Probing

Figures 1-3 show the board layout, main components, and critical probe points for testing the LM5115 AC mode evaluation board in conjunction with the LM5025A board. The following notes should be considered prior to applying power to the board:

1. Main input power (36V to 72V) is applied to points J1 and J4 of the LM5025A board, connected to VIN and GND respectively.
2. The main current carrying components (LM5115 board: L1, Q1, and Q2; LM5025A board L2, Q3-Q6) will be hot to the touch at maximum load current. USE CAUTION. When operating at load currents in excess of 5A the use of a fan to provide forced air flow **IS NECESSARY**.
3. The diameter and length of the wire used to connect the load is important. To ensure that there is not a significant voltage drop in the wires, a minimum of 14 gauge wire is recommended.

## Board Connections/Start-Up

The input power connections are made to terminals J1 (+) and J4 (-) of the LM5025A evaluation board. The input source must be capable of supplying the load on both the output of the LM5025A board and LM5115 board. The input to the LM5115 is supplied by the secondary winding of the LM5025A board. J7 (LM5025A) connects to J1 (LM5115) and J10 (LM5025A) connects to J2 (LM5115) (see Figure 1-3). The main load is connected to terminals J9 (+) and J5 (-) for the LM5025. Terminals J3 (+) and J4 (-) are the load connections for the LM5115. Before start-up, a voltmeter should be connected to the input terminals and to the output terminals. The input current should be monitored with an ammeter or a current probe. Soft-start provided by the LM5115 will insure that the output rises with a smooth turn on without overshoot (Figure 12). The LM5115 evaluation board will operate in the continuous conduction mode even with a light or no load (Figure 4).

## Performance LM5115 Secondary Side Post Regulator

Performance of the LM5115 evaluation board can be seen in the following figures:

1. Power Conversion Efficiency (Figure 5 & 6)
2. Gate Delays (Figure 7 & 8)
3. Short circuit response (Figure 9)
4. Step Load Response (Figure 10 & 11)
5. Startup and Shutdown Response (Figure 12 & 13)
6. Ripple Voltage (Figure 14)
7. Load Regulation (Figure 15)
8. Secondary Closed Loop Frequency Response (Figure 16)

## $V_{CC}$

The LM5115 produces a LDO 7V regulated output (VCC) that can supply up to 40mA of DC current. The VCC regulator supplies power for the high current gate drive for the low side MOSFET and the bootstrap capacitor of the high side MOSFET driver.

## Current Limit Operation

Inductor current is sensed through the parallel resistances of R7, R8, and R9. The resistor values are designed for a current limit of ~9A. Current limiting occurs when the delta voltage across the sense resistor exceeds 45mV causing the current sense amplifier to pull down the combined CO and COMP pins. Pulling COMP low reduces the width of pulses to the high side driver, limiting the output current of the converter. After reaching the current limit, the voltage feedback causes the COMP pin to rise and turn on the high side driver until the inductor current again reaches the ~9A current limit threshold. (Figure 9).

The parallel resistance also serves to inject the inductor current into the LM5115 feedback loop. Injecting a signal proportional to the instantaneous inductor current into a voltage mode controller improves the control loop stability and bandwidth. Current injection, which is a form of average current mode control, eliminates the lead R-C network in the feedback path that is normally required with voltage mode control. This not only simplifies the compensation but also reduces sensitivity to output noise that could pass through the lead network to the error amplifier.

In cases where a noisy current sense is present, adding a low pass filter to the input of CS and VOUT can help restore a cleaner waveform (*Figure 18* , R16 and C10). Care must be taken not to have a large RC time constant to avoid instability.

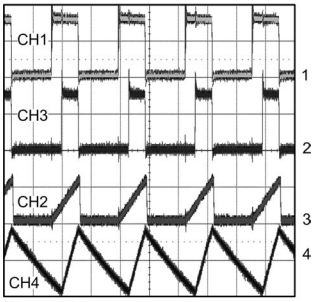
## Foldback Current Limit

Current limit foldback can be implemented with the following components: R17, R18, C10, D5, and R16 (see *Figure 18*). At nominal output voltage (VOUT > 3V) D5 is reversed biased and the current limit threshold is still ~45mV. At lower output voltage the resistor divider network along with the forward biased diode (D5) will increase the voltage across R16. In order to reach the 45mV current limit threshold, the voltage across the sense resistor (R7-R9) is reduced due to the increase in voltage across R16. Thus, the current limit is reduced providing current limit foldback. The resistor divider sets the voltage when current limit foldback kicks in and R16 sets the amount of current limit foldback.

A most common occurrence, that will prove unnerving, is when the current limit set on the source supply is insufficient for the load. The result is similar to having the high source impedance referred to earlier. The interaction of the source supply folding back and the UUT going into undervoltage shutdown will start an oscillation, or chatter, that may have highly undesirable consequences.

## Optional DC Buck

LM5115 can also be configured as a DC buck regulator. Information for the DC board can be found in LM5115 DC application note and LM5115 datasheet.




**$V_{IN}$ = 48V, Secondary output load = open**
CH1 = Main Phase Signal (5V/Div).
CH2 = RAMP (1V/Div).
CH3 = Secondary Switch Signal (5V/Div).
CH4 = Inductor Current Secondary (2A/Div).
Horizontal Resolution = 2 μs/Div.

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**FIGURE 4. Representative Waveform**

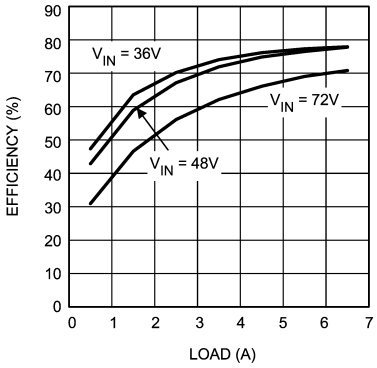


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**FIGURE 5. System Efficiency vs. Load Current and $V_{IN}$**

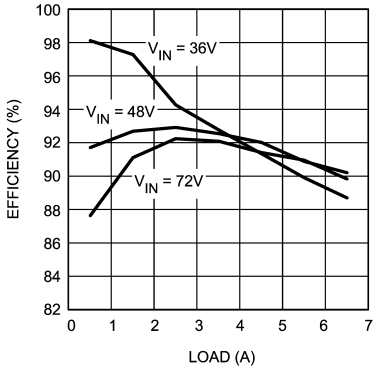


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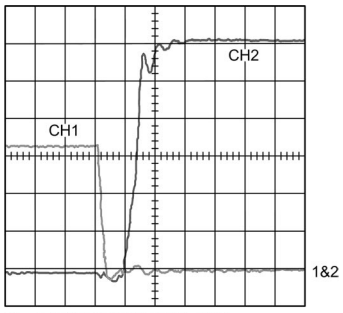
**FIGURE 6. Adjusted Efficiency on secondary side vs. Load Current and $V_{IN}$**




**$V_{IN}$ = 48V; LM5115 Load = 5.0A**
CH1 = Lo Side Sw Gate Drive, 2V/Div.
CH2 = Hi Side Sw Gate Drive, 2V/Div.
Horizontal Resolution = 100 ns/Div.

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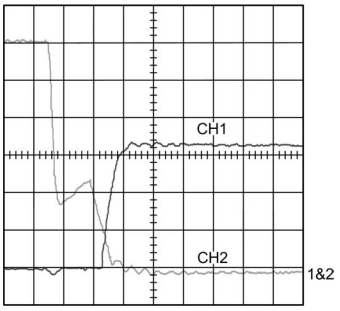
**FIGURE 7. Gate Turn-on Delay**




**$V_{IN}$ = 48V; LM5115 Load = 5.0A**
CH1 = Lo Side Sw Gate Drive, 2V/Div.
CH2 = Hi Side Sw Gate Drive, 2V/Div.
Horizontal Resolution = 100 ns/Div.

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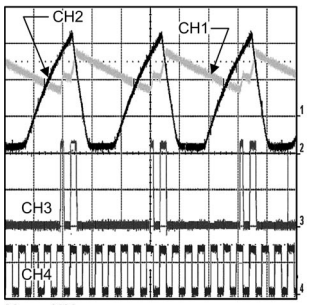
**FIGURE 8. Gate Turn-off Delay**




**$V_{IN}$ = 48V**
CH1 = Inductor Current, 5A/Div.
CH2 = COMP/CO, 1V/Div.
CH3 = High Side Switch Gate Drive, 5V/Div.
CH4 = Phase Signal, 5V/Div.
Horizontal Resolution = 10 μs/Div.

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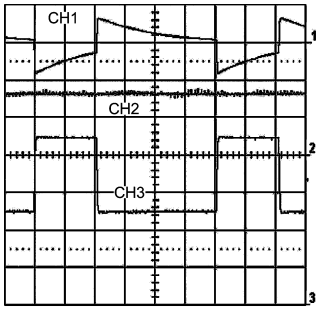
**FIGURE 9. Secondary Output Short Response**




**$V_{IN}$ = 48V**
CH1 = Secondary 2.0V Output, 100 mV/Div. (AC Mode).
CH2 = Main 3.3V Output, 2V/Div.
CH3 = Secondary Current Load (5A to 9A), 2A/Div.
Horizontal Resolution = 500 μs/Div.

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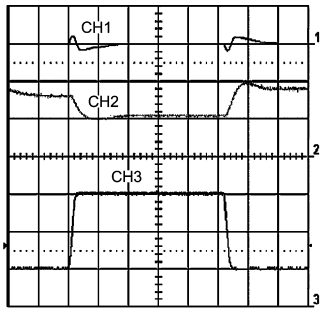
**FIGURE 10. Secondary Step Load Response**




**$V_{IN}$ = 48V**
CH1 = Secondary 2.0V Output, 100 mV/Div. AC.
CH2 = Main 3.3V Output, 2V/Div.
CH3 = Main Current Load (10A to 30A), 10A/Div.
Horizontal Resolution = 200 μs/Div.

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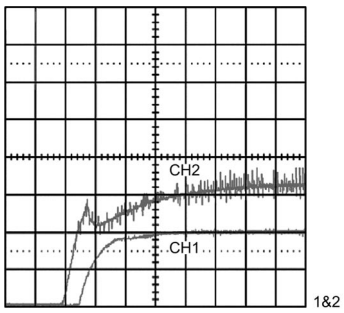
**FIGURE 11. Cross Regulation Step Load**




**$V_{IN}$ = 48V; LM5115 Load = 5.0A, LM5025 Load = Open**
CH1 = Secondary 2V Output, 1V/Div.
CH2 = Main 3.3V Output, 1V/Div.
Horizontal Resolution = 1 ms/Div.

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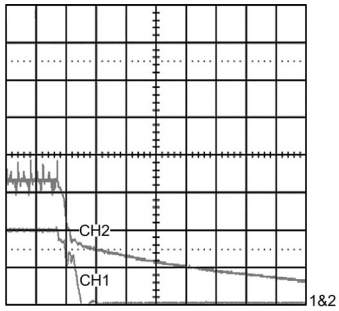
**FIGURE 12. Startup Response**




**$V_{IN}$ = 48V; LM5115 Load = 5.0A, LM5025 Load = Open**
CH1 = Secondary 2V Output, 1V/Div.
CH2 = Main 3.3V Output, 1V/Div.
Horizontal Resolution = 200 μs/Div.

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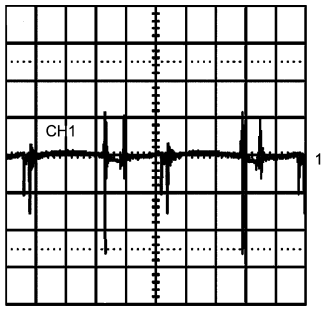
**FIGURE 13. Shutdown Response**




**$V_{IN}$ = 48V; LM5115 Load = 8.0A**
CH1 = Secondary 2V Output, 50 mV/Div. (AC Mode).
Horizontal Resolution = 1 μs/Div.

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**FIGURE 14. Secondary Ripple Voltage**

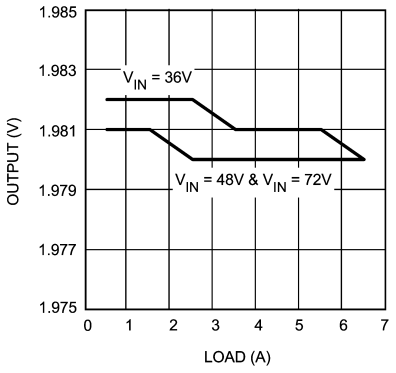


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**FIGURE 15. Output vs. Load Current & $V_{IN}$**

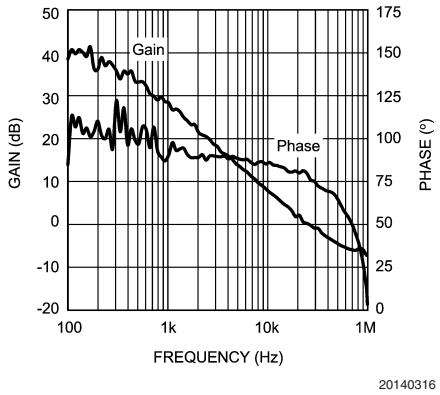



**FIGURE 16. Secondary Closed Loop Response**

# Application Circuit Schematic

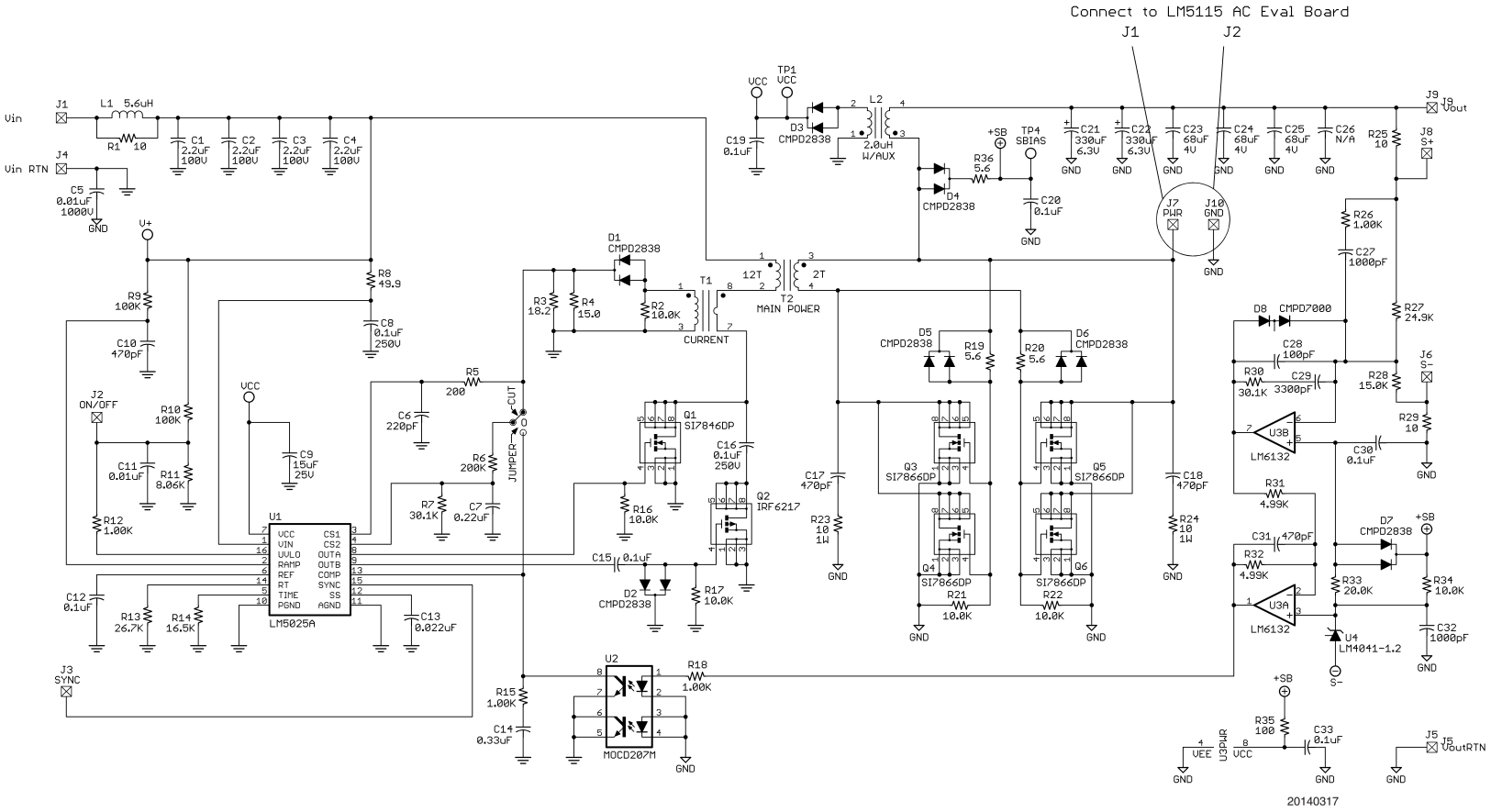
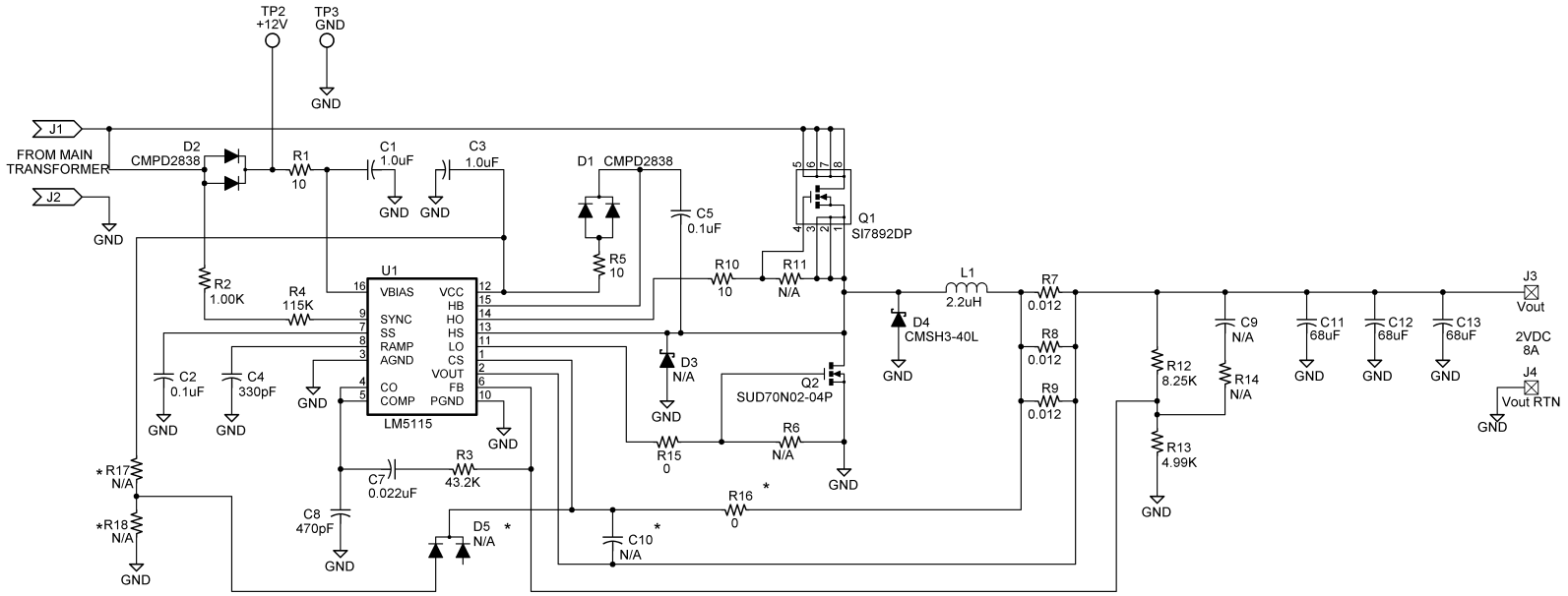



**FIGURE 17. LM5025A Eval Board**

## Application Circuit Schematic (Continued)




Note: * Components needed to implement fold-back current limit

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**FIGURE 18. LM5115 AC Eval Board Schematic**

## Bill of Materials

| ITEM | | PART NUMBER | DESCRIPTION | VALUE |
|---|---|---|---|---|
| C | 1 | C3216X7R1E105K | CAPACITOR, CER, TDK | 1.0 µF, 25V |
| C | 2 | C2012X7R1H104K | CAPACITOR, CER, TDK | 0.1 µF, 50V |
| C | 3 | C3216X7R1E105K | CAPACITOR, CER, TDK | 1.0 µF, 25V |
| C | 4 | C2012COG1H331K | CAPACITOR, CER, TDK | 330 pF, 50V |
| C | 5 | C2012X7R1H104K | CAPACITOR, CER, TDK | 0.1 µF, 50V |
| C | 6 | | | Not Used |
| C | 7 | C2012COG1H223K | CAPACITOR, CER, TDK | 0.022µF, 50V |
| C | 8 | C2012COG1H471K | CAPACITOR, CER, TDK | 470 pF, 50V |
| C | 9 | | | Not Used |
| C | 10 | | | Not Used |
| C | 11 | C4532X7SOG686M | CAPACITOR, CER, TDK | 68 µF, 4.0V |
| C | 12 | C4532X7SOG686M | CAPACITOR, CER, TDK | 68 µF, 4.0V |
| C | 13 | C4532X7SOG686M | CAPACITOR, CER, TDK | 68 µF, 4.0V |
| D | 1 | CMPD2838E-NSA | DIODE, SIGNAL, CENTRAL, SEMI | |
| D | 2 | CMPD2838E-NSA | DIODE, SIGNAL, CENTRAL, SEMI | |
| D | 3 | | | Not Used |
| D | 4 | CMSH3-40L-NSA | DIODE SHOTTKY, CENTRAL, SEMI | CMSH3-40L |
| D | 5 | | | Not Used |
| J | 1 | 2515-1-01-01-00-00-07-0 | SOLDER TERMINAL SLOTTED, MILL-MAX | |
| J | 2 | 2515-1-01-01-00-00-07-0 | SOLDER TERMINAL SLOTTED, MILL-MAX | |
| J | 3 | 5002 | TERMINAL, SMALL TEST POINT, KEYSTONE | |
| J | 4 | 5002 | TERMINAL, SMALL TEST POINT, KEYSTONE | |
| R | 1 | CRCW080510R0J | RESISTOR, VISHAY | 10 |
| R | 2 | CRCW08051001F | RESISTOR, VISHAY | 1.00 K |
| R | 3 | CRCW08054322F | RESISTOR, VISHAY | 43.2 K |
| R | 4 | CRCW08051153F | RESISTOR, VISHAY | 115 K |
| R | 5 | CRCW080510R0J | RESISTOR, VISHAY | 10 |
| R | 6 | | | Not Used |
| R | 7 | CRCW1206R012F | RESISTOR, VISHAY , Newark # 06HO462 | 0.012 |
| R | 8 | CRCW1206R012F | RESISTOR, VISHAY , Newark # 06HO462 | 0.012 |
| R | 9 | CRCW1206R012F | RESISTOR, VISHAY , Newark # 06HO462 | 0.012 |
| R | 10 | CRCW080510R0J | RESISTOR, VISHAY | 10 |
| R | 11 | | | Not Used |
| R | 12 | CRCW08058251F | RESISTOR, VISHAY | 8.25 K |
| R | 13 | CRCW08054991F | RESISTOR, VISHAY | 4.99K |
| R | 14 | | | Not Used |
| R | 15 | CRCW08050000Z | RESISTOR, VISHAY | 0 OHMS |
| R | 16 | CRCW08050000Z | RESISTOR, VISHAY | 0 OHMS |
| R | 17 | | | Not Used |
| R | 18 | | | Not Used |
| Q | 1 | SI7892DP | MOSFET, N-CH, POWER S0-8 PKG, VISHAY | SI7892DP |
| Q | 2 | SUD70N02 | MOSFET, N-CH, DPAK PKG, VISHAY | SUD70N02 |
| L | 1 | DR356-2-272 | INDUCTOR, COOPER, DR127-2R2 | 2.2 uH - 12A |
| U | 1 | LM5115 | CONTROLLER, SINGLE OUT, PWM, NATIONAL | LM 5115 |

## PCB Layout(s)

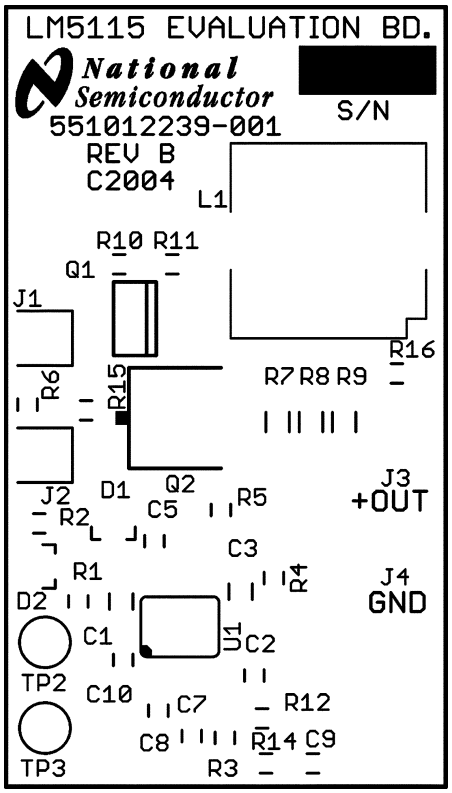


**FIGURE 19. Top Silk Screen LM5115**

## PCB Layout(s) (Continued)

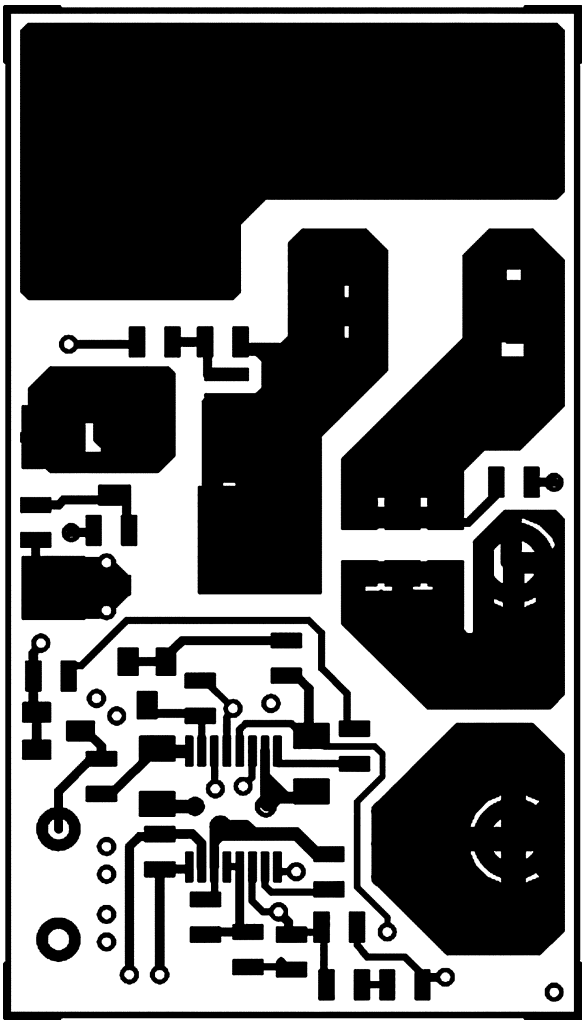

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**FIGURE 20. Top Layer LM5115**

## PCB Layout(s) (Continued)

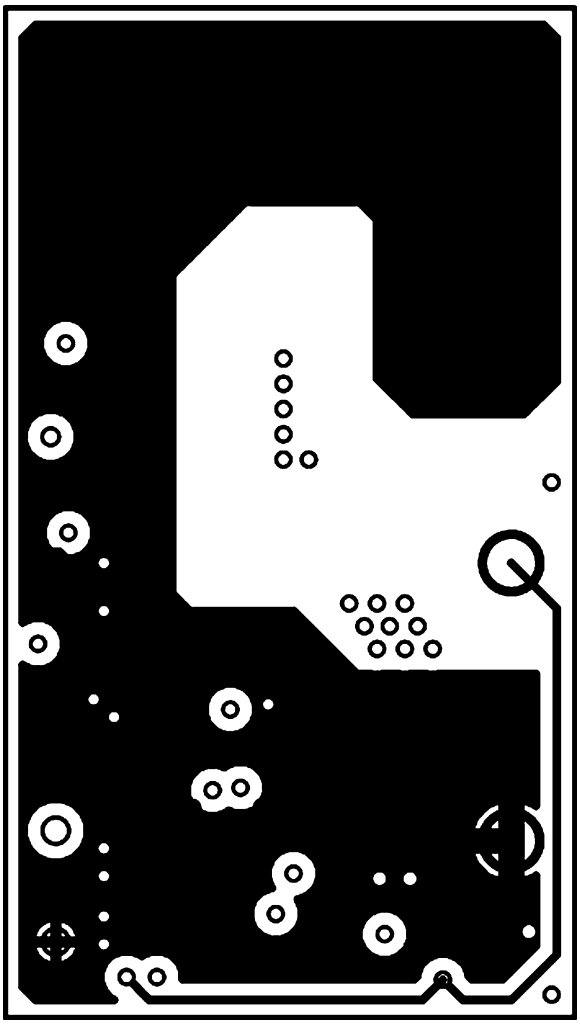

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**FIGURE 21. Layer 2 LM5115**

## PCB Layout(s) (Continued)

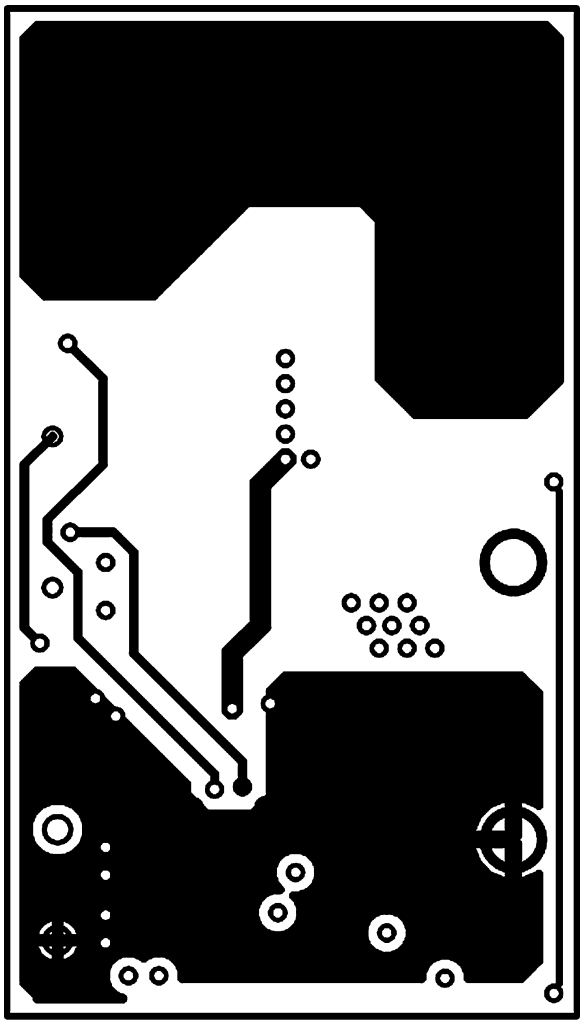

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**FIGURE 22. Layer 3 LM5115**

## PCB Layout(s) (Continued)

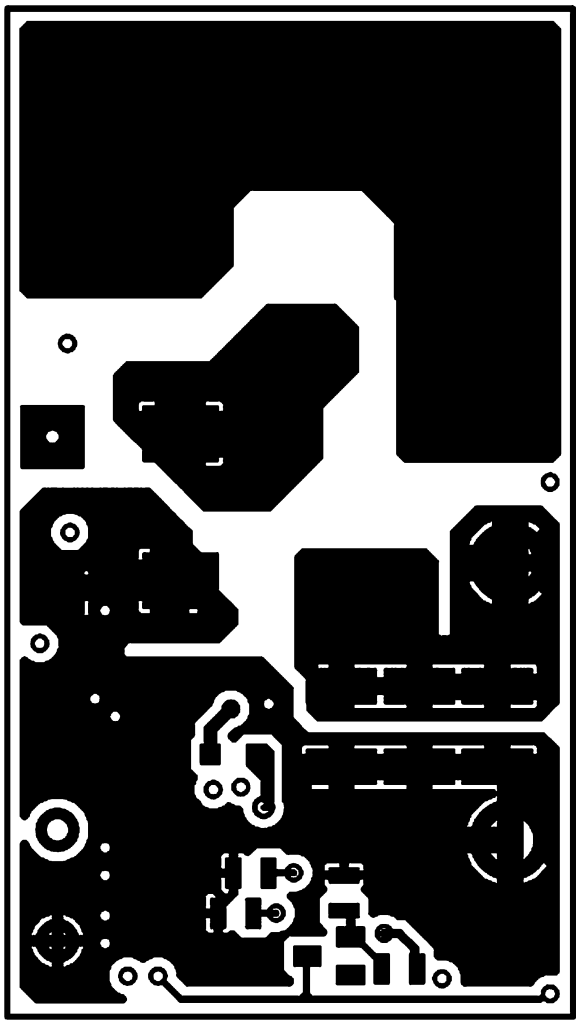

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**FIGURE 23. Bottom Layer LM5115, as Viewed from Top**

## PCB Layout(s) (Continued)

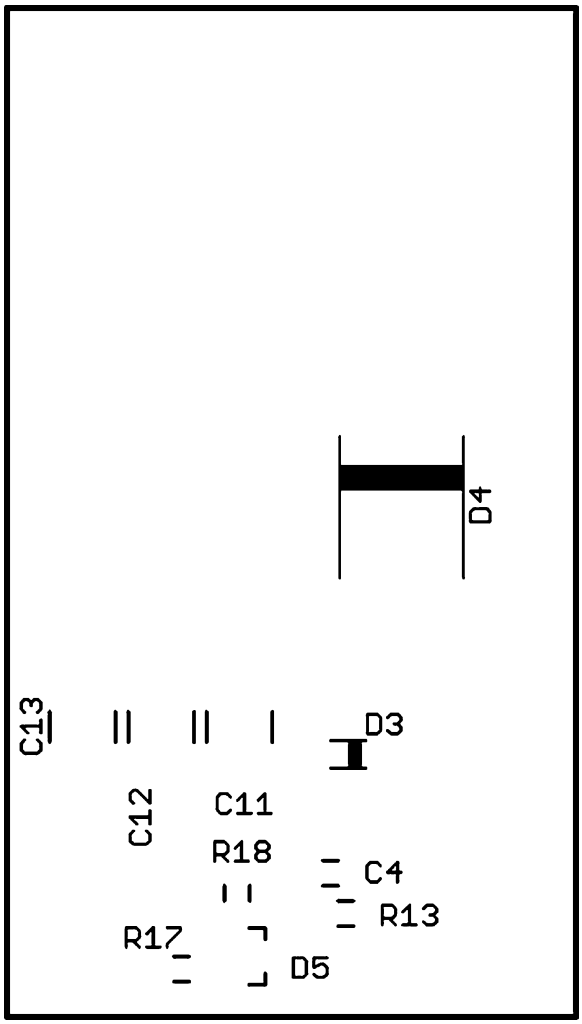


**FIGURE 24. Bottom Silk Screen LM5115**

## Notes



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