Comparison of COP8SAx7 to the Flash Based COP8TAx9 Family - Hardware and Software Considerations

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Bob Moeckel and Abdul Aleaf
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1.0 Introduction

The purpose of this Application Note is to provide a detailed comparison and feature analysis of the COP8SAx7 and COP8TAx9 families of devices. Where applicable, this report can be used to assist in converting applications developed for the COP8SAx7 device to operate on an equivalent COP8TAx9 device.

As suggested, the COP8TAx9 family offers additional useful and enhanced features when compared to the COP8SAx7 family. With the additional features, the COP8TAx9 family may appear much different, but this family is designed to maintain downward compatibility with the COP8SAx7 family as much as possible. The intent is to provide the COP8SAx7 user with an easy upgrade path to the COP8TAx9 devices with minimal firmware changes.

The COP8SAA7, COP8SAB7 and COP8SAC7 (COP8SAx7 family) devices are members of the COP8 Feature Family that contain EPROM, RAM, a 16-bit multi-function timer with two autorelaod/capture registers, eight interrupt sources supporting a vectored interrupt scheme, the enhanced MICROWIRE/PLUS serial interface and, in addition, these devices contain features such as Multi-Input Wakeup with up to 7 wakeup inputs, WATCHDOG/Clock Monitor, Idle timer supporting Idle mode, internal Power-On Reset, on-chip RC oscillator, 8 bytes of user storage space in EPROM, and on-chip EMI reduction circuitry. The devices are offered in 16-pin SO/DIP, 20-pin SO/DIP, 28-pin SO/DIP, 40-pin DIP, and 44-pin PLCC/PQFP. The operating voltage range is from 2.7V to 5.5V. See the datasheet for more details.

The COP8TAB9 and COP8TAC9 (COP8TAx9 family) devices encompass all the features of the COP8SAx7 family, but with Flash memory and some additions. One additonal interrupt source is provided which supports the ACCESS-.Bus serial interface which is compatible with I2C® and SMBus™ interfaces. Eight additional Multi-Input Wakeup inputs are provided for a total of 16 wakeup inputs, An improved on-chip RC oscillator with on-chip programmable clock divider is available for the user. The devices are offered in 20-pin SOIC, 28-pin SOIC and 44-pin LLP chip scale packages. The operating voltage is well suited to battery applications with a range of 2.25V to 2.75V. See the datasheet for more details.

The COP8TAB9 and COP8TAC9 are also supported by low cost ROM devices (COP8TAB5 and COP8TAC5) for large volume applications.

2.0 Highlights of COP8TAx9 Enhancements Over COP8SAx7

1. The operating voltage has been reduced for lower power dissipation, reduced emissions and better suitability for battery powered applications (2.25V to 2.75V).
2. The dynamic supply current is lower.
3. A programmable clock divider has been provide to dynamically reduce the frequency of operation. This allows the user to reduce power dissipation at times of low performance requirement while maintaining the capability to quickly increase performance when it is required.
4. The R/C oscillator option is expanded to include the choice of selecting on-chip R/C components.
5. Accuracy of the R/C oscillator is improved to ±20%.
6. COP8SAx7's Port D is replaced with a bi-directional Port J.
7. All inputs utilize Schmitt trigger circuitry for improved noise immunity.
8. The user selectable Power-On Reset feature is added, in addition to the ability to reset the device externally. The on-chip Power-On Reset eliminates the need for using external components associated with reset circuitry.
9. The unique power saving Multi-Input Wakeup feature is expanded to include Port C Pins.
10. The ACCESS.Bus serial interface has been added to provide greater flexibility in interfacing with host processors and peripherals. The ACCESS.Bus serial interface is compatible with the popular I2C and SMBus interfaces. The ACCESS.Bus interface can optionally be made compatible with busses operating at 1.8V logic levels.
11. The Option Register is expanded to select additional user selectable features such as WATCHDOG, on-chip R/C oscillator (with either fixed value on-chip or user supplied off-chip frequency control resistor), on-chip crystal oscillator biasing resistor, HALT mode and selection of 1.8V compatibility for ACCESS.Bus inputs.

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3.0 Summary of Differences Between COP8SAx7 and COP8TAx9

The following table provides a detailed summary of differences between the COP8SAx7 and COP8TAx9.

TABLE 1. Differences Between COP8SAx7 and COP8TAx9

FEATURES	COP8SAx7	COP8TAx9
Operating Voltage	2.7V to 5.5V	2.25V to 2.75V
Dynamic Supply Current CKI = 10 MHz	10 mA @ 5.0V	6 mA @ 2.5V
Typical HALT Current	< 4 µA	<2.5 µA
Maximum Clock Frequency	Crystal: 10 MHz, R/C 6MHz, External 10MHz	Crystal: 15 MHz, R/C 15 MHz, External 15 MHz
Port L0-L7	Port L has Schmitt Trigger inputs.	All inputs have Schmitt Triggers.
Port L0-L3 Min Sink Current	15 mA, Vol = 1.0V at V_{CC} = 4.5V	All outputs with 10mA sink capability. Vol = 0.4V at V_{CC} = 2.25V
R/C Oscillator	On-Chip R/C or On-Chip R/C with External Capacitor.	On-Chip R/C or On-Chip R/C with External Resistor.
R/C Oscillator Frequency Tolerance	R/C Oscillator tolerance is ±35%. Maximum R/C Oscillator Frequency is 6MHz.	On-chip R/C Oscillator tolerance is about ±20%. The addition of precision external frequency control resistor improves this tolerance to ±10%. The maximum R/C Oscillator Frequency (with external Resistor) is 15MHz.
Programmable Clock Divider	None. The internal clock is fixed to the CKI frequency.	A programmable clock divider has been provided which allows the user to dynamically divide the input clock by an integer value and thus control power and performance.
Output Only Port	Port D is output only.	Port D is replaced with an 8-bit I/O (Port J). Port J is Reset to output high state for software compatibility.
Pin G1		When WATCHDOG output is enabled on pin G1, a weak pullup is enabled which removes the requirement for external pullup resistor.
Pins G0-G3		New emulator interface which allows every device to be its own emulator.
RAM Map	Location DC (hex) is used to access the Port D output Register. This register is set to FF (hex) on RESET. Locations DD and DE (hex) are reserved.	Location DC (hex) is used to access the Port J output Register. Location DD (hex) is used to access the Port J Configuration Register. These registers are set to FF (hex) on RESET. Location DE (hex) is used to read current state of the Port J pins.
Reset/POR	External reset or on-chip, user selectable Power-On Reset. The external RC delay must be greater than 5x power supply rise time or 15 ms, whichever is greater.	Power-On Reset is always enabled, however external Reset is, internally, functionally ORed with Power-On Reset. External Reset can be used to extend the Power-On Reset or to reset the device during stable power.
ACCESS.Bus	None	The ACCESS.Bus synchronous serial interface has been added to provide greater flexibility in interfacing to peripherals and host processors. ACCESS.Bus is compatible with I2C and SMBus interfaces.

3.0 Summary of Differences Between COP8SAx7 and COP8TAx9 (Continued)

TABLE 1. Differences Between COP8SAx7 and COP8TAx9 (Continued)

ECON/Option Register	See the device datasheet for specifics of ECON bit assignment.	See the device datasheet for specifics of ECON bit assignment.
	1. The ECON Register is resident at the first memory address following the end of available program memory. For example, the ECON Register is situated at location 1000 (hex) on the 4k COP8SAC7 device.	1. The Option Register is resident at the last location of the available program memory. For example, the Option Registeris situated at location 0FFF (hex) on the 4k COP8TAC9 device.
	2. The least significant bit of the ECON Register is used for the HALT enable function on the COP8SAx7 devices. See the device datasheet for specifics of Option Register bit assignment.	2. The least significant bit of the Option Register is now used for the FLEX bit. This bit determines the source of instructions for execution on exit from RESET.
		3. The Power-On Reset selection has been eliminated, since the Power-On Reset is always enabled. This bit is used as a third bit for oscillator mode selection.
		4. The most significant bit of the Option Register provides the capability to interface the ACCESS.Bus with 1.8V logic levels.
Idle Timer/ Idle Mode	Contains an Idle Timer. Supports Idle Mode.	The Idle Timer interrupt is programmable to select a longer interval between Idle Timer interrupts or to provide a longer Idle interval.
Instruction Set	COP888 Feature family instruction set.	COP888 Feature family instruction set with additonal instructions to facilitate user written In-System Programming.
Packages	16-pin SO/DIP, 20-pin SO/DIP, 28-pin SO/DIP, 40-pin DIP, 44-pin PLCC	20-pin SOIC, 28-pin SOIC, 44-pin LLP
Reading Program Memory with Security Enabled	EPROM Reads FF (hex). If EPROM is secured, it can't be erased and rewritten. Security bit is protected from malicious erasure.	Flash Reads FF (hex) from external access, however Program Memory is not protected from access and updates from the firmware. This facilitates user written ISP updates.
Emulation	COP8-EM or DM replaces device in target board. Requires socket or adapter.	COP8-DMFlash interfaces via a 14 pin connector which can be placed on the target board right next to the device.
In-System Programmability	Not recommended	Provided via the MICROWIRE/PLUS serial interface and a special program or by the emulator. No high voltages required.
EMI	Contains EMI reduction circuitry.	Lower supply voltage and reduced supply current equate to reduced emissions.

4.0 Compatibility - Converting From COP8SAx7 to COP8TAx9

Using the differences outlined in *Table 1*, the following steps should be followed when converting from the COP8SAx7 to the COP8TAx9.

4.1 HARDWARE CONSIDERATIONS

4.1.1 PC Layout

In order to reduce the effect of digital noise within the device and within the system, the pinout of the device has been changed. The comparative pinouts for 20 and 28 pin SOIC devices are shown in *Figure 1* and *Figure 2*. A 44LLP (chip scale surface mount) package has been provided for users that require a greater number of I/O port pins.

4.0 Compatibility - Converting From COP8SAx7 to COP8TAx9 (Continued)

FIGURE 1. Comparative pinouts for 20 pin SOIC

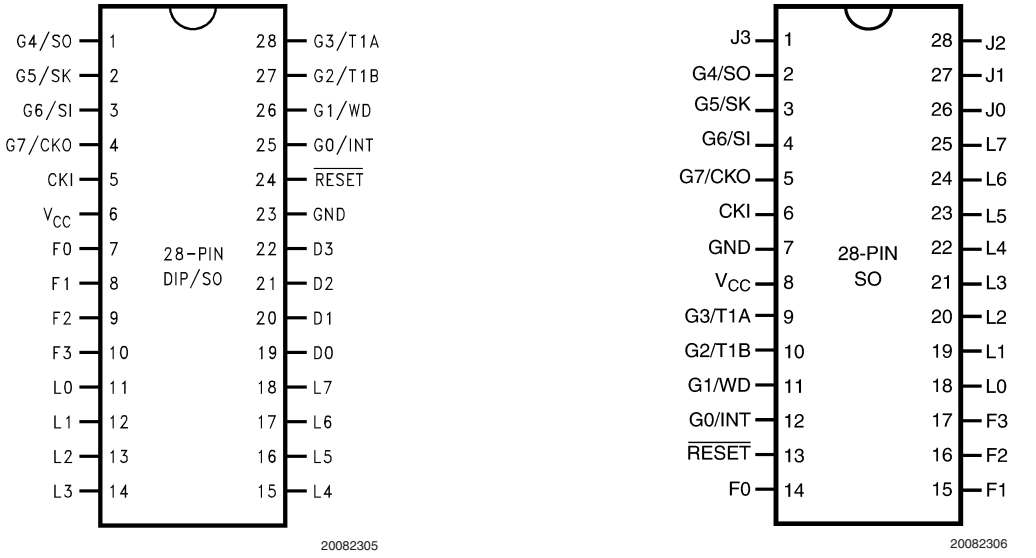

FIGURE 2. Comparative pinouts for 28 pin SOIC

4.1.2 ECON Register vs Option Byte

1. **R/C Oscillator**

   Bits 6 and 4 of the Option Register must be programmed with 0. This will select the R/C oscillator. External components are not needed unless a different operating frequency is required. For a different operating frequency, bit 3 of the Option Register must be set and an external resistor needs to be added from the CKI to the GND pin. This resistor defines a current which is used to control the internal frequency. See the datasheet for the appropriate resistor value. There are differences in R/C oscillator tolerances between the COP8SAx7 and COP8TAx9. For comparison, see the datasheets for these devices.

2. **Crystal Oscillator**

   Bits 6 and 4 of Option register must be programmed with 0 and 1 respectively. Bit 3 of the Option Register will then select the internal or external bias resistor depending on its state of 0 or 1, respectively.

3. **External Oscillator**

   Bit 6 of Option Register must be programmed with 1 to enable the external clock.

4. **Reset**

   Power-On Reset is always enabled. There is no setting for this in the Option Register.

5. **HALT Mode**

   Bit 1 of Option Register must be programmed with 1 to disable the HALT mode.

6. **WATCHDOG**

   Bit 2 of Option Register must be programmed with 1 to disable the WATCHDOG logic. This will allow the G1 pin to serve as a general purpose I/O.

4.0 Compatibility - Converting From COP8SAx7 to COP8TAx9

(Continued)

7. **RAM**

   RAM size does not vary by device. COP8TAB9 and COP8TAC9 have 128 bytes of RAM.

8. **Bit 7 of Option Register**

   When this bit is set, and the ACCESS.Bus is enabled, the input thresholds of pins L0 (SDA), L1 (SCL) and L2 are adjusted to be compatible with 1.8V logic.

9. **Bit 0 of Option Register**

   This bit (FLEX) determines the source of instructions for execution on exit from RESET. If this bit is set, instruction execution will start from location 0 of the Flash Memory. If this bit is cleared, instruction execution will start from location 0 of the resident 1k Boot ROM and will enter the MICROWIRE/PLUS ISP mode of operation.

10. **In-System Programmability**

    One of the most useful improvements of moving from EPROM to Flash is the addition of in-system programmability and reprogrammability. The COP8TAx9 devices provide the user with the capability to include this capability in production systems with little impact on the final application.

    In-system programming can be performed by two methods.:

    — The device contains a 1k byte Boot ROM which includes the firmware to communicate with a host via the MICROWIRE/PLUS serial interface and program the device. The Boot ROM code will be executed automatically if Bit 7 (FLEX) of the Option Register is cleared on exit from RESET. This is the case with all devices shipped from the factory.

    — The user program can provide the capability to update the flash memory using any chosen communication method. The code can link to subroutines in the Boot ROM which can Read and Write individual bytes and blocks of flash memory and also erase 512 byte pages or the entire flash memory. Note that if the entire flash memory is erased, the Boot ROM will initiate the MICROWIRE/PLUS ISP operation.

    The device can be forced into the MICROWIRE/PLUS ISP mode, regardless of the state of the Flex bit through simple techniques. Refer to the datasheet for more information.

11. **Emulation**

    Device emulation during development is considerably easier with flash based microcontrollers. The COP8TAx9 devices employ a technique which requires only the interruption of RESET and four port pins between the device and the system. In this way, development can be performed using the final production package in the final production board. The emulation connector can be replaced by simple jumpers for shipment to customers.

4.0 Compatibility - Converting From COP8SAx7 to COP8TAx9

(Continued)

4.2 SOFTWARE CONSIDERATIONS

1. **Port D/Port J Configuration**

   Since Port D is replaced by Port J on the COP8TAx9, Port J is configured as outputs in a High state upon reset. This means Port J data register (RAM location DC (hex)) and Port J configuration register (RAM location DD (hex)) both contain values of FF (hex) upon reset and user code may use Port J the same as Port D without software changes. In addition, Port J is read into RAM location DE (hex) and Port J may be used as a fully bidirectional port.

2. **Interrupt Handling**

   The COP8TAx9, adds one additional interrupt source from the ACCESS.Bus interface. In order to keep the COP8SAx7 interrupt handling code compatible with the COP8TAx9, the ACCESS.Bus interrupt source that is available on the COP8TAx9 must be disabled. The Enable bit associated with this additional interrupt source resides in the ACBCTL1 register (RAM location BB (hex)) and is cleared upon reset. Therefore, there is no code modification **required** as long as the user keeps the new additional source disabled.

   As with all unused interrupts, it is **recommended** that the user set up the interrupt handler to disable the ACCESS.Bus interrupt, should one occur. This can be accomplished by providing an interrupt subroutine that clears the pending bit and disables the ACCESS.Bus interrupt.

```
ACCESS:
 RBIT ENABLE,ACBCTL2      ;DISABLE
                          ; ACCESS.BUS MODULE
 RBIT INTEN,ACBCTL1       ;DISABLE ACCESS.BUS
                          ;INTERRUPT
 RETI                     ;RETURN FROM INTERRUPT
.= 01E0
 .ADDRW DEFVIS      ;NO INTERRUPT IS PENDING.
                    ;THIS IS A VALID CONDITION IF A
                    ;LEGAL INTERRUPT OCCURRED
                    ;DURING AN INSTRUCTION THAT
                    ;DISABLED IT
 .ADDRW LPINT       ;L/C PORT (MIWU) INTERRUPT
 .ADDRW RSVD        ;RESERVED INTERRUPT. THIS
                    ;SHOULDN'T HAPPEN
 .ADDRW RSVD        ;RESERVED INTERRUPT. THIS
                    ;SHOULDN'T HAPPEN
 .ADDRW RSVD        ;RESERVED INTERRUPT. THIS
                    ;SHOULDN'T HAPPEN
 .ADDRW RSVD        ;RESERVED INTERRUPT. THIS
                    ;SHOULDN'T HAPPEN
 .ADDRW RSVD        ;RESERVED INTERRUPT. THIS
                    ;SHOULDN'T HAPPEN
 .ADDRW RSVD        ;RESERVED INTERRUPT. THIS
                    ;SHOULDN'T HAPPEN
 .ADDRW ACCESS      ;ACCESS.BUS INTERRUPT
 .ADDRW UWIREINT    ;MICROWIRE+
                    ;INTERRUPT
 .ADDRW T1BINT      ;TIMER T1B INTERRUPT
 .ADDRW T1AINT      ;TIMER T1A/UNDERFLOW
                    ;INTERRUPT
 .ADDRW T0UND       ;T0 UNDERFLOW INTERRUPT
 .ADDRW EXTINT      ;EXTERNAL (G0) INTERRUPT
 .ADDRW NMINT       ;NMI INTERRUPT. NOT
                    ;IMPLEMENTED ON THIS CHIP
 .ADDRW TRAP        ;SOFTWARE TRAP
```

3. **Timer T0 (Idle Timer)**

   The enhanced capability of the COP8TAx9 Idle Timer allows the user to program the Idle Timer interrupt and Idle Mode wakeup interval. Available interval selections include 4096 (4k - reset default), 8192 (8k), 16384 (16k), 32768 (32k) or 65536 (64k) instruction cycles. See the COP8TAx9 datasheet for more information. If the user does not wish to change the Idle Timer interval, no program changes are necessary, however the user may wish to take advantage of the power reduction of a reduced number of wakeups in a given time period.

4. **Option Register location**

   The Option Register is resident at the last location of the available program memory. For example, the Option Register is situated at location 0FFF (hex) on the 4k COP8TAC9 device. This location becomes unavailable to the program and will always provide a 0 when accessed by the program memory for either data or instruction fetch. This will provide protection from accidentally executing this instruction by causing a Software Trap (INTR instruction).

4.3 ADDITIONAL FUNCTIONALITY

The COP8TAx9 devices provide additional functionality beyond that provided by the COP8SAx7. This additional functionality provides the user with the opportunity for applicaiton upgrades.

1. **ACCESS.Bus**

   The ACCESS.Bus synchronous serial communications protocol is compatible with the I2C and SMBus protocols. This allows the user greater flexibility in the choice of peripheral devices and communications channels.

   ACCESS.Bus is compatible with I2C and SMBus interfaces. This may eliminate the need for "bit banging" code which simulates these interfaces and may actually reduce the required code space. If the user chooses not to use this interface, no program changes are necessary.

4.0 Compatibility - Converting From COP8SAx7 to COP8TAx9

(Continued)

2. **Programmable Clock Divider**

   The device includes an on-chip clock divider which allows the user to reduce the effective operating frequency of the device by dividing the input clock frequency by an integer value.

   By reducing the effective clock frequency, power dissipation is reduced, although not as much as reducing the input frequency, however the user is still provided with a powerful tool which can tailor the power dissipation to the processing needs of the moment. Switching from faster clock to slower (or vice-versa) is quick, glitch free and requires only a write to a single register.

   If the user chooses not to take advantage of this feature, no changes need be made to the program.

3. **Multi-Input Wakeup**

   Both devices offer the power saving Multi-Input Wakeup feature, however the COP8TAx9 offers up to 8 additional Multi-Input Wakeup inputs. These additonal inputs are an alternate function of Port C. Still, there is no code change required because, during reset initialization, the Port C Wakeup Enable register (RAM address location 85 (hex)) is cleared, thus disabling the Port C Multi-Input Wakeup feature.

   Pin L0 has an alternate function of the ACCESS.Bus SDA line. This allows the user to select wakeup on ACCESS.Bus activity. The byte transfer, which accomplishes the wakeup of the device, will be lost, however this can be considered in system design.

4. **In-System Programming**

   One of the benefits of Flash memory over EPROM is that ease of programming and reprogramming, often in-system. COP8TAx devices provide a simple means for initial and update programming, via the MICROWIRE/Plus interface without removal from te system.

5. **Emulation**

   Non-Flash based COP8 devices require special emulation devices for use with In-System emulators for development. COP8TAx9 devices are designed such that, with the inclusion of a standard 14 pin header (0.1 in. X 0.1 in. spacing) on the application board, the emulation system can be connected to any production unit. This provides easy debugging of field returns and an additional means of programming.

6. **Virtual EEPROM**

   Field configurable applications often require non-volatile memory to maintain configuration options from one use to another. One or more pages (512 byte increments) of the COP8TAx9 device's flash memory can be reserved within the application for the storage of configuration information. By calling subroutines in the Boot ROM, the user can erase and reprogram pages of the flash memory under program control.

National Semiconductor
Americas Customer
Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560