# DP83848 - Single 10/100 Mb/s Ethernet Transceiver Initialization During Power Down Mode

National Semiconductor
Application Note 1402
Brad Kennedy
September 2005



## 1.0 Introduction

Certain systems or applications require the Ethernet network connection be held in a disconnected state or a Power Down mode until the rest of the system is powered up, initialized and ready to accept network traffic. This requirement is in addition to the ability to power down from a normal powered up operating mode.

National's DP83848 10/100 Mb/s single port Physical Layer device is designed with an option to support initialization during a Power Down mode at system power up. This option can be implemented using external logic, an external resistor, or a combination of logic and a resistor.

This application note details the procedure to put the device into Power Down mode during initialization, configure the registers of the device to the desired mode, and then exit Power Down.

## 2.0 Power Down Mode Functionality

During Power Down mode, the DP83848 core functions are disabled. This includes the line driver, the receiver and the MII/RMII interface. Management entities can still access the internal registers through the MDIO when the device is in this Power Down mode. Upon entering and exiting Power Down mode, the registers will preserve their configuration.

### 2.1 Note on Dual Function PWR_DOWN/INT Pin

The PWR DOWN/INT pin is a dual function pin. By default, the pin acts as an active low power down input. When configured via register access, the pin can alternately operate as an active low interrupt output. In this case, interrupts are asynchronously indicated by asserting the interrupt pin.

To configure interrupts, the user must set the INTEN bit (MICR bit 0) to configure the PWRDN_INTN pin as an active low interrupt pin. When interrupts are enabled, the PWRDN_INTN pin no longer acts as a power down input.

## 3.0 Power Down Configuration Sequence

The PWR_DOWN/INT pin (Pin 7) of the DP83848 is designed with an internal weak pull up. By default, this pin functions as a power down input.

During normal operation or upon initial power up, the DP83848 can be put in Power Down mode by asserting the PWR_DOWN/INT pin (Pin 7) low. This is equivalent to setting bit 11 (Power Down mode) in the Basic Mode Control Register, BMCR (0x00h). In this mode, the PHY is disabled, but still supports reads and writes to the registers.

Note that the status reflected in the BMCR power down bit is an OR function of the value written via MDIO access and the value asserted via the PWR_DOWN/INT pin. If the PWR_DOWN/INT pin is asserted low, attempts to clear the BMCR power down bit through MDIO accesses will be unsuccessful.

### 3.1 Initialization into Power Down Mode

The PWR_DOWN/INT pin can be asserted to a low state by one of two methods:

- Using an external pull-down resistor (See *Figure 1*).

or

- Directly driving the PWRDOWN/INT pin to a logic low level (See *Figure 2* or *Figure 3*).

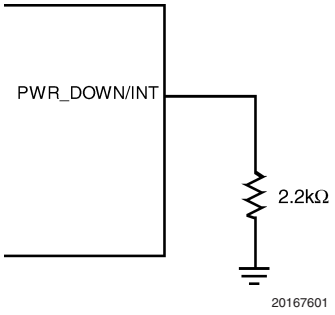


**FIGURE 1. Initialization Via Pull Down Resistor**

 

## 3.0 Power Down Configuration Sequence (Continued)

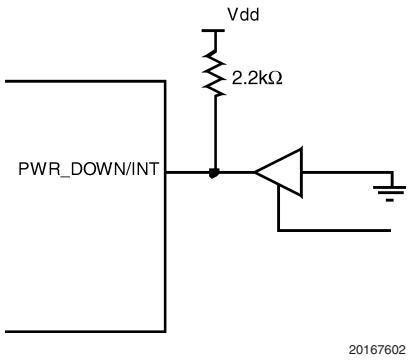


**FIGURE 2. Intitialization Via Tri-state Driver**

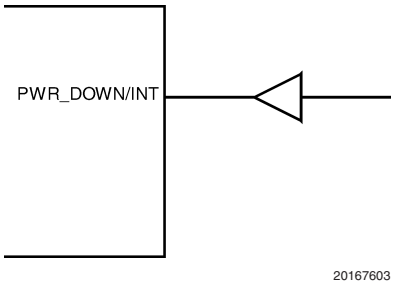


**FIGURE 3. Initialization Via Driver**

Note that using an external resistor (*Figure 1*) or using a logic driver (*Figure 3*) prevents the PWR_DOWN/INT pin from normal interrupt operation. When configured as an interrupt with one of these connections, the pin would be pulled down or driven low, effectively signalling an interrupt.

Using a tri-state driver and a pull up resistor (*Figure 2*), interrupt capability can be maintained. However, during the time that the device is held in a power down state via the tri-state driver, the system would have to ignore the interrupt signal from the device.

### 3.2 Configuration During Power Down Mode

In Power Down mode, the data path is disabled, i.e. no signals are driven onto the MII/RMII or the TPTD+/- and TPRD+/- pairs. The device registers can still be configured. Link speed, LED options and interrupt settings are all examples of register configurations.

The DP83848 retains the user selected configuration data upon powering up to a normal operating mode.

### 3.3 Exit from Power Down Mode

After the device is configured as desired, the device can be brought out of the Power Down mode into the normal operation in one of two ways:

- If Power Down Mode was established by asserting the PWR_DOWN/INT pin low via an external control signal, the signal can simply be driven high or tri-stated.

or

- If Power Down Mode was established using a pull-down resistor, normal operating mode is achieved via the dual functionality of the pin. In this case, the user must set the INT_OE bit in the MII Interrupt Control Register, MICR (0x11). This will enable the pin as an interrupt output, thus disabling the power down input and allowing the device to enter a normal operating mode. Note that the pin should not be utilized as a system interrupt in this case as the pull-down resistor would effectively signal a constant interrupt.

## 4.0 Summary

The DP83848 features an externally selectable option to enable Power Down mode. The device retains register configuration while transitioning between power down mode and normal operation mode.

For systems or applications that are power conscious, the DP83848 is a perfect fit. In addition to an architecture optimized for low power consumption, the DP83848 provides options for flexible device configuration with minimal system intervention overhead.

## Notes



**National Semiconductor**
**Americas Customer**
**Support Center**
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

**National Semiconductor**
**Europe Customer Support Center**
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

**National Semiconductor**
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Email: ap.support@nsc.com

**National Semiconductor**
**Japan Customer Support Center**
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560