## LM3409HV Evaluation Board

## Introduction

This evaluation board showcases the LM3409HV PFET controller for a buck current regulator. It is designed to drive 12 LEDs $\left(\mathrm{V}_{\mathrm{O}}=42 \mathrm{~V}\right)$ at a maximum average LED current ( $\mathrm{I}_{\mathrm{LED}}=$ $1.5 \mathrm{~A})$ from a $D C$ input voltage ( $\mathrm{V}_{\text {IN }}=48 \mathrm{~V}$ ). The switching frequency ( $\mathrm{f}_{\mathrm{Sw}}=400 \mathrm{kHz}$ ) is targeted for the nominal operating point, however $\mathrm{f}_{\mathrm{Sw}}$ varies across the entire operating range. The circuit can accept an input voltage of $6 \mathrm{~V}-75 \mathrm{~V}$. However, if the input voltage drops below the regulated LED string voltage, the converter goes into dropout and $\mathrm{V}_{\mathrm{O}}=\mathrm{V}_{\text {IN }}$ ideally.
The PCB is made using 4 layers of 2 oz . copper with FR4 dieletric. The evaluation board showcases all features of the LM3409HV including analog dimming using the IADJ pin and internal PWM dimming using the EN pin. High frequency external parallel FET shunt PWM dimming can also be evaluated. The board has a header ( J 1 ) with a removable jumper, which is used to select the PWM dimming method.
The evaluation board has a right angle connector (J2) which can mate with an external LED load board allowing for the LEDs to be mounted close to the driver. This reduces potential ringing when there is no output capacitor. Alternatively, the LED+ and LED- turrets can be used to connect the LED load.

This board can be easily modified to demonstrate other operating points as shown in the Alternate Designs section. The LM3409/09HV datasheet Design Procedure can be used to design for any set of specifications.

National Semiconductor
Application Note 1953
James Patterson
November 20, 2009

EFFICIENCY WITH 12 SERIES LEDS AT 1.5A


Since the board contains a buck regulator designed for 48 V input, the efficiency is very high at input voltages near or less than 48 V . The switching frequency increases as input voltage increases, yielding lower efficiency at higher input voltages. Note that increasing the off-time resistor (R6) will increase the efficiency at high input voltage.

## Schematic



## Pin Descriptions

| Pin(s) | Name | Description | Application Information |
| :---: | :---: | :---: | :---: |
| 1 | UVLO | Input under-voltage lockout | Connect to a resistor divider from $\mathrm{V}_{\text {IN }}$ and GND. Turn-on threshold is 1.24 V and hysteresis for turn-off is provided by a $22 \mu \mathrm{~A}$ current source. |
| 2 | IADJ | Analog LED current adjust | Apply a voltage between 0-1.24V, connect a resistor to GND, or leave open to set the current sense threshold voltage. |
| 3 | EN | Logic level enable / PWM dimming | Apply a voltage $>1.74 \mathrm{~V}$ to enable device, a PWM signal to dim, or a voltage $<0.5 \mathrm{~V}$ for low power shutdown. |
| 4 | COFF | Off-time programming | Connect resistor to $\mathrm{V}_{\mathrm{O}}$, and capacitor to GND to set the off-time. |
| 5 | GND | Ground | Connect to the system ground. |
| 6 | PGATE | Gate drive | Connect to the gate of the external PFET. |
| 7 | CSN | Negative current sense | Connect to the negative side of the sense resistor. |
| 8 | CSP | Positive current sense | Connect to the positive side of the sense resistor ( $\mathrm{V}_{\text {IN }}$ ). |
| 9 | VCC | $\mathrm{V}_{\mathrm{IN}}$ - referenced linear regulator output | Connect at least a $1 \mu \mathrm{~F}$ ceramic capacitor to $\mathrm{V}_{\mathbb{I}}$. The regulator provides power for the PFET drive. |
| 10 | VIN | Input voltage | Connect to the input voltage. |
| DAP | DAP | Thermal pad on bottom of IC | Connect to pin 5 (GND). Place 4-6 vias from DAP to bottom GND plane. |

## Bill of Materials

| Qty | Part ID | Part Value | Manufacturer | Part Number |
| :---: | :---: | :---: | :---: | :---: |
| 1 | U1 | Buck controller | NSC | LM3409HVMY |
| 2 | C1, C2 | 2.2 $\mu \mathrm{F}$ X7R 10\% 100V | MURATA | GRM43ER72A225KA01L |
| 1 | C3 | $0.1 \mu \mathrm{~F}$ X7R 10\% 100V | MURATA | GRM188R72A104KA35D |
| 1 | C4 | 1.0رF X7R 10\% 16V | TDK | C1608X7R1C105K |
| 1 | C5 | 0.1瑗 X7R 10\% 50V | MURATA | GRM319R71H104KA01D |
| 1 | C6 | 0.1瑗 X7R 10\% 50V | MURATA | GCM188R71H104KA57D |
| 1 | C7 | 470pF X7R 10\% 50V | TDK | C1608X7R1H471K |
| 3 | C8, D2, R11 | No Load |  |  |
| 1 | C9 | 2200pF X7R 10\% 50V | MURATA | GRM188R71H222KA01D |
| 1 | Q1 | PMOS 100V 3.8A | ZETEX | ZXMP10A18KTC |
| 1 | Q2 | CMOS 30V 2A | FAIRCHILD | FDC6333C |
| 1 | Q3 | NMOS 100V 7.5A | FAIRCHILD | FDS3672 |
| 1 | D1 | Schottky 100V 3A | VISHAY | SS3H10-E3/57T |
| 1 | L1 | $33 \mu \mathrm{H} 20 \% 3.2 \mathrm{~A}$ | TDK | SLF12575T-330M3R2 |
| 2 | R1, R2 | $1 \Omega 1 \%$ | VISHAY | CRCW06031R00FNEA |
| 1 | R3 | 10k $\Omega$ 1\% | VISHAY | CRCW060310K0FKEA |
| 1 | R4 | 100 $1 \%$ | VISHAY | CRCW0603100RFKEA |
| 1 | R5 | $0 \Omega 1 \%$ | VISHAY | CRCW06030000Z0EA |
| 1 | R6 | $16.5 \mathrm{k} \Omega 1 \%$ | VISHAY | CRCW060316K5FKEA |
| 1 | R7 | 6.98k 1 \% | VISHAY | CRCW06036K98FKEA |
| 1 | R8 | 49.9k 1 \% | VISHAY | CRCW060349K9FKEA |
| 1 | R9 | 0.15S 1\% 1W | VISHAY | WSL2512R1500FEA |
| 1 | R10 | 1k $1 \%$ | VISHAY | CRCW06031K00FKEA |
| 1 | J1 | 3 pin header | MOLEX | 22-28-4033 |
| 1 | J2 | 2x7 pin RA shrouded | SAMTEC | TSSH-107-01-S-D-RA |
| 2 | VIN, GND | banana jack | KEYSTONE | 575-8 |
| 7 | EN, Vadj, +5V, GND2, PWM2, LED+, LED- | turret | KEYSTONE | 1502-2 |

## PCB Layout

The 2 inner planes are GND and $\mathrm{V}_{1 \mathrm{~N}}$.


Top Layer
30093540


Bottom Layer

## Design Procedure

## SPECIFICATIONS

$\mathrm{V}_{\text {IN }}=48 \mathrm{~V} ; \mathrm{V}_{\text {IN-MAX }}=75 \mathrm{~V}$
$\mathrm{V}_{\mathrm{O}}=42 \mathrm{~V}$
$\mathrm{f}_{\mathrm{Sw}}=400 \mathrm{kHz}$
$\mathrm{I}_{\mathrm{LED}}=1.5 \mathrm{~A}$
$\Delta \mathrm{i}_{\text {LED-PP }}=\Delta \mathrm{i}_{\text {L-PP }}=300 \mathrm{~mA}$
$\Delta v_{\text {IN-PP }}=1.44 \mathrm{~V}$
$V_{\text {TURN }-\mathrm{ON}}=10 \mathrm{~V} ; \mathrm{V}_{\text {HYS }}=1.1 \mathrm{~V}$
$\eta=0.97$

1. NOMINAL SWITCHING FREQUENCY

Assume C7 $=470 \mathrm{pF}$ and $\eta=0.97$. Solve for R6:

$$
\begin{aligned}
& R 6=\frac{-\left(1-\frac{V_{O}}{\eta \times V_{\mathrm{IN}}}\right)}{(\mathrm{C} 7+20 \mathrm{pF}) \times f_{\mathrm{SW}} \times \ln \left(1-\frac{1.24 \mathrm{~V}}{V_{\mathrm{O}}}\right)} \\
& R 6=\frac{-\left(1-\frac{42 \mathrm{~V}}{0.97 \times 48 \mathrm{~V}}\right)}{490 \mathrm{pF} \times 400 \mathrm{kHz} \times \ln \left(1-\frac{1.24 \mathrm{~V}}{42 \mathrm{~V}}\right)}=16.7 \mathrm{k} \Omega
\end{aligned}
$$

The closest $1 \%$ tolerance resistor is $16.5 \mathrm{k} \Omega$ therefore the actual $\mathrm{t}_{\text {OFF }}$ and target $\mathrm{f}_{\text {Sw }}$ are:

$$
\begin{aligned}
& t_{\text {OFF }}=-(C 7+20 \mathrm{pF}) \times R 6 \times \ln \left(1-\frac{1.24 \mathrm{~V}}{\mathrm{~V}_{\mathrm{O}}}\right) \\
& \mathrm{t}_{\mathrm{OFF}}=-490 \mathrm{pF} \times 16.5 \mathrm{k} \Omega \times \ln \left(1-\frac{1.24 \mathrm{~V}}{42 \mathrm{~V}}\right)=242 \mathrm{~ns} \\
& \mathrm{f}_{\mathrm{SW}}=\frac{1-\left(\frac{\mathrm{V}_{\mathrm{O}}}{\eta \times \mathrm{V}_{\mathrm{N}}}\right)}{\mathrm{t}_{\mathrm{OFF}}}=\frac{1-\left(\frac{42 \mathrm{~V}}{0.97 \times 48 \mathrm{~V}}\right)}{242 \mathrm{~ns}}=404 \mathrm{kHz}
\end{aligned}
$$

The chosen components from step 1 are:

$$
\begin{aligned}
\mathrm{C} 7 & =470 \mathrm{pF} \\
\mathrm{R} 6 & =16.5 \mathrm{k} \Omega
\end{aligned}
$$

2. INDUCTOR RIPPLE CURRENT

Solve for L1:

$$
\mathrm{L} 1=\frac{\mathrm{V}_{\mathrm{O}} \times \mathrm{t}_{\mathrm{OFF}}}{\Delta \mathrm{i}_{\mathrm{L}-\mathrm{PP}}}=\frac{42 \mathrm{~V} \times 242 \mathrm{~ns}}{300 \mathrm{~mA}}=33.9 \mu \mathrm{H}
$$

The closest standard inductor value is $33 \mu \mathrm{H}$ therefore the actual $\Delta \mathrm{i}_{\mathrm{L}-\mathrm{Pp}}$ is:

$$
\Delta \mathrm{i}_{\mathrm{L}-\mathrm{PP}}=\frac{\mathrm{V}_{\mathrm{O}} \times \mathrm{t}_{\mathrm{OFF}}}{\mathrm{~L} 1}=\frac{42 \mathrm{~V} \times 242 \mathrm{~ns}}{33 \mu \mathrm{H}}=308 \mathrm{~mA}
$$

The chosen component from step 2 is:

$$
\mathrm{L} 1=33 \mu \mathrm{H}
$$

## 3. AVERAGE LED CURRENT

Determine $\mathrm{I}_{\mathrm{L}-\mathrm{MAX}}$ :

$$
\mathrm{I}_{\mathrm{L}-\mathrm{MAX}}=\mathrm{I}_{\mathrm{LED}}+\frac{\Delta \mathrm{i}_{\mathrm{L}-\mathrm{PP}}}{2}=1.5 \mathrm{~A}+\frac{308 \mathrm{~mA}}{2}=1.65 \mathrm{~A}
$$

Assume $\mathrm{V}_{\mathrm{ADJ}}=1.24 \mathrm{~V}$ and solve for R 9 :

$$
\mathrm{R} 9=\frac{\mathrm{V}_{\mathrm{ADJ}}}{5 \times \mathrm{I}_{\mathrm{L}-\mathrm{MAX}}}=\frac{1.24 \mathrm{~V}}{5 \times 1.65 \mathrm{~A}}=0.15 \Omega
$$

The closest $1 \%$ tolerance resistor is $0.15 \Omega$ therefore the $I_{\text {LED }}$ is:

$$
\begin{aligned}
& I_{\text {LED }}=\frac{V_{A D J}}{5 \times R 9}-\frac{\Delta i_{L-P P}}{2} \\
& I_{\text {LED }}=\frac{1.24 V}{5 \times 0.15 \Omega}-\frac{308 \mathrm{~mA}}{2}=1.5 \mathrm{~A}
\end{aligned}
$$

The chosen component from step 3 is:

$$
\mathrm{R} 9=0.15 \Omega
$$

## 4. OUTPUT CAPACITANCE

No output capacitance is necessary.

## 5. INPUT CAPACITANCE

Determine $\mathrm{t}_{\mathrm{ON}}$ :

$$
\mathrm{t}_{\mathrm{ON}}=\frac{1}{\mathrm{f}_{\mathrm{SW}}}-\mathrm{t}_{\text {OFF }}=\frac{1}{404 \mathrm{kHz}}-242 \mathrm{~ns}=2.23 \mu \mathrm{~s}
$$

Solve for $\mathrm{C}_{\text {IN-MIN }}$ :

$$
\mathrm{C}_{\mathrm{IN}-\mathrm{MIN}}=\frac{\mathrm{I}_{\mathrm{LED}} \times \mathrm{t}_{\mathrm{ON}}}{\Delta \mathrm{v}_{\mathrm{IN}-\mathrm{PP}}}=\frac{1.5 \mathrm{~A} \times 2.23 \mu \mathrm{~s}}{1.44 \mathrm{~V}}=2.32 \mu \mathrm{~F}
$$

Choose $\mathrm{C}_{\mathrm{IN}}$ :

$$
\mathrm{C}_{\mathrm{IN}}=\mathrm{C}_{\text {IN-MIN }} \times 1.75=4.07 \mu \mathrm{~F}
$$

Determine $\mathrm{I}_{\mathrm{IN}_{\mathrm{RMS}}}$ :
$I_{\text {IN-RMS }}=I_{\text {LED }} \times f_{\text {SW }} \times \sqrt{t_{\text {ON }} \times t_{\text {OFF }}}$
$\mathrm{I}_{\mathrm{N} \text {-RMS }}=1.5 \mathrm{~A} \times 404 \mathrm{kHz} \times \sqrt{2.32 \mu \mathrm{~s} \times 242 \mathrm{~ns}}=446 \mathrm{~mA}$
The chosen components from step 5 are:

$$
\begin{aligned}
& \mathrm{C} 1=\mathrm{C} 2=2.2 \mu \mathrm{~F} \\
& \mathrm{C} 3=0.1 \mu \mathrm{~F}
\end{aligned}
$$

## 6. P-CHANNEL MOSFET

Determine minimum Q1 voltage rating and current rating:

$$
\begin{gathered}
V_{T-M A X}=V_{I N-M A X}=75 \mathrm{~V} \\
I_{T}=D \times I_{\text {LED }}=\frac{V_{O} \times I_{\text {LED }}}{V_{I N} \times \eta}=\frac{42 \mathrm{~V} \times 1.5 \mathrm{~A}}{48 \mathrm{~V} \times 0.97}=1.35 \mathrm{~A}
\end{gathered}
$$

A 100V 3.8A PFET is chosen with $R_{D S-O N}=190 \mathrm{~m} \Omega$ and $Q_{g}=$ 20nC. Determine $\mathrm{I}_{\mathrm{T}-\mathrm{RMS}}$ and $\mathrm{P}_{\mathrm{T}}$ :

$$
\begin{aligned}
& I_{T-R M S}=I_{\text {LED }} \times \sqrt{D x\left(1+\frac{1}{12} \times\left(\frac{\Delta i_{\mathrm{L}-\mathrm{PP}}}{I_{\mathrm{LED}}}\right)^{2}\right)} \\
& I_{\mathrm{T}-R M S}=1.5 \mathrm{~A} \times \sqrt{\frac{42 \mathrm{~V}}{48 \mathrm{~V} \times 0.97} \times\left(1+\frac{1}{12} \times\left(\frac{308 \mathrm{~mA}}{1.5 \mathrm{~A}}\right)^{2}\right)} \\
& I_{\mathrm{T}-\text { RMS }}=1.43 \mathrm{~A}
\end{aligned}
$$

$$
P_{T}=I_{T-R M S}{ }^{2} \times R_{D S O N}=1.43 A^{2} \times 190 \mathrm{~m} \Omega=387 \mathrm{~mW}
$$

The chosen component from step 6 is:

$$
\mathrm{Q} 1 \rightarrow 3.8 \mathrm{~A}, 100 \mathrm{~V}, \mathrm{DPAK}
$$

## 7. RE-CIRCULATING DIODE

Determine minimum D1 voltage rating and current rating:

$$
\begin{gathered}
V_{D-M A X}=V_{I N-M A X}=75 \mathrm{~V} \\
I_{D}=(1-D) \times I_{\text {LED }}=\left(1-\frac{V_{O}}{V_{I N} \times \eta}\right) \times I_{\text {LED }} \\
I_{D}=\left(1-\frac{42 \mathrm{~V}}{48 \mathrm{~V} \times 0.97}\right) \times 1.5 \mathrm{~A}=147 \mathrm{~mA}
\end{gathered}
$$

A 100 V 3 A diode is chosen with $\mathrm{V}_{\mathrm{D}}=750 \mathrm{mV}$. Determine $\mathrm{P}_{\mathrm{D}}$ :

$$
P_{D}=I_{D} \times V_{D}=147 \mathrm{~mA} \times 750 \mathrm{mV}=110 \mathrm{~mW}
$$

The chosen component from step 7 is:

$$
\text { D1 } \rightarrow 3 \mathrm{~A}, 100 \mathrm{~V}, \mathrm{SMC}
$$

## 8. INPUT UNDER-VOLTAGE LOCKOUT (UVLO)

Solve for R8:

$$
\mathrm{R} 8=\frac{\mathrm{V}_{\mathrm{HYS}}}{22 \mu \mathrm{~A}}=\frac{1.1 \mathrm{~V}}{22 \mu \mathrm{~A}}=50 \mathrm{k} \Omega
$$

The closest $1 \%$ tolerance resistor is $49.9 \mathrm{k} \Omega$ so $\mathrm{V}_{\mathrm{HYS}}$ is:

$$
V_{H Y S}=R 8 \times 22 \mu \mathrm{~A}=49.9 \mathrm{k} \Omega \times 22 \mu \mathrm{~A}=1.1 \mathrm{~V}
$$

Solve for R7:

$$
\mathrm{R} 7=\frac{1.24 \mathrm{~V} \times R 8}{\mathrm{~V}_{\text {TURN }-\mathrm{ON}}-1.24 \mathrm{~V}}=\frac{1.24 \mathrm{~V} \times 49.9 \mathrm{k} \Omega}{10 \mathrm{~V}-1.24 \mathrm{~V}}=7.06 \mathrm{k} \Omega
$$

The closest $1 \%$ tolerance resistor is $6.98 \mathrm{k} \Omega$ so $\mathrm{V}_{\text {TURN-ON }}$ is:

$$
\begin{aligned}
& V_{\text {TURN }-O N}=\frac{1.24 \mathrm{~V} \times(\mathrm{R} 7+\mathrm{R} 8)}{\mathrm{R} 7} \\
& V_{\text {TURN }-O N}=\frac{1.24 \mathrm{~V} \times(6.98 \mathrm{k} \Omega+49.9 \mathrm{k} \Omega)}{6.98 \mathrm{k} \Omega}=10.1 \mathrm{~V}
\end{aligned}
$$

The chosen components from step 8 are:

$$
\begin{aligned}
& \mathrm{R} 7=6.98 \mathrm{k} \Omega \\
& \mathrm{R} 8=49.9 \mathrm{k} \Omega
\end{aligned}
$$

## 9. IADJ CONNECTION METHOD

The IADJ pin controls the high-side current sense threshold in three ways outlined in the datasheet. The LM3409HV evaluation board allows for all three methods to be evaluated using C6, R10, and the VADJ terminal.
Method \#1: If the VADJ terminal is not connected to the power supply, then the internal Zener diode biases the pin to 1.24 V and the current sense threshold is nominally 248 mV .

Method \#2: Applying an external voltage to the VADJ terminal between 0 and 1.24 V linearly scales the current sense threshold between 0 and 248 mV nominally. It can be necessary to have an RC filter when using an external power supply in order to remove any high frequency noise or oscillations created by the power supply and the connecting cables. The filter is chosen by assuming a standard value of $\mathrm{C} 6=0.1 \mu \mathrm{~F}$ and solving for a cut-off frequency $\mathrm{f}_{\mathrm{C}}<2 \mathrm{kHz}$ :

$$
\mathrm{R} 10>\frac{1}{2 \pi \times \mathrm{f}_{\mathrm{C}} \times \mathrm{C} 6}=\frac{1}{2 \pi \times 2 \mathrm{kHz} \times 0.1 \mu \mathrm{~F}}=796 \Omega
$$

Since an exact $f_{C}$ is not critical, a standard value of $1 \mathrm{k} \Omega$ is used. The Typical Waveforms section shows a typical LED current waveform when analog dimming using an external voltage source.
Method \#3: (This method requires modification of the received evaluation board). The internal $5 \mu \mathrm{~A}$ current source can be used to bias the voltage across an external resistor to ground ( $\mathrm{R}_{\mathrm{EXT}}$ ) across C 6 on the evaluation board. The resistor is sized knowing the desired average LED current I LED (must be $<1.5 \mathrm{~A}$ which is default using method \#1):


The chosen components from step 9 are:

$$
\begin{aligned}
& \mathrm{C} 6=0.1 \mu \mathrm{~F} \\
& \mathrm{R} 10=1 \mathrm{k} \Omega
\end{aligned}
$$

## 10. PWM DIMMING METHOD

The LM3409HV evaluation board allows for PWM dimming to be evaluated as follows:

$$
\begin{aligned}
& \text { 1: No } \mathrm{PWM}, \mathrm{EN}=\mathrm{V}_{\mathrm{IN}} \\
& \text { 2: External } \mathrm{PWM}, \mathrm{EN} \text { coupled } \\
& \text { 3: Internal } \mathrm{PWM} \text {, using EN }
\end{aligned}
$$



30093502
Method \#1: If no PWM dimming is desired, a jumper should be placed in position 1 (shorts pins 1 and 2) on header J1. This shorts VIN and EN which ensures the controller is always enabled if an input voltage greater than 1.74 V is applied.
Method \#2: External parallel FET shunt dimming can be evaluated by placing the jumper in position 2 (shorts pins 2 and 3 ) on header J1. This connects the capacitive coupling circuit to the EN pin as suggested in the datasheet. The resistor (R4) can be solved for assuming a standard capacitor value C9 = 2.2 nF and a desired time constant ( $\mathrm{t}_{\mathrm{C}}=220 \mathrm{~ns}<\mathrm{t}_{\text {OFF }}$ ) as follows:

$$
\mathrm{R} 4=\frac{\mathrm{t}_{\mathrm{C}}}{\mathrm{C} 9}=\frac{220 \mathrm{~ns}}{2.2 \mathrm{nF}}=100 \Omega
$$

The external shunt FET dimming circuit shown below is designed using an N -channel MosFET (Q3), a CMOS FET (Q2), two gate current limiting resistors (R1 and R2), a pull-up resistor (R3), and a bypass capacitor (C5). With an external 5V power supply attached to the 5 V terminal and an external PWM signal attached to the PWM2 terminal, the shunt dimming circuit is complete. Q3 is the shunt dimFET which conducts the LED current when turned on and blocks the LED voltage when turned off. Q3 needs to be fast and rated for $\mathrm{V}_{\mathrm{O}}$ and $\mathrm{I}_{\text {LED }}$. For design flexibility, a fast $100 \mathrm{~V}, 7.5 \mathrm{~A}$ NFET is chosen. Q2 is necessary to invert the PWM signal so it prop-
erly translates the duty cycle to the shunt dimming FET. Q2 also needs to be fast and rated for 5 V and fairly small current, therefore a 30V, 2A fast CMOS FET was chosen. R1 and R2 are $1 \Omega$ resistors to slow down the rising edge of the FETs slightly to prevent the gate from ringing. R3 is a $10 \mathrm{k} \Omega$ pull-up resistor to ensure the CMOS gate is pulled all the way to 5 V if a sub-5V PWM signal is applied to PWM2. The bypass capacitor (C5) for the 5 V power supply is chosen to be $0.1 \mu \mathrm{~F}$. See the Shunt FET Circuit Modification section for an improvement that can be made to this circuit.
Method \#3: Internal PWM dimming using the EN pin can be evaluated by removing the jumper from header J1. An external PWM signal can then be applied to the EN terminal to provide PWM dimming.
The Typical Waveforms section shows typical LED current waveforms during both types of PWM dimming.
The chosen components from step 10 are:

$$
\begin{aligned}
& \mathrm{C} 6=0.1 \mu \mathrm{~F} \\
& \mathrm{C} 9=2.2 \mathrm{nF} \\
& \mathrm{R} 1=\mathrm{R} 2=1 \Omega \\
& \mathrm{R} 3=10 \mathrm{k} \Omega \\
& \mathrm{R} 4=100 \Omega \\
& \mathrm{Q} 2 \rightarrow 30 \mathrm{~V}, 20 \mathrm{~A}, \mathrm{SOT}-6, \mathrm{CMOS} \\
& \mathrm{Q} 3 \rightarrow 100 \mathrm{~V}, 7.5 \mathrm{~A}, \mathrm{SOIC}-8, \mathrm{NMOS}
\end{aligned}
$$

## 11. BYPASS CAPACITOR

The internal regulator requires at least $1 \mu \mathrm{~F}$ of ceramic capacitance with a voltage rating of 16 V .
The chosen component from step 11 is:
$\mathrm{C} 4=1.0 \mu \mathrm{~F}$


External shunt FET dimming circuit with EN pin coupling

## Shunt FET Circuit Modification

When the shunt FET (Q3) is on, the LM3409 is driving current into a short, therefore a maximum off-time (typical $300 \mu \mathrm{~s}$ ) occurs followed by a minimum on-time. Maximum off-time followed by minimum on-time continues until Q3 is turned off. At low dimming frequencies and depending on the duty cycle, the inductor current may be at a very low level when the Q3 turns off. This will eliminate the benefits of using the shunt FET over the EN pin because the inductor will have to slew the current back to the nominal value anyways.
A simple modification to the external parallel FET dimming circuit will keep the inductor current close to its nominal value when Q3 is turned off. This modification will ensure that the rise time of the LED current is only limited by the turn-off time of the shunt FET as desired. The following circuit additions
allow for two different off-times to occur. When Q3 is off, the standard off-timer referenced from $\mathrm{V}_{\mathrm{O}}$ is set. However when the Q3 is on, a second off-timer referenced to the gate signal of the Q3 is enabled and a controlled (non-maximum) off-time is set.
This modification includes 2 extra diodes (i.e. BAT54H) and one resistor ( $\mathrm{R}_{\text {OFF2 }}$ ) and is only relevant when shunt FET PWM dimming below 10 kHz or so. In general, this second off-timer should be set to allow the inductor current to fall no more than $10 \%$ of its nominal value. A simple approximation can be used to find $\mathrm{R}_{\text {OFF2 } 2}$ :

$$
\mathrm{R}_{\mathrm{OFF} 2}<\frac{0.1 \times L \times \mathrm{I}_{\mathrm{LED}}}{\mathrm{C} 7 \times \mathrm{V}_{\mathrm{O}}}
$$



## Typical Waveforms

$\mathrm{T}_{\mathrm{A}}=+25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{IN}}=48 \mathrm{~V}$ and $\mathrm{V}_{\mathrm{O}}=42 \mathrm{~V}$.


20kHz 50\% EN pin PWM dimming


100kHz 50\% External FET PWM dimming


Analog dimming minimum $\left(\mathrm{V}_{\mathrm{ADJ}}=\mathbf{O V}\right)^{30093545}$


20kHz 50\% EN pin PWM dimming (rising edge)


100kHz 50\% External FET PWM dimming (rising edge)


Analog dimming maximum ( $\mathrm{V}_{\mathrm{ADJ}}$ open)

## Alternate Designs

Alternate designs with the LM3409HV evaluation board are possible with very few changes to the existing hardware. The evaluation board FETs and diodes are already rated higher than necessary for design flexibility. The input UVLO can remain the same and the input capacitance is sufficient for most designs, though the input voltage ripple will change. Other designs can evaluated by changing R6, R9, L1, and C8.

The table below gives the main specifications for five different designs and the corresponding values for R6, R9, L1 and C8. The RMS current rating of L1 should be at least $50 \%$ higher than the specified $\mathrm{I}_{\text {LED }}$. Designs 3 and 5 are optimized for best analog dimming range, while designs 1,2 , and 4 are optimized for best PWM dimming range. These are just examples, however any combination of specifications can be achieved by following the Design Procedure in the LM3409/09HV datasheet.

| Specification / <br> Component | Design 1 | Design 2 | Design 3 | Design 4 | Design 5 |
| :--- | :--- | :--- | :--- | :--- | :--- |
| Dimming Method | PWM | PWM | Analog | PWM | Analog |
| $\mathrm{V}_{\text {IN }}$ | 24 V | 36 V | 48 V | 65 V | 75 V |
| $\mathrm{~V}_{\mathrm{O}}$ | 14 V | 24 V | 35 V | 56 V | 42 V |
| $\mathrm{f}_{\mathrm{SW}}$ | 500 kHz | 450 kHz | 300 kHz | 350 kHz | 300 kHz |
| $\mathrm{I}_{\mathrm{LED}}$ | 1 A | 700 mA | 2 A | 3 A | 1.5 A |
| $\mathrm{~L}_{\mathrm{LED}}$ | 450 mA | 250 mA | 70 mA | 1 A | 80 mA |
| R 6 | $15.4 \mathrm{k} \Omega$ | $25.5 \mathrm{k} \Omega$ | $46.4 \mathrm{k} \Omega$ | $24.9 \mathrm{k} \Omega$ | $95.3 \mathrm{k} \Omega$ |
| R 9 | $0.2 \Omega$ | $0.3 \Omega$ | $0.12 \Omega$ | $0.07 \Omega$ | $0.15 \Omega$ |
| L 1 | $22 \mu \mathrm{H}$ | $68 \mu \mathrm{H}$ | $150 \mu \mathrm{H}$ | $15 \mu \mathrm{H}$ | $330 \mu \mathrm{H}$ |
| C 8 | None | None | $2.2 \mu \mathrm{~F}$ | None | $2.2 \mu \mathrm{~F}$ |

For more National Semiconductor product information and proven design tools, visit the following Web sites at:

| Products |  | Design Support |  |
| :--- | :--- | :--- | :--- |
| Amplifiers | www.national.com/amplifiers | WEBENCH® Tools | www.national.com/webench |
| Audio | www.national.com/audio | App Notes | www.national.com/appnotes |
| Clock and Timing | www.national.com/timing | Reference Designs | www.national.com/refdesigns |
| Data Converters | www.national.com/adc | Samples | www.national.com/samples |
| Interface | www.national.com/interface | Eval Boards | www.national.com/evalboards |
| LVDS | www.national.com/lvds | Packaging | www.national.com/packaging |
| Power Management | www.national.com/power | Green Compliance | www.national.com/quality/green |
| Switching Regulators | www.national.com/switchers | Distributors | www.national.com/contacts |
| LDOs | www.national.com/Ido | Quality and Reliability | www.national.com/quality |
| LED Lighting | www.national.com/led | Feedback/Support | www.national.com/feedback |
| Voltage Reference | www.national.com/vref | Design Made Easy | www.national.com/easy |
| PowerWise® Solutions | www.national.com/powerwise | Solutions | www.national.com/solutions |
| Serial Digital Interface (SDI) | www.national.com/sdi | Mil/Aero | www.national.com/milaero |
| Temperature Sensors | www.national.com/tempsensors | SolarMagicTM | www.national.com/solarmagic |
| Wireless (PLL/VCO) | www.national.com/wireless | PowerWise $® ~ D e s i g n ~$ <br> (Pniversity | www.national.com/training |

THE CONTENTS OF THIS DOCUMENT ARE PROVIDED IN CONNECTION WITH NATIONAL SEMICONDUCTOR CORPORATION ("NATIONAL") PRODUCTS. NATIONAL MAKES NO REPRESENTATIONS OR WARRANTIES WITH RESPECT TO THE ACCURACY OR COMPLETENESS OF THE CONTENTS OF THIS PUBLICATION AND RESERVES THE RIGHT TO MAKE CHANGES TO SPECIFICATIONS AND PRODUCT DESCRIPTIONS AT ANY TIME WITHOUT NOTICE. NO LICENSE, WHETHER EXPRESS, IMPLIED, ARISING BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.
TESTING AND OTHER QUALITY CONTROLS ARE USED TO THE EXTENT NATIONAL DEEMS NECESSARY TO SUPPORT NATIONAL'S PRODUCT WARRANTY. EXCEPT WHERE MANDATED BY GOVERNMENT REQUIREMENTS, TESTING OF ALL PARAMETERS OF EACH PRODUCT IS NOT NECESSARILY PERFORMED. NATIONAL ASSUMES NO LIABILITY FOR APPLICATIONS ASSISTANCE OR BUYER PRODUCT DESIGN. BUYERS ARE RESPONSIBLE FOR THEIR PRODUCTS AND APPLICATIONS USING NATIONAL COMPONENTS. PRIOR TO USING OR DISTRIBUTING ANY PRODUCTS THAT INCLUDE NATIONAL COMPONENTS, BUYERS SHOULD PROVIDE ADEQUATE DESIGN, TESTING AND OPERATING SAFEGUARDS.
EXCEPT AS PROVIDED IN NATIONAL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, NATIONAL ASSUMES NO LIABILITY WHATSOEVER, AND NATIONAL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF NATIONAL PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

## LIFE SUPPORT POLICY

## NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE CHIEF EXECUTIVE OFFICER AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

Life support devices or systems are devices which (a) are intended for surgical implant into the body, or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

National Semiconductor and the National Semiconductor logo are registered trademarks of National Semiconductor Corporation. All other brand or product names may be trademarks or registered trademarks of their respective holders.
Copyright® 2009 National Semiconductor Corporation
For the most current product information visit us at www.national.com

|  |  |  |  |
| :--- | :--- | :--- | :--- |
| National Semiconductor | National Semiconductor Europe | National Semiconductor Asia | National Semiconductor Japan |
| Americas Technical | Technical Support Center | Pacific Technical Support Center | Technical Support Center |
| Support Center | Email: europe.support@nsc.com |  |  |
| Email: support@nsc.com |  |  |  |
|  |  |  |  |

