## **Programmable Power Regulators Help Check Out Computer System Operating Margins**

It is a familiar situation that some computer systems which are functional with a 5V supply may run marginally at 5.1V but can show a solid failure at 5.3V (or, vice versa) even though all these voltages are within the system's specifications. The LM338 is an example of a monolithic voltage regulator which can be placed under computer control, and can trim the supply to a particular variation above (and below) the design-center voltage. Simultaneously the computer is exercised through a standard test sequence. Any deviation from correct functioning, at one supply voltage level or another, will serve as a warning of impending malfunction or failure. This test approach can be used for diagnostics, for troubleshooting, and for engineering evaluation. It can help detect skew, race conditions, timing problems, and noise and threshold problems.

## HERE'S HOW

During normal operation, the latch (IC 1) is programmed to have its Q1 and Q2 outputs HIGH, and its Q3 and Q4 LOW. Then R4 and R5 are connected effectively in parallel with R6, and V<sub>OUT</sub> is adjusted to 5V. If Q4 is commanded HIGH, the net conductance from the adjust bus to ground will decrease, and VOUT will rise 3% to 5.151V. Conversely if Q1 is commanded LOW. the output voltage will fall 3.3% to 4.835V. The complete list of output voltages (in approximately 3.2% steps) is shown in Table I, covering a ±9.5% total range

The same basic function can be accomplished for  $-5.2\ensuremath{\text{V}}$ regulators (as are used for ECL) using LM337 negative adjustable regulators. If the command is from TTL latches, the circuit of Figure 2 will be suitable to interface between the (0V and 2.4V) logic levels and the saturated PNP collectors National Semiconductor Linear Brief 49 **Robert Pease** October 1980



Computer System Operating Margins

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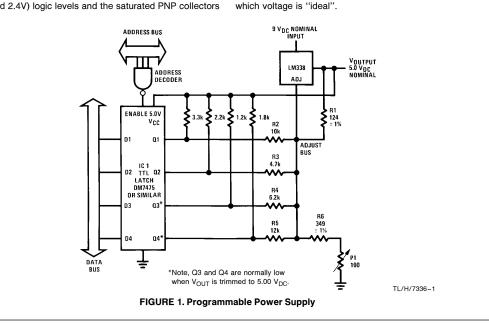
as shown. The resistors R101-R104 are switched by transistors Q101-Q104 in a similar way to Figure 1. Note that the resistors in Figure 2 are in a binary-weighted proportion. To decrease V<sub>OUT</sub> by 2%, just change Q4 to LOW; but to increase VOLT by 2%, set Q1 HIGH and Q2, Q3, Q4 all LOW, in a standard offset binary scheme.

**TABLE I. Available Trim Range** 

Q1	Q2	Q3	Q4	V <sub>OUT</sub>	%∆V <sub>OUT</sub>
1	1	0	0	5.000V	(trimmed)
1	1	0	1	5.151V	+3.0%
1	1	1	0	5.299V	+6.0%
1	1	1	1	5.469V	+9.4%
0	1	0	0	4.835V	-3.3%
1	0	0	0	4.669V	-6.6%
0	0	0	0	4.526V	-9.5%

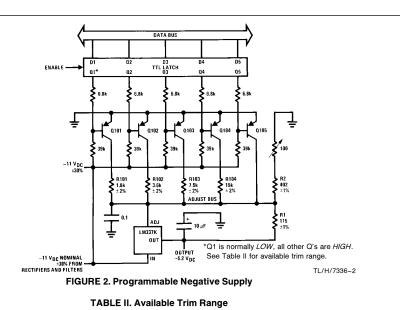
Figure 2 also provides another feature. If Q5 goes LOW, Q105 will saturate and pull the adjust bus to within 100 mV of ground, and the  $V_{\mbox{OUT}}$  will collapse to  $\,-135\mbox{V}.$  The negative supply will be effectively shut down, and the computer will draw substantially zero power.

In an extreme case of automation, the computer could trim the -5.2V supply to the "best" value, and the trimpot would be completely superfluous. The circuit of Figure 2 has a trim resolution of 3% steps, and can set  $V_{\mbox{OUT}}$  well within 2% of the ideal value, so long as some measurement has decided



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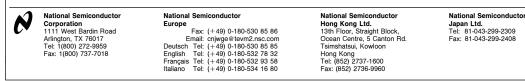


Q1	Q2	Q3	Q4	Vout	%∆V <sub>ОUT</sub>
0	1	1	1	5.200V	(trimmed)
0	1	1	0	5.110V	-1.7%
0	1	0	1	5.025V	-3.4%
0	1	0	0	4.944V	-4.9%
0	0	1	1	4.853V	-6.7%
0	0	1	0	4.779V	-8.1%
0	0	0	1	4.707V	-9.5%
0	0	0	0	4.638V	-10.8%
1	0	0	0	5.310V	+2.1%
1	0	0	1	5.409V	+4.0%
1	0	1	0	5.513V	+6.0%
1	0	1	1	5.622V	+8.1%
1	1	0	0	5.757V	+ 10.7%
1	1	0	1	5.880V	+ 13.1%
1	1	1	0	6.010V	+ 15.6%
1	1	1	1	6.147V	+ 18.2%

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