LMP7300 Single Precision Comparator with Reference Evaluation Boards (SOIC and MSOP)

The following evaluation boards are designed to demonstrate the LMP7300 micropower precision comparator, with precision voltage reference. National recommends the use of these boards as an aid in the evaluation and characterization of the LMP7300.

- -551013114- For the LMP7300 MO8A Eval (SOIC pkg).
- -551013115- For the LMP7300 MUA8A Eval (MSOP pkg).

The boards have identical circuit configurations and layouts. All components are surface mount 0805 except the test points for supply and voltage measurement. The layout input and output will accommodate either BNC or SMA connectors.

Basic Configuration as Threshold Detector

The LMP7300 evaluation boards are designed to provide maximum flexibility while investigating different circuit configurations. The values chosen are for micropower precision level threshold applications where supply noise is at a minimum. If supply noise is present, provision has been made to add decoupling as needed. While most component values are shown, some are application specific and should be defined by the user. For example, the bridge gain can be changed with R1, R2, and R4, while supply line decoupling can be improved with C2 and C6. The potentiometers, R6 and R7, can be used to quickly trim the trip points.

As shown in *Figure 1*, the input signal, V_{IN} is brought onto the board through a BNC or SMA connector and divided by the bridge gain. If the desired V_{IN} trigger level is set to twice V_{REF}, the comparator will trip around V_{REF}. The signal path is connected via jumper JP1 to the comparator's inverting input and JP2 for the non-inverting input. The bridge gain is set to $\sim \frac{1}{2}$ with R1 and R2 both stuffed as 1 M Ω and R4 set to 0 Ω for initial setup, then trimmed for high or low threshold detection. There is a provision for a resistor R3 to be placed between the input pins for large hysteresis levels.

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Hysteresis

The hysteresis for the LMP7300, unlike most comparators, is totally independent of the supply, the input conditions, or the output connections. The part design allows for five hysteresis settings: asymmetric, symmetric, positive only, negative only, or none. The hysteresis is easily determined by two resistors in a voltage divider format with the precision 2.048V voltage reference tied to the top resistor and ground set to the bottom. The center voltage tap is connected to device pin HYSTP, or HYSTN to fix the hysteresis at 1 mV/mV. Trim potentiometers R6 and R7 are provided for quick and easy resolution of the proper hysteresis. Resistors R5 and R10 are set to 1 M Ω to establish $\sim 2 \ \mu A$ current through the divider to ground. The hysteresis is the voltage measured across the trim potentiometer resistance or V_{REF} - the voltage at the voltage divider center tap. A maximum of 100 to 130 mV is recommended.

Reconfigure Application with Jumper Pins

- For negative threshold detection: The input signal V_{IN} is normally above the threshold, dropping below the threshold. Connect V_{IN} to the non-inverting input with JP2, and V_{REF} to the inverting input with JP3
- For positive threshold detection: The input signal V_{IN} is normally below the threshold, rising above the threshold. Connect V_{IN} to the inverting input with JP1, and V_{REF} to the non-inverting input with JP4.
- For split supply use JP5.
- For single supply use JP6.

Bypassing the Voltage Reference

In noisy supply line applications, bypassing the voltage reference to improve line regulation with respect to supply line transients is recommended. The reference output can drive a bypass capacitance of 0.05 μ F, with minimum peaking and no oscillation. For larger capacitors, add a small value of resistance in series with the capacitor. A 190 Ω resistor in series with a 5 μ F ceramic capacitor is recommended.

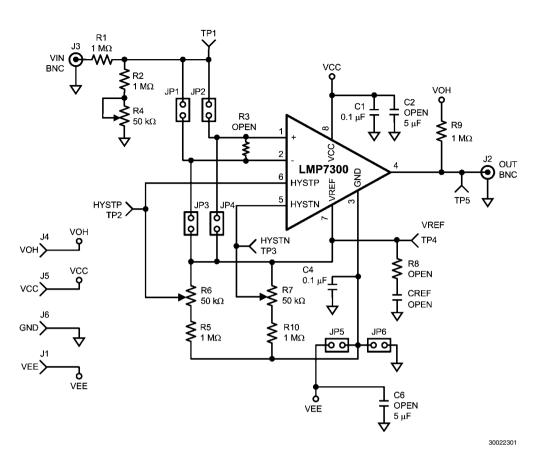


FIGURE 1. Evaluation Board Schematic

Output Stage

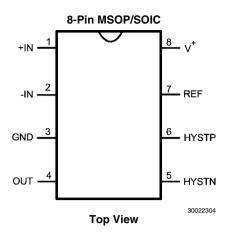
The comparator employs an open collector output stage that can drive both voltage and current loads, such as solenoids, lamps, heater, etc. Since the pull-up resistor can be taken to any voltage between 0.5V and 12V, independent of the comparator supply voltage, interfacing with mixed voltage systems is straight forward. The open collector design also

TABLE 1. Bill of Materials

permits wired-OR connection to the multiple comparator outputs. This output stage easily interfaces with various logic inputs, such as TTL and CMOS. When the positive input is above the negative input, the output is in an off or high state. The output voltage high level is determined by the pull-up supply. For the reverse condition, when the positive input is below the negative input, the output is in an on or low state. The maximum load current is around 10 mA for a low state.

| ID | Part Number | Туре | Size | Parameters | Qty | Vendor |
|---------------------|-----------------|---------------|-----------------|---------------------------|-----|----------|
| U1 | LMP7300 | Comparator | 8-Pin SOIC/MSOP | | 1 | NSC |
| R8 | P191CCT-ND | Resistor | 805 | 190Ω, 1%, 1/8W, Open | | Digi-Key |
| R1, R2, R5, R9, R10 | P100MCCT-ND | Resistor | 805 | 1.00 MΩ, 1%, 1/8W | 5 | Digi-Key |
| R4, R6, R7 | 3299Y-503LF-ND | Potentiometer | | 50 kΩ, 1/2W | | Digi-Key |
| JP1 - JP6 | 929450-01-36-ND | Header | 2-pin, 0.1" | | | Digi-Key |
| C1, C4 | PCC1828CT-ND | Capacitor | 805 | 0.1 μF, X7R, 10%, 25V | | Digi-Key |
| C2, C6, CREF | | Capacitor | | 5 µF, X7R, 10%, 25V, Open | 3 | Digi-Key |
| J2,J3 | 22C4690 | BNC | PCB Edge Mount | | 2 | Newark |
| J1 | 5009K-ND | LG Test Point | | Yellow | 1 | Digi-Key |
| J4 | 5007K-ND | LG Test Point | | White | 1 | Digi-Key |
| J5 | 5005K-ND | LG Test Point | | Red | 1 | Digi-Key |
| J6 | 5006K-ND | LG Test Point | | Black | 1 | Digi-Key |
| TP1 – TP5 | 5004K-ND | Test Point | | Black | 5 | Digi-Key |
| Jumper Shunt | 5900D | Short | 2 pin, 0.1" | 0Ω Black | | Digi-Key |

Connection Diagram



Pin Descriptions

| +IN | Non-Inverting | The +IN has a common-mode voltage range from 1V above the negative rail to, and | | |
|-------|-------------------------|--|--|--|
| | Comparator Input | including, the positive rail. Internal ESD diodes, connected from the +IN pin to the rails, | | |
| | | protect the input stage from overvoltage. If the input voltage exceeds the rails, the diodes | | |
| | | turn on and clamp the input to a safe level. | | |
| –IN | Inverting Comparator | The -IN has a common-mode voltage range from 1V above the negative rail to, and | | |
| | Input | including, the positive rail. Internal ESD diodes, connected from the -IN pin to the rails, | | |
| | | protects the input stage from overvoltage. If the input voltage exceeds the rails, the diodes turn on and clamp the input to a safe level. | | |
| GND | Ground | This pin may be connected to a negative DC voltage source for applications requiring a | | |
| | | dual supply. If connected to a negative supply, decouple this pin with 0.1 μF ceramic | | |
| | | capacitor to ground. The internal reference output voltage is referenced to this pin. GND | | |
| | | is the die substrate connection. | | |
| OUT | Comparator Output | The output is an open-collector. It can drive voltage loads by using a pullup resistor, drive | | |
| | | current loads by sinking a maximum output current. This pin may be taken to maximum of | | |
| | | +12V with respect to the ground pin, irrespective of supply voltage. | | |
| HYSTN | Negative Hysteresis Pin | This pin sets the lower trip voltage V_{IL} . The common mode range is from 1V above the | | |
| | | negative rail to V_{CC} . The input signal must fall below V_{IL} for the comparator to switch from | | |
| | | high to low state. | | |
| HYSTP | Positive Hysteresis pin | This pin sets the upper trip voltage $V_{\mathrm{IH}}.$ The common mode range is from 1V above the | | |
| | | negative rail to $V_{\text{CC}}.$ The input signal must rise above V_{IH} for the comparator to switch from | | |
| | | low to high state. | | |
| REF | Reference Voltage | This is the output pin of a 2.048V band gap precision reference. | | |
| | Output Pin | | | |
| V+ | Positive Supply | The supply voltage range is 2.7V to 12V. Decouple this pin with 0.1 μF ceramic capacitor | | |
| | Terminal | to ground. | | |

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Board Layout

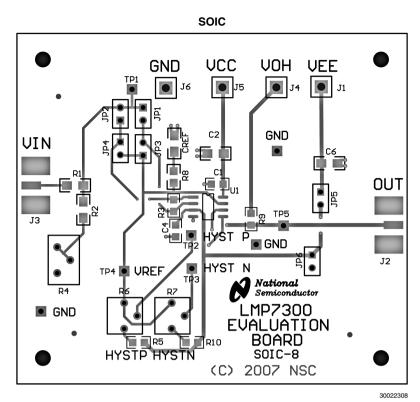


FIGURE 2. Top Layer

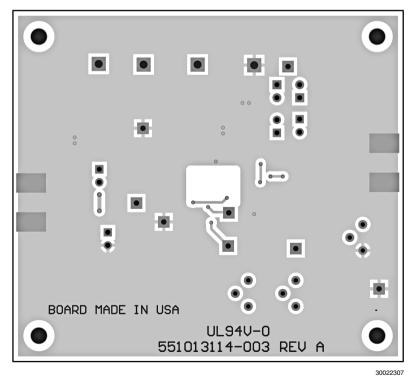


FIGURE 3. Bottom Layer

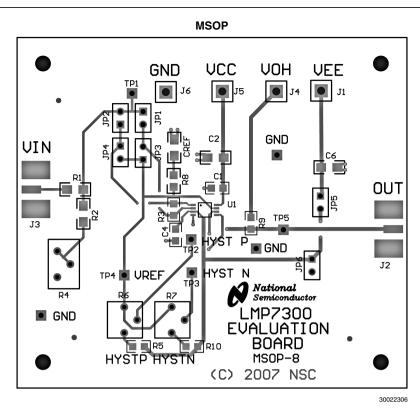


FIGURE 4. Top Layer

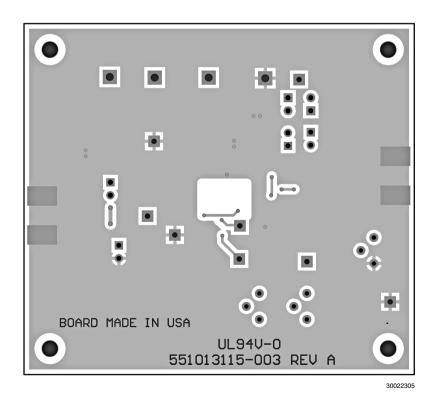


FIGURE 5. Bottom Layer

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Notes

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