LM49100 Evaluation Board User's Guide

National Semiconductor
Application Note 1622
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Quick Start Guide

Connect the I²C signal generation and interface board to a computer's parallel port.

Apply 2.7V to 5.5V power supply's positive output to the "VDD" pin on jumper "VDD GND". Connect the power supply's ground return to the "GND" pin also on the aforementioned jumper.

Connect the supplied 6-wire (one pin is a No Connect) cable between the I²C signal generation and interface board and the 6-pin connector (I²C Interface; one pin is a No Connect) on the LM49100 demonstration board. If logic levels other than those set by V_{DD} are required, jumper J1 needs to be connected and a separate supply applied to the 2–pin header with the I2CVDD pin, with respect to ground.

Headphone amplifier output mode: Apply a stereo input audio signal to jumpers Left Input and Right Input. Apply the sources' +input pins and GND pins, respectively, to the demonstration board.

Connect a load (≥16Ω) to header HPL (left headphone) and another load (≥16Ω) to header HPR (right headphone). The HPL pin and HPR pin carries the output signals from the two amplifiers, and each of the other pins connecting to ground making this configuration single-ended connections.

Differential mono amplifier output mode: Apply a mono differential input audio signal to jumper Mono Input. Apply the sources' +input and –input to the middle two pins of the 4-pin jumper. The two outer pins are connected to ground, which are used when the mono input is configured as single-ended instead of differential.

Connect the 32Ω load across the two pins (differential) of the Speaker jumper on the demonstration board.

Apply power. Make measurements. Enjoy the sound.

Introduction

To help the user investigate and evaluate the LM49100's performance and capabilities, a fully populated demonstration board is available from the National Semiconductor Corporation's Audio Products Group. This board is shown in Figure 1. Connected to an external power supply (2.7V to 5.5V), a signal source and an I²C controller (or signal source), the LM49100 demonstration board easily demonstrate the amplifier's features.

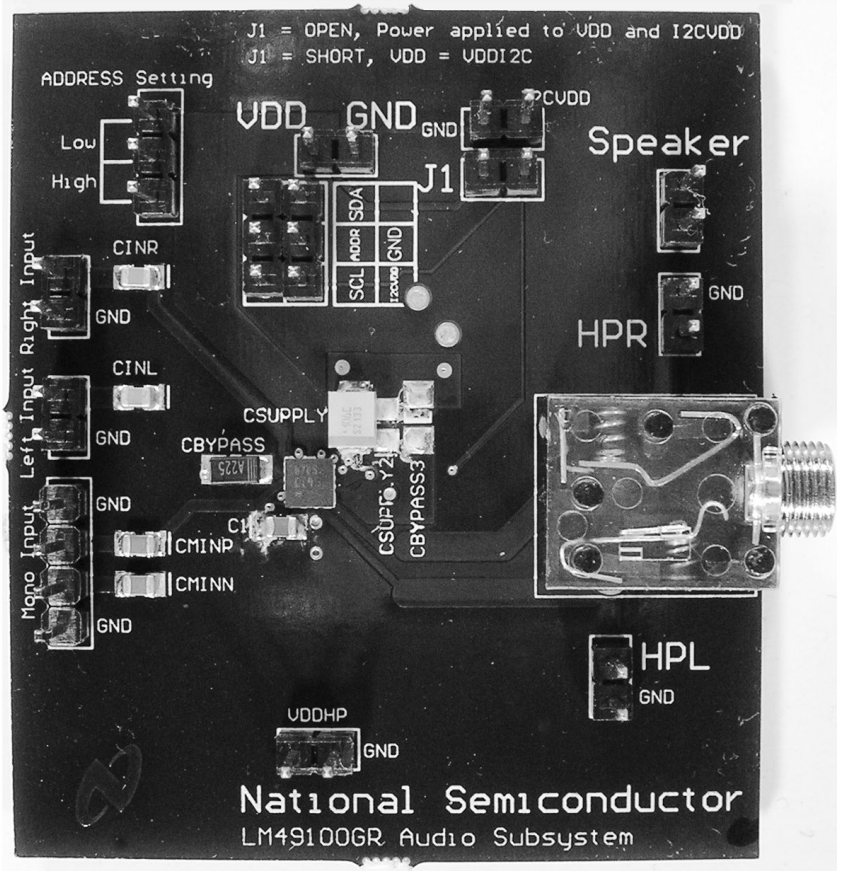

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FIGURE 1. The LM49100 Demonstration Board

General Description

The LM49100 is a fully integrated audio subsystem capable of delivering 1.275W of continuous average power into a mono 8Ω bridged-tied load (BTL) with 1% THD+N and with a 5V power supply. The LM49100 also has a stereo true-ground headphone amplifier capable of 50mW per channel of continuous average power into a 32Ω single-ended (SE) loads with 1% THD+N.

The LM49100 has three input channels. One pair of SE inputs can be used with a stereo signal. The other input channel is fully differential and may be used with a mono input signal. The LM49100 features a 32-step digital volume control and ten distinct output modes. The mixer, volume control, and device mode select are controlled through an I²C compatible interface.

Thermal overload protection prevent the device from being damaged during fault conditions. Superior click and pop suppression eliminates audible transients on power-up/down and during shutdown.

Operating Conditions

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage V_{DD}LS	$2.7V \le V_{DD}LS \le 5.5V$
Supply Voltage V_{DD}HP	$2.4\ V \le V_{DD}HP \le 2.9V$
I²C Voltage (V_{DD}I²C)	$1.7V \le V_{DD}I^2C \le 5.5V$
	$V_{DD}HP \le V_{DD}LS$
	$V_{DD}I^2C \le V_{DD}LS$
■ Temperature Range	$-40°C \le T_A \le 85°C$

Board Features

The LM49100 demonstration board has all of the necessary connections, using 0.100" headers, to apply the power supply voltage, the audio input signals, and the I²C signal inputs. The amplified audio signal is available on both a stereo headphone jack and auxiliary output connections.

Also included with the demonstration board is an I²C signal generation board and software. With this board and the software, the user can easily control the LM49100's, shutdown function, mute, and stereo volume control. Figure 1 shows the software's graphical user interface.

Schematic

Figure 2 shows the LM49100 Demonstration Board schematic. Refer to Table 3 for a list of the connections and their functions.

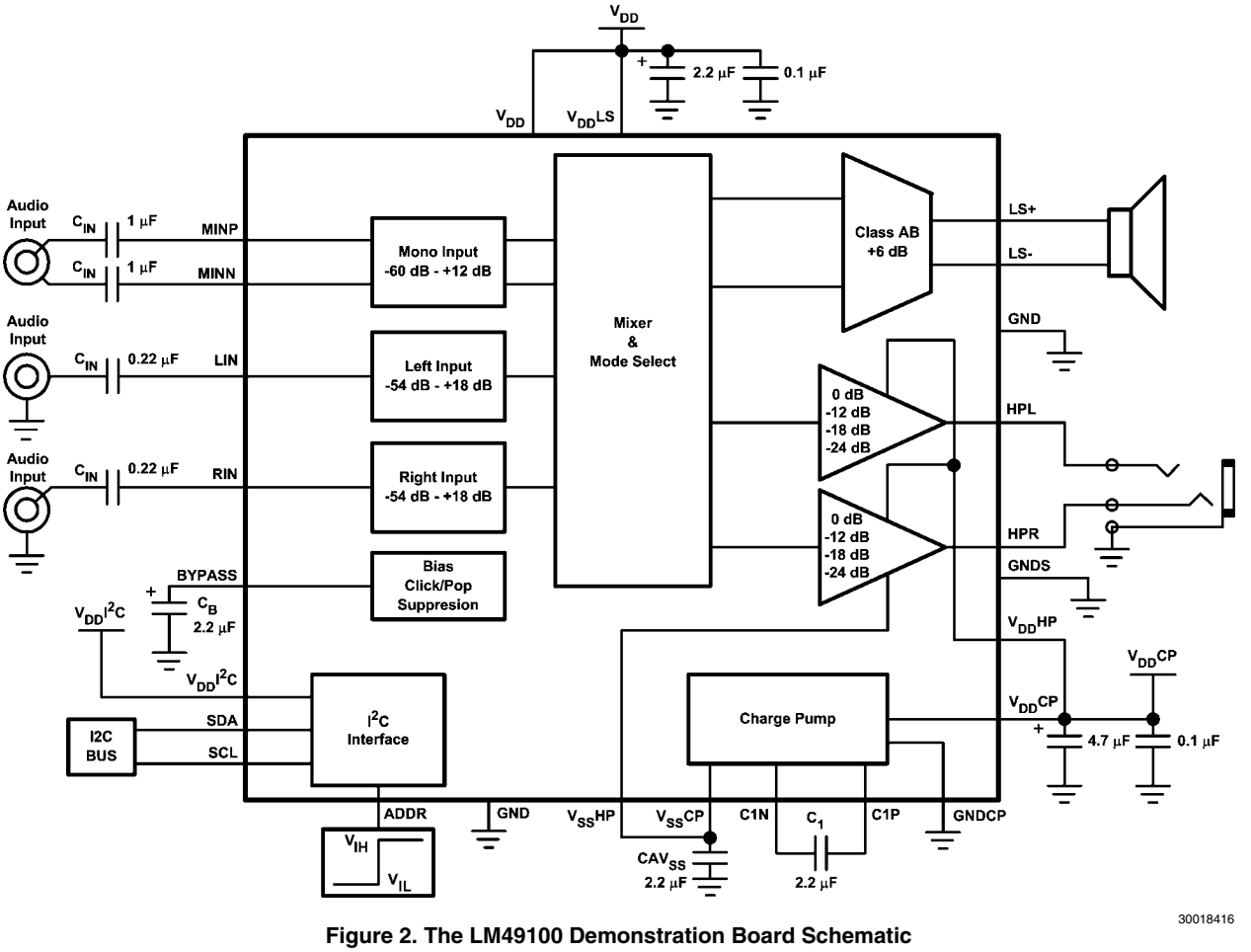

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Figure 2. The LM49100 Demonstration Board Schematic

Connections

Connecting to the world is accomplished through the 0.100" headers on the LM49100 demonstration board. The functions of the different headers are detailed in Table 1.

TABLE 1. LM49100 Demonstration Board Connections

Header or Jumper Designation	Function or Use
V_{DD}/GND	Main power supply and ground for the demonstration board.
V_{DDHP}/GND	Headphone power supply for the headphone amplifier which creates split supplies: for the positive voltage is converted by switch capacitor creating a negative voltage of equal magnitude.
J1	A shorted J1 connects VDD directly to I²CVDD. An opened J1 disconnects VDD and I²CVDD. If open, a separate power supply connected to I²CVDD/GND header must be applied.
I^2CV_{DD}	Header to apply an independent I²C power supply when J1 is open.
Right Input	This is the connection to the amplifier's single-ended right channel input.
Left Input	This is the connection to the amplifier's single-ended left channel input.
Mono Input	This is the connection to the amplifier's differential or single-ended left/right mono input. The center two pins are the differential inputs, or single-ended inputs, while the outside pins are the grounds.
Address Setting	Used to set the address of the device. Normally set at "Low" on the demonstration board.
I²C Interface	This is the input connection for the I²C serial clock and serial data signals. The demonstration board has an adjacent I²C label identifying each pin.
Speaker	Two-pin header used to connect the "+" and "-" terminals of the mono speaker.
HPR	This is the connection to the amplifier's single-ended, ground referenced right channel output. The "HPR" label refers to the output pin and "GND" is the corresponding ground.
HPL	This is the connection to the amplifier's single-ended, ground referenced left channel output. The "HPL" label refers to the output pin and "GND" is the corresponding ground.

Power Supply Sequencing

The LM49100 uses two power supply voltages: V_{DD} for the analog circuitry and I^2CV_{DD}, which defines the digital control logic high voltage level. To ensure proper functionality, apply V_{DD} first, followed by I^2CV_{DD}. If one power supply is used, V_{DD} and I^2CV_{DD} can be connected together. The part will power-up with both channels shutdown, the volume control set to minimum, and the mute function active.

I²C Signal Generation Board and Software

The I²C signal generation and interface board, along with the LM49100 software, will generate the address byte and the data byte used in the I²C control data transaction. To use the I²C signal generation and interface board, please plug it into a PC's parallel port (on either a notebook or a desktop computer).

The software comes with an installer. To install, unzip the file titled "LM49100_Software." After the file unzips, double-click the "setup.exe" file. After it launches, please follow the installer's instructions. Setup will create a folder named "LM49100" in the "Program" folder on the "C" disk (if the default is used) along with a shortcut of the same name in the "Programs" folder in the "Start" menu.

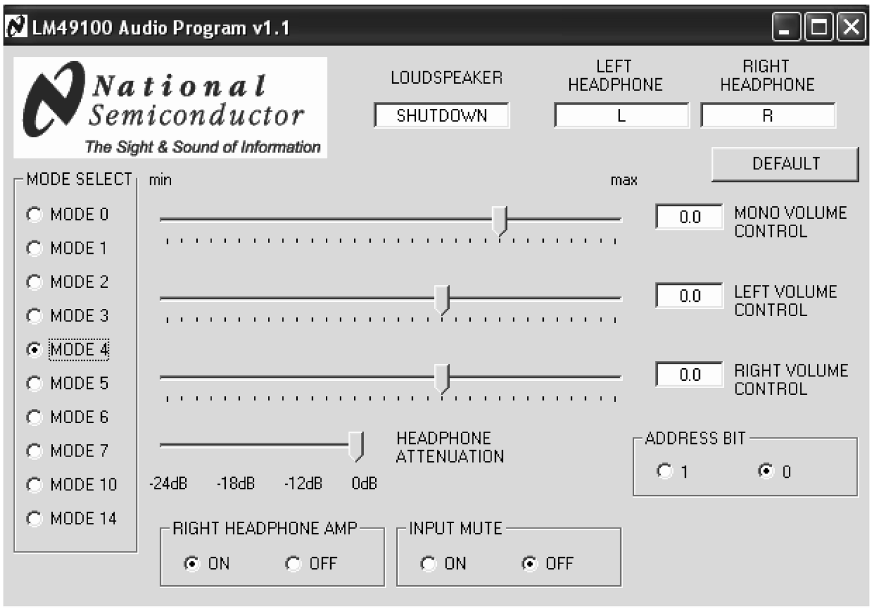

Figure 3. The LM49100 Software User's Interface

The LM49100 program includes controls for the amplifier's volume control, individual channel shutdown, and the mute function. The control program's on-screen user interface is shown in Figure 3.

The Default button is used to return the LM49100 to its power-on reset state: minimum volume setting, shutdown on both amplifiers active, and mute active.

The LM49100's stereo **VOLUME CONTROL** has 32 steps and a gain range of –76dB to 18dB. It is controlled using the slider located at the bottom of the program's window. Each time the slider is moved from one tick mark to another, the program updates the amplifier's volume control.

LEFT CHANNEL, BOTH CHANNELS, and RIGHT CHANNEL controls each have two buttons. For the left and right channel control, the "ON" button activates its respective channel, whereas the "OFF" button places its respective channel in shutdown mode. Selecting the **BOTH CHANNELS** "ON" button simultaneously activates both channels, whereas selecting the "OFF" button places channels in shutdown mode.

PCB Layout Guidelines

This section provides general practical guidelines for PCB layouts that use various power and ground traces. Designers should note that these are only "rule-of-thumb" recommendations and the actual results are predicated on the final layout.

POWER AND GROUND CIRCUITS

Star trace routing techniques (returning individual traces back to a central point rather than daisy chaining traces together in a serial manner) can have a major positive impact on low-level signal performance. Star trace routing refers to using individual traces that radiate from a signal point to feed power and ground to each circuit or even device. This technique may require greater design time, but should not increase the final price of the board.

For good THD+N and low noise performance and to ensure correct power-on behavior at the maximum allowed supply voltage, a local 2.2µF power supply bypass capacitor should be connected as physically close as possible to the V_{DD}LS pin.

AVOIDING TYPICAL DESIGN/LAYOUT PROBLEMS

Avoid ground loops or running digital and analog traces parallel to each other (side-by-side) on the same PCB layer. When traces must cross over each other, do so at 90 degrees. Running digital and analog traces at 90 degrees to each other from the top to the bottom side as much as possible will minimize capacitive noise coupling and crosstalk.

Bill of Materials

Designator	Part Description	Value	Tolerance	Rating	Package Type	Manufacturer	Manufacturer's Part Number
C1	Tantalum Capacitor	2.2µF			1206		
CAVSS	Tantalum Capacitor	2.2µF			1206		
CBYPASS	Tantalum Capacitor	2.2µF			1206		
CCPUMP1	Tantalum Capacitor	4.7µF			1206		
CCPUMP2	Multilayer Ceramic Capacitor	0.1µF			0805		
CINL	Multilayer Ceramic Capacitor	0.22µF			0805		
CINR	Multilayer Ceramic Capacitor	2.2µF			0805		
CMINN	Multilayer Ceramic Capacitor	1µF			0805		
CMINP	Multilayer Ceramic Capacitor	1µF			0805		
CSUPPLY1	Tantalum Capacitor	2.2µF			1206		
CSUPPLY2	Multilayer Ceramic Capacitor	0.1µF			0805		
HPL	2–pin header, 100 mil pitch				1x2 Header		
HPR	2–pin header, 100 mil pitch				1x2 Header		
I2C 6–pin Header	6–pin header, 100 mil pitch				2x3 Header		
Left Input	2–pin header, 100 mil pitch				1x2 Header		
Mono Input	4–pin header, 100 mil pitch				1x2 Header		
Right Input	2–pin header, 100 mil pitch				1x2 Header		
Speaker	2–pin header, 100 mil pitch				1x2 Header		
Stereo Headphone Jack	Headphone Jack						

Designator	Part Description	Value	Tolerance	Rating	Package Type	Manufacturer	Manufacturer's Part Number
V_{DD}	2–pin header, 100 mil pitch				1x2 Header		
U1	Mono Class AB Audio Subsystem with a True-Ground Headphone Amplifier					National Semiconductor	LM49100GR

Demonstration Board PCB Layout

Figures 4 through 9 show the different layers used to create the LM49100 four-layer demonstration board. Figure 4 is the silkscreen that shows parts location. Figure 5 is the top layer. Figure 6 is the upper inner layer. Figure 7 is the lower middle layer. Figure 8 is the bottom layer. Figure 9 is the bottom silkscreen layer.

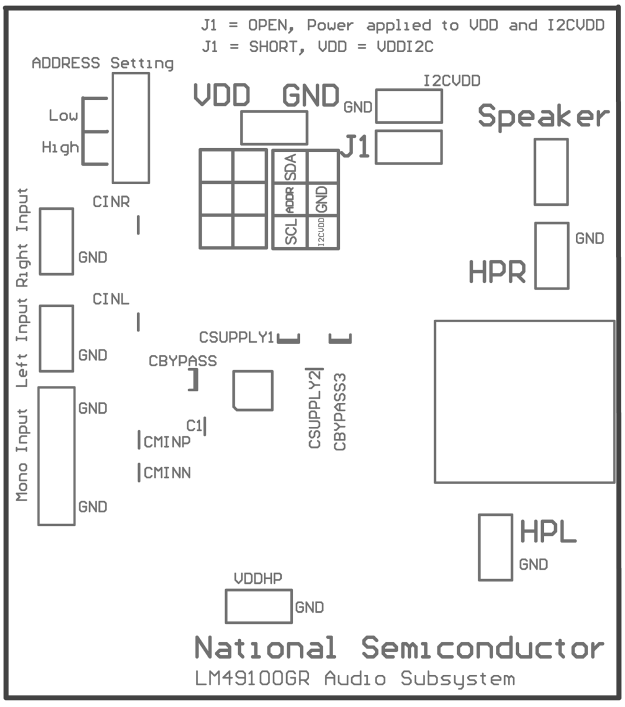

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Figure 4. Top Overlay

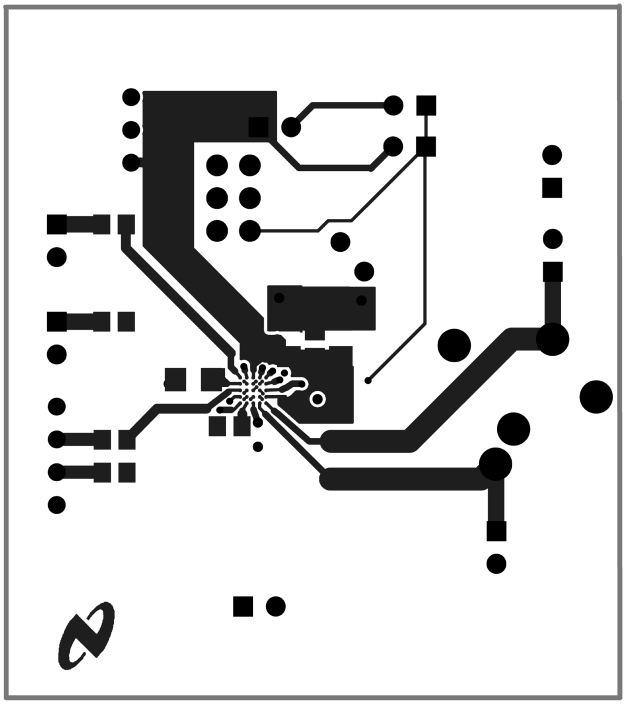

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Figure 5. Top Layer

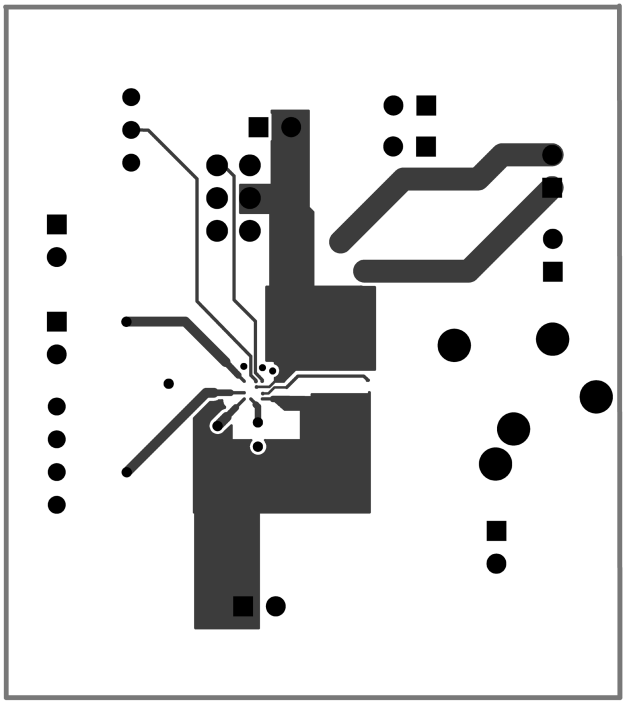

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Figure 6. Signal 1

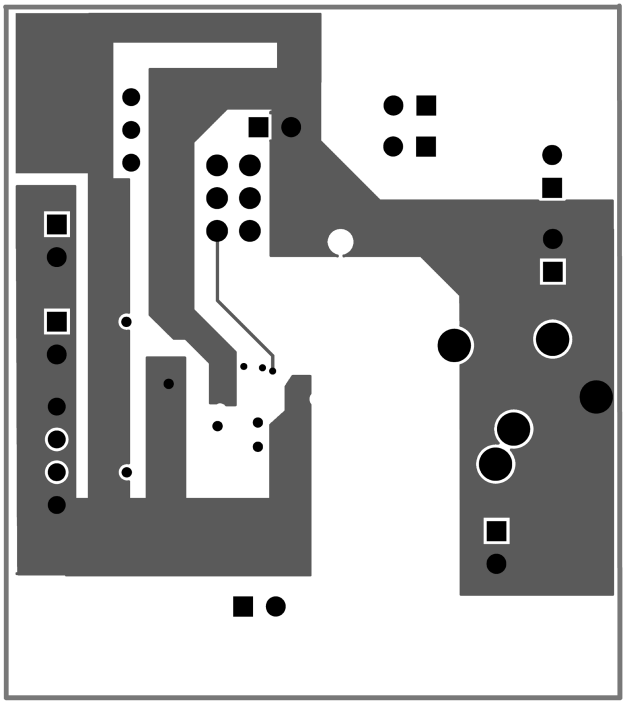

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Figure 7. Signal 2

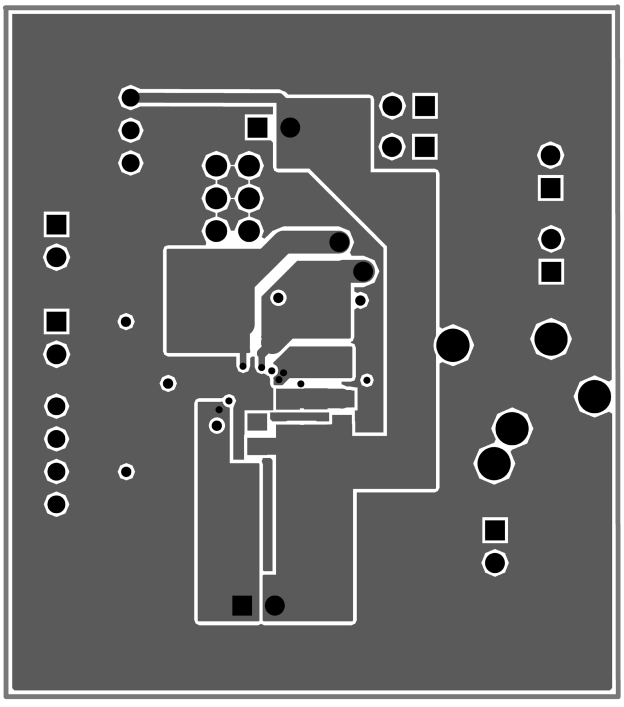

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Figure 8. Bottom Layer

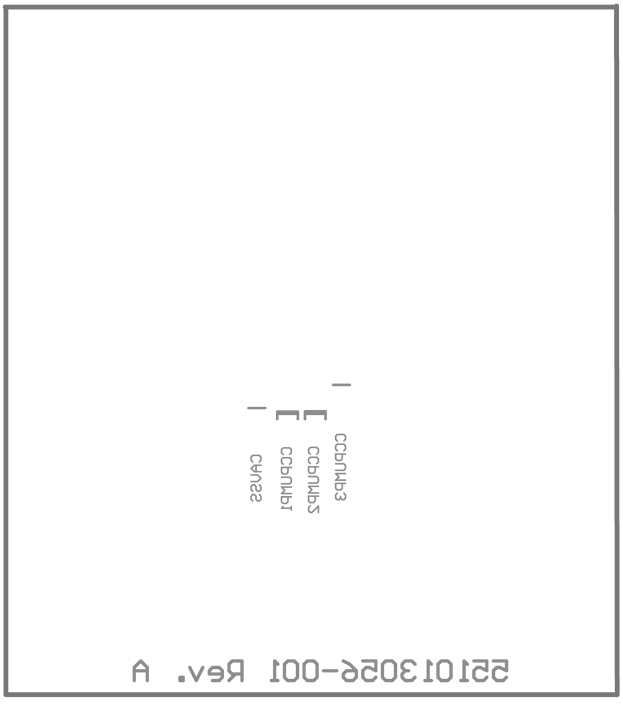

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Figure 9. Bottom Overlay

Typical Demonstration Board Audio Performance

Typical THD+N versus Frequency performance curves at V_{DD} = 3.6V, 3V, and 5V for 16Ω and 32Ω are shown in Figure 10 through Figure 15, respectively. Typical THD+N versus Output Power performance curves at V_{DD} = 3V, 3.6V, and 5V for 32Ω and 8Ω are shown in Figure 16 and Figure 17, respectively.

Figure 10. THD+N vs Frequency
V_{DD} = 3.6V, R_L = 8Ω, P_O = 320mW
BW = 22kHz, LS, Mode 1

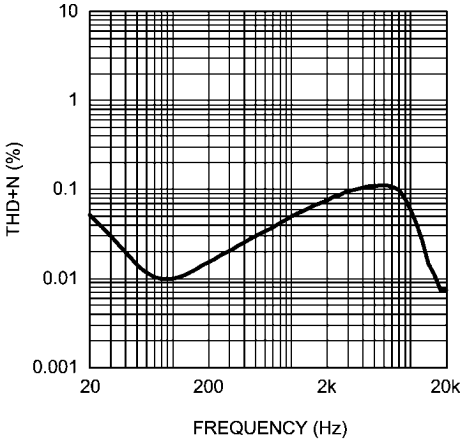

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Figure 11. THD+N vs Frequency
V_{DD} = 3.6V, R_L = 32Ω, P_O = 25mW
BW = 22kHz, HP, Mode 4, 7

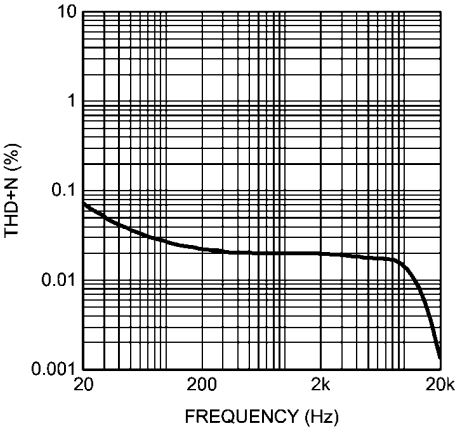

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Figure 12. THD+N vs Frequency
V_{DD} = 3V, R_L = 8Ω, P_O = 215mW
BW = 22kHz, LS, Mode 1

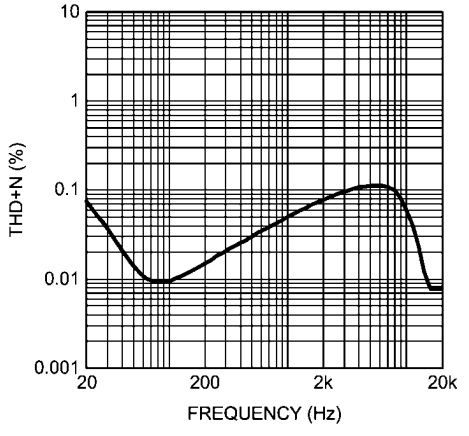

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Figure 13. THD+N vs Frequency
V_{DD} = 3V, R_L = 32Ω, P_O = 25mW
BW = 22kHz, HP, Mode 4, 7

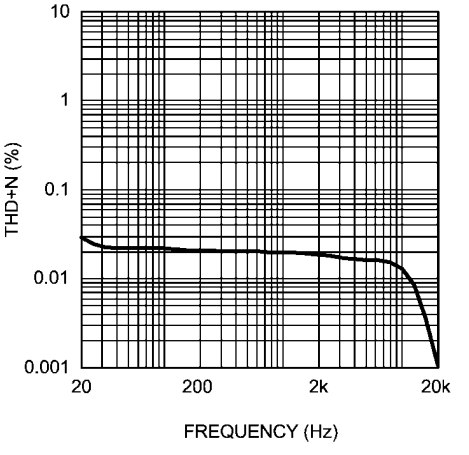

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Figure 14. THD+N vs Frequency
V_{DD} = 5V, R_L = 8Ω, P_O = 630mW
BW = 22kHz, Loudspeaker, Mode 1

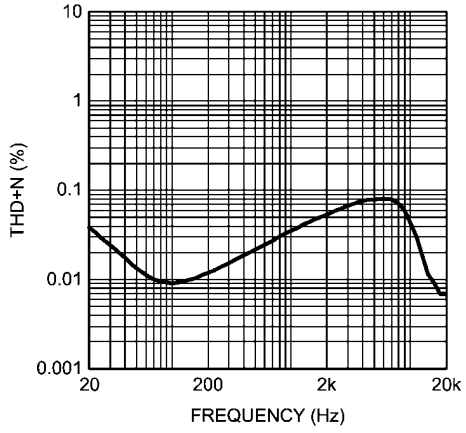

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Figure 15. THD+N vs Frequency
V_{DD} = 5V, R_L = 32Ω, P_O = 25mW
BW = 22kHz, Headphone, Mode 4, 7

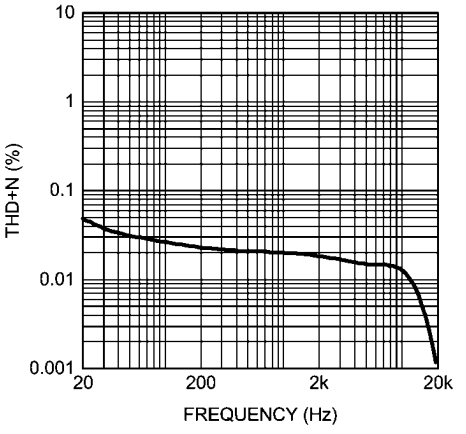

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Figure 16. THD+N vs Output Power
R_L = 32Ω, f = 1kHz
BW = 22kHz, HP, Mode 4

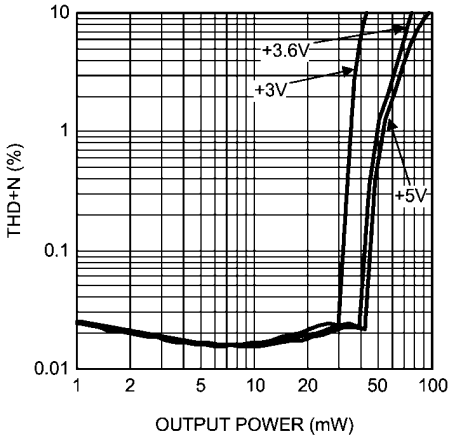

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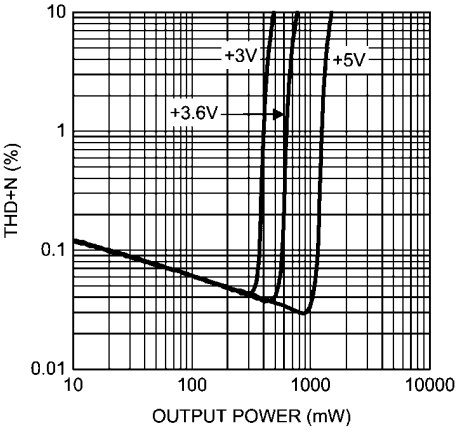
Figure 17. THD+N vs Output Power
R_L = 8Ω, f = 1kHz
BW = 22kHz, LS , Mode 1



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LM49100 Control Tables

TABLE 2. I²C Control Register Table

The LM49100 is controlled through an I²C compatible interface. The I²C chip address is 0xF8 (ADR pin = 0) or 0xFAh (ADDR pin = 1).

	D7	D6	D5	D4	D3	D2	D1	D0
Modes Control	0	0	1	1	MC3	MC2	MC1	MC0
HP Volume (Gain) Control	0	1	INPUT_MUTE	0	0	HPR_SD	HPVC1	HPVC0
Mono Volume Control	1	0	0	MV4	MV3	MV2	MV1	MV0
Left Volume (Gain) Control	1	1	0	LV4	LV3	LV2	LV1	LV0
Right Volume (Gain) Control	1	1	1	RV4	RV3	RV2	RV1	RV0

TABLE 3. Headphone Attenuation Control

The following bits have added for extra headphone output attenuation:

Gain Select	HPVC1	HPVC0	Gain, dB
0	0	0	0
1	0	1	−12
2	1	0	−18
3	1	1	−24

TABLE 4. Output Mode Selection

Output Mode Number	MC3	MC2	MC1	MC0	Handsfree Mono Output	Right HP Output	Left HP Output
0	0	0	0	0	SD	SD	SD
1	0	0	0	1	$2 \times G_M \times M$	SD	SD
2	0	0	1	0	SD	$G_{HP} \times (G_M \times M)$	$G_{HP} \times (G_M \times M)$
3	0	0	1	1	$2 \times (G_L \times L + G_R \times R)$	SD	SD
4	0	1	0	0	SD	$G_{HP} \times (G_R \times R)$	$G_{HP} \times (G_L \times L)$
5	0	1	0	1	$2 \times (G_L \times L + G_R \times R + G_M \times M)$	SD	SD
6	0	1	1	0	SD	$G_{HP} \times (G_R \times R + G_M \times M)$	$G_{HP} \times (G_L \times L + G_M \times M)$
7	0	1	1	1	$2 \times (G_L \times L + G_R \times R)$	$G_{HP} \times (G_R \times R)$	$G_{HP} \times (G_L \times L)$
10	1	0	1	0	$2 \times (G_L \times L + G_R \times R)$	$G_{HP} \times (G_M \times M)$	$G_{HP} \times (G_M \times M)$
14	1	1	1	0	$2 \times (G_L \times L + G_R \times R)$	$G_{HP} \times (G_R \times R + G_M \times M)$	$G_{HP} \times (G_L \times L + G_M \times M)$

G_L — Left channel gain
G_R — Right channel gain
G_M — Mono channel gain
G_{HP} — Headphone Amplifier gain
R — Right input signal
L — Left input signal
SD — Shutdown
M — Mono input signal

TABLE 5. Mono/Stereo Left/Stereo Right Input Gain Control

Volume Step	MV4/LV4/RV4	MV3/LV3/RV3	MV2/LV2/RV2	MV1/LV1/RV1	MV0/LV0/RV0	R/L Gain, dB	MonoGain, dB
1	0	0	0	0	0	−54	−60
2	0	0	0	0	1	−47	−53
3	0	0	0	1	0	−40.5	−46.5
4	0	0	0	1	1	−34.5	−40.5
5	0	0	1	0	0	−30.0	−36
6	0	0	1	0	1	−27	−33
7	0	0	1	1	0	−24	−30
8	0	0	1	1	1	−21	−27
9	0	1	0	0	0	−18	−24
10	0	1	0	0	1	−15	−21
11	0	1	0	1	0	−13.5	−19.5
12	0	1	0	1	1	−12	−18
13	0	1	1	0	0	−10.5	−16.5
14	0	1	1	0	1	−9	−15
15	0	1	1	1	0	−7.5	−13.5
16	0	1	1	1	1	−6	−12
17	1	0	0	0	0	−4.5	−10.5
18	1	0	0	0	1	−3	−9
19	1	0	0	1	0	−1.5	−7.5
20	1	0	0	1	1	0	−6
21	1	0	1	0	0	1.5	−4.5
22	1	0	1	0	1	3	−3
23	1	0	1	1	0	4.5	−1.5
24	1	0	1	1	1	6	0
25	1	1	0	0	0	7.5	1.5
26	1	1	0	0	1	9	3
27	1	1	0	1	0	10.5	4.5
28	1	1	0	1	1	12	6
29	1	1	1	0	0	13.5	7.5
30	1	1	1	0	1	15	9
31	1	1	1	1	0	16.5	10.5
32	1	1	1	1	1	18	12

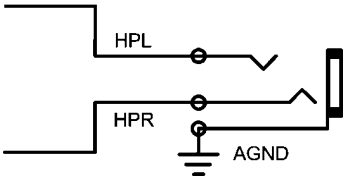
Application Information

MINIMIZING CLICK AND POP

To minimize the audible click and pop heard through a headphone, maximize the input signal through the corresponding volume (gain) control registers and adjust the output amplifier gain accordingly to achieve the user's desired signal gain. For example, setting the output of the headphone amplifier to -24dB and setting the input volume control gain to 24dB will reduce the output offset from 7mV (typical) to 2.2mV (typical). This will reduce the audible click and pop noise significantly while maintaining a 0dB signal gain.

SIGNAL GROUND NOISE

The LM49100 has proprietary suppression circuitry, which provides an additional -50dB (typical) attenuation of the headphone ground noise and its incursion into the headphone. For optimum utilization of this feature the headphone jack ground should connect to the AGND (E3) bump.



I²C PIN DESCRIPTION

SDA: This is the serial data input pin.

SCL: This is the clock input pin.

ADDR: This is the address select input pin.

I²C COMPATIBLE INTERFACE

The LM49100 uses a serial bus which conforms to the I²C protocol to control the chip's functions with two wires: clock (SCL) and data (SDA). The clock line is uni-directional. The data line is bi-directional (open-collector). The LM49100's I²C compatible interface supports standard (100kHz) and fast (400kHz) I²C modes. In this discussion, the master is the controlling microcontroller and the slave is the LM49100.

The I²C address for the LM49100 is determined using the ADDR pin. The LM49100's two possible I²C chip addresses are of the form $111110X_10$ (binary), where $X_1 = 0$, if ADDR pin is logic LOW; and $X_1 = 1$, if ADDR pin is logic HIGH. If the I²C interface is used to address a number of chips in a system, the LM49100's chip address can be changed to avoid any possible address conflicts.

The bus format for the I²C interface is shown in Figure 2. The bus format diagram is broken up into six major sections:

The "start" signal is generated by lowering the data signal while the clock signal is HIGH. The start signal will alert all devices attached to the I²C bus to check the incoming address against their own address.

The 8-bit chip address is sent next, most significant bit first. The data is latched in on the rising edge of the clock. Each address bit must be stable while the clock level is HIGH.

After the last bit of the address bit is sent, the master releases the data line HIGH (through a pull-up resistor). Then the master sends an acknowledge clock pulse. If the LM49100 has received the address correctly, then it holds the data line LOW during the clock pulse. If the data line is not held LOW during the acknowledge clock pulse, then the master should abort the rest of the data transfer to the LM49100.

The 8 bits of data are sent next, most significant bit first. Each data bit should be valid while the clock level is stable HIGH.

After the data byte is sent, the master must check for another acknowledge to see if the LM49100 received the data.

If the master has more data bytes to send to the LM49100, then the master can repeat the previous two steps until all data bytes have been sent.

The "stop" signal ends the transfer. To signal "stop", the data signal goes HIGH while the clock signal is HIGH. The data line should be held HIGH when not in use.

I²C INTERFACE POWER SUPPLY PIN (V_{DD}I²C)

The LM49100's I²C interface is powered up through theV_{DD} I²C pin. The LM49100's I²C interface operates at a voltage level set by the V_{DD} I²C pin which can be set independent to that of the main power supply pin V_{DD}. This is ideal whenever logic levels for the I²C interface are dictated by a microcontroller or microprocessor that is operating at a lower supply voltage than the main battery of a portable system.

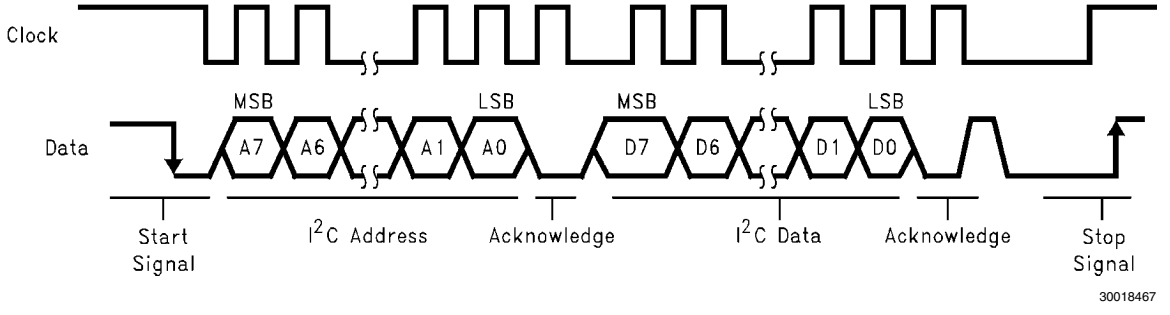


FIGURE 2. I²C Bus Format

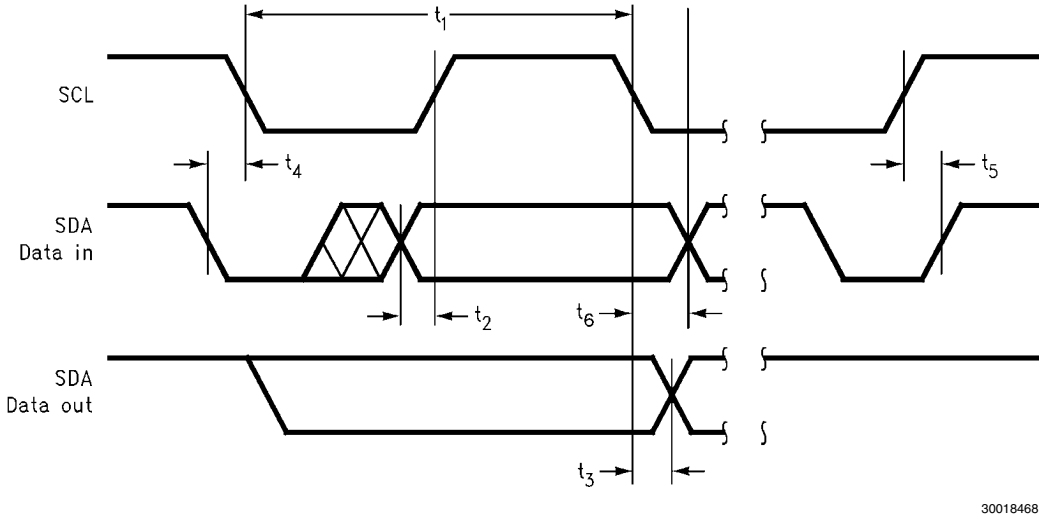


FIGURE 3. I²C Timing Diagram

PCB LAYOUT AND SUPPLY REGULATION CONSIDERATIONS FOR DRIVING 8Ω LOAD

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by an 8Ω load from 158.3mW to 156.4mW. The problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

BRIDGE CONFIGURATION EXPLANATION

The LM49100 drives a load, such as a loudspeaker, connected between outputs, LS+ and LS-.

This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between LS- and LS+ and driven differentially (commonly referred to as "bridge mode").

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. Theoretically, this produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited and that the output signal is not clipped.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing LS- and LS+ outputs at half-supply. This eliminates the coupling capacitor that single supply, single-ended amplifiers require. Eliminating an output coupling capacitor in a typical single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as loudspeakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier.

A direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation. The LM49100 has a pair of bridged-tied amplifiers driving a handsfree loudspeaker, LS. The maximum internal power dissipation operating in the bridge mode is twice that of a single-ended amplifier. From Equation (1), assuming a 5V power supply and an 8Ω load, the maximum MONO power dissipation is 634mW.

$$P_{DMAX\text{-}LS} = 4(V_{DD})^2 / (2\pi^2 R_L)\text{: Bridge Mode} \quad (1)$$

The LM49100 also has a pair of single-ended amplifiers driving stereo headphones, HPR and HPL. The maximum internal power dissipation for HPR and HPL is given by equation (2). Assuming a 2.8V power supply and a 32Ω load, the maximum power dissipation for L_{OUT} and R_{OUT} is 49mW, or 99mW total.

$$P_{DMAX\text{-}HPL} = 4(V_{DD}HP)^2 / (2\pi^2 R_L)\text{: Single-ended Mode} \quad (2)$$

The maximum internal power dissipation of the LM49100 occurs when all three amplifiers pairs are simultaneously on; and is given by Equation (3).

$$P_{DMAX\text{-}TOTAL} = P_{DMAX\text{-}LS} + P_{DMAX\text{-}HPL} + P_{DMAX\text{-}HPR} \quad (3)$$

The maximum power dissipation point given by Equation (3) must not exceed the power dissipation given by Equation (4):

$$P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA} \quad (4)$$

The LM49100's T_{JMAX} = 150°C. In the GR package, the LM49100's θ_{JA} is 50.2°C/W. At any given ambient temperature T_A, use Equation (4) to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation (4) and substituting $P_{DMAX-TOTAL}$ for P_{DMAX} results in Equation (5). This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the LM49100's maximum junction temperature.

$$T_A = T_{JMAX} - P_{DMAX-TOTAL}\, \theta_{JA} \quad (5)$$

For a typical application with a 5V power supply and an 8Ω load, the maximum ambient temperature that allows maximum mono power dissipation without exceeding the maximum junction temperature is approximately 114°C for the GR package.

$$T_{JMAX} = P_{DMAX-TOTAL}\, \theta_{JA} + T_A \quad (6)$$

Equation (6) gives the maximum junction temperature T_{JMAX}. If the result violates the LM49100's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures.

The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases. If the result of Equation (3) is greater than that of Equation (4), then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 1µF in parallel with a 0.1µF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 4.7µF tantalum bypass capacitor and a parallel 0.1µF ceramic capacitor connected between the LM49100's supply pin and ground. Keep the length of leads and traces that connect capacitors between the LM49100's power supply pin and ground as short as possible.

SELECTING EXTERNAL COMPONENTS

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitor (C_{IN} in Figure 1). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the loudspeakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using loudspeakers and headphones with this limited frequency response reap little improvement by using large input capacitor.

The internal input resistor (R_i), typical 12.5kΩ, and the input capacitor (C_{IN}) produce a high pass filter cutoff frequency that is found using Equation (7).

$$f_c = 1 / (2\pi R_i C_{IN}) \quad (7)$$

Bypass Capacitor Value Selection

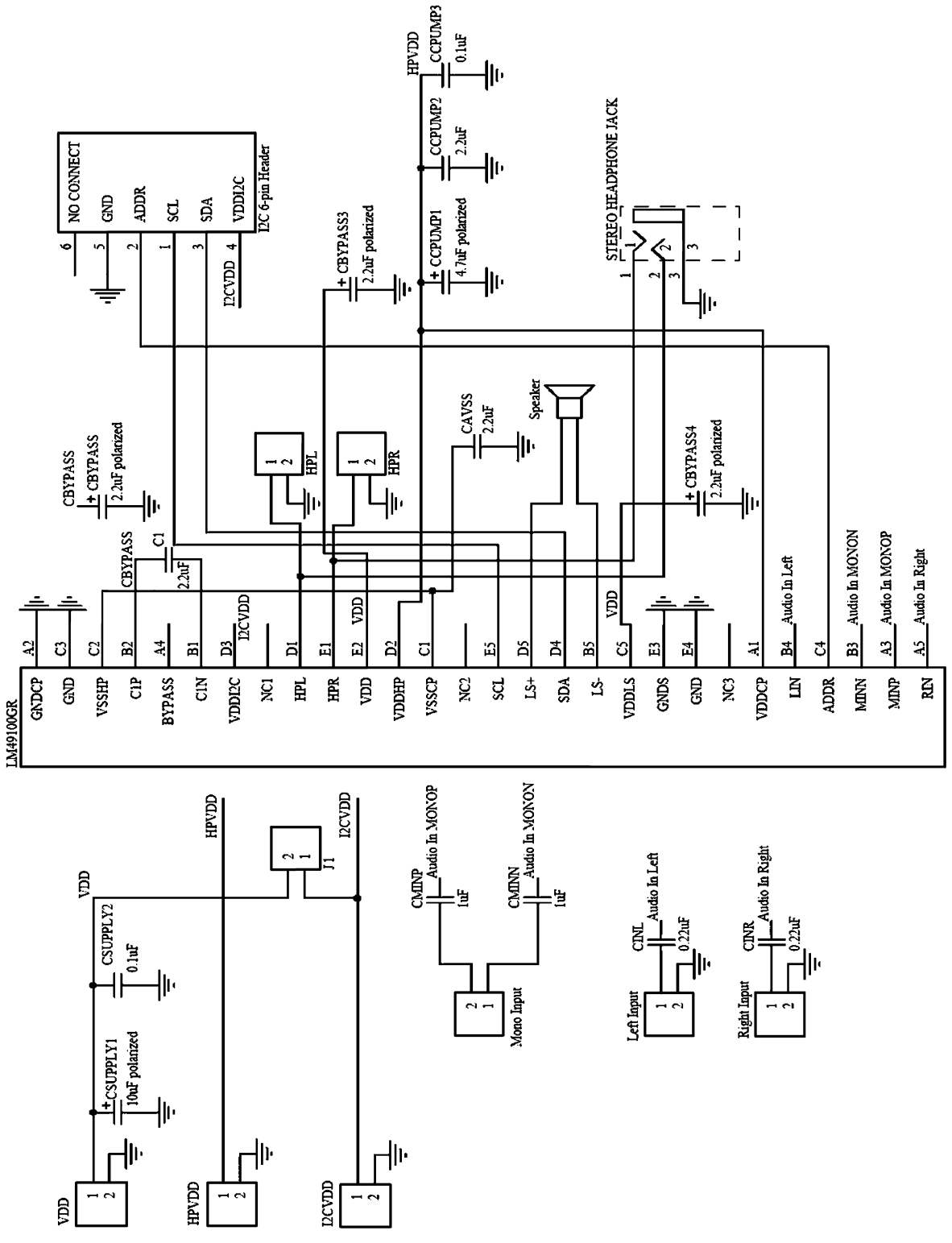
Besides minimizing the input capacitor size, careful consideration should be paid to value of C_B, the capacitor connected to the BYPASS pin. Since C_B determines how fast the LM49100 settles to quiescent operation, its value is critical when minimizing turn-on pops. Choosing C_B equal to 2.2µF along with a small value of C_i (in the range of 0.1µF to 0.33µF), produces a click-less and pop-less shutdown function. As discussed above, choosing C_{IN} no larger than necessary for the desired bandwidth helps minimize clicks and pops. C_B's value should be in the range of 4 to 5 times the value of C_{IN} . This ensures that output transients are eliminated when power is first applied or the LM49100 resumes operation after shutdown.

Since National Semiconductor is constantly pursuing the best package performance possible, please refer to the following web page for possible updates to the µSMD package information presented in Appendix D: <http://www.national.com/an/AN/AN-1112.pdf.

Appendix C Micro SMD Wafer Level Chip Scale Package, PCB, Layout, and Mounting Considerations

Refer to Application Notes (AN-1112) for more information on Micro SMD Wafer Level Chip Scale Package.

Demo Board Schematic



Revision History

Rev	Date	Description
1.0	10/1907	Initial release.

Notes

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