DS90UR241/124 Spread Spectrum Tolerance Support

National Semiconductor
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Compliance to EMI limits is often a challenge. Spread spectrum clocking is commonly used to minimize EMI. The effect of modulating periodic signals, both clock and data, reduces the peak emissions by spreading the energy over a range of frequencies. The DS90UR241 and DS90UR124 chipset allows the use of spread spectrum clock and data inputs. The following is a discussion of spread spectrum clock characteristics and the interaction with DS90UR241/124 chipset.

Spread Spectrum Modulation

Two key parameters, frequency deviation and modulation frequency, are used to define a spread spectrum output. Most spread spectrum generators will modulate the fundamental clock frequency by several percent. This modulation may be "center spread" or "down spread". The rate of this frequency change, modulation frequency, is often quite slow in comparison to the fundamental clock frequency - typically in the 10's of kHz range.

Table 1 provides guidance for the frequency deviation and modulation frequencies supported by the DS90UR241/124 chipset. This data is based on testing with an ideal source. The input clock signal was modulated by the triangle output of an arbitrary waveform generator. There was a direct connection between serializer and deserializer (no cable). No effects of additional jitter or cable length are included.

Additional factors associated with spread spectrum operation must also be considered. A modulated clock output may contain additional higher frequency jitter components – beyond the modulation frequency. It is important that this additional jitter not exceed the input jitter tolerance of the downstream device. Per the DS90UR241 specification, the input jitter tolerance is ±100ps (200ps pk-pk) at the maximum operating frequency of 43MHz. This value scales with input clock period. For example, at 33MHz the recommended input clock pk-pk jitter maximum increases to 260ps. Please refer to the Appendix for a description of measuring peak-to-peak jitter.

The frequency profile of the modulated signal is also important. There are two common modulation profiles – triangle and Lexmark ("Hershey Kiss"). Both apply a fixed modulation rate to the clock signal, and are proven to effectively reduce EMI. The DS90UR241/124 is targeted to support these two profiles. Note that some other profiles do exist, with slightly different behavior (i.e. varying the modulation rate over a range of frequencies).

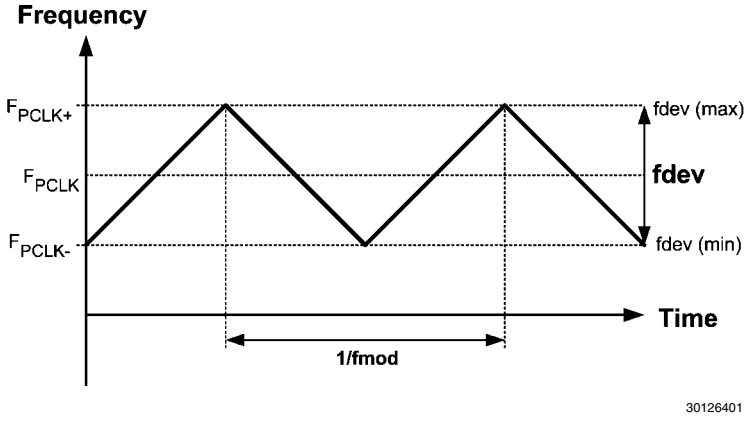

FIGURE 1. SSC Triangle Modulation

TABLE 1. Frequency and Modulation Frequencies for SSC

Maximum f_{dev}	Maximum f_{mod}	
	PCLK = 33 MHz	PCLK = 8 MHz
±4% center spread (8% total)	20 kHz	5 kHz
±2% center spread (4% total)	50 kHz	25 kHz

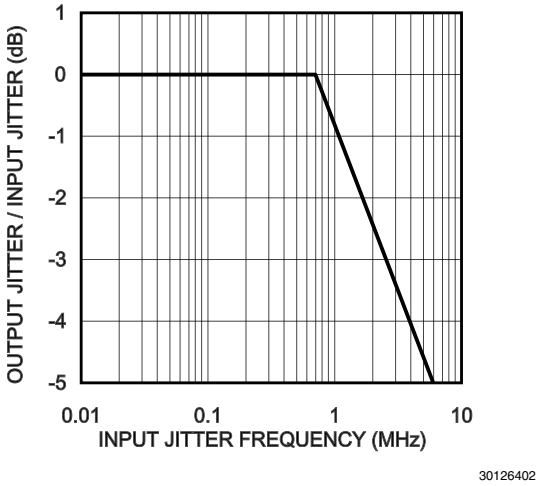

FIGURE 2. Example of PLL Jitter Transfer

When viewing the frequency spectra, the energy should be spread evenly across a range as defined by the frequency deviation. Outside of the specified range, the energy should quickly reduce to baseline levels. Additional "peaks" outside the desired deviation range are undesirable, resulting in a high frequency component which the PLL will not track.

Theory of Operation: Serializer and Deserializer PLL Response to Jitter

The bandwidth of the device PLL determines its fundamental response to jitter. Input jitter with a frequency below the bandwidth of the PLL – "low frequency jitter" – will be tracked and passed to the output of the PLL. Input jitter with a frequency above the bandwidth of the PLL – "high frequency jitter" – will be attenuated at the serial output. A typical PLL jitter transfer curve is shown in *Figure 2*. This illustrates gain (ratio of PLL input to output jitter) vs. the frequency of the jitter.

At the serializer input, jitter frequencies below the serializer bandwidth will be tracked by the PLL, and passed along the serial link to the downstream deserializer. Jitter with a frequency above the serializer bandwidth will be attenuated to some degree as defined by the PLL's jitter transfer curve. This high frequency jitter must not exceed the jitter tolerance of the serializer input.

Now let's consider the input to the deserializer. As with the serializer, any jitter below the deserializer bandwidth will be tracked by the PLL and pass to the deserializer's outputs. Frequencies above the deserializer bandwidth are not tracked, and must be considered with respect to the receiver's input jitter tolerance specification.

Response to SSC source

Spread spectrum clock sources modulate at frequencies well below the bandwidth of the PLLs. This low frequency modulation is easily tracked by the PLLs, and passes along cleanly to the output of the deserializer. However, the generated SSC signal will have additional frequency components, some of which may appear as high frequency jitter. Depending upon the frequency and magnitude of these additional jitter components, input jitter tolerance may be violated and potentially impact the ability to accurately recover serialized data. Thus the quality of the SSC generated output is important in the selection of an SSC device. It is recommended that the user select the minimum spread spectrum f_{dev} and f_{mod} necessary to achieve EMC compliance.

Appendix — Jitter Measurements

It is important to understand the high frequency jitter contribution of a spread spectrum clock source. The high frequency peak-to-peak jitter can be measured using a real time scope combined with jitter analysis software. When analyzing the peak-to-peak jitter, a high pass filter should be applied. This filter value should be set at approximately the bandwidth of the PLL. This focuses the analysis on the high-frequency jitter, and ignores the intentional modulation frequency of the spread spectrum device.

Notes

Notes

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