DP83847 to DP83848C/I/YB PHYTER System Rollover Document

National Semiconductor
Application Note 1470
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October 2006

Purpose

This is an informational document detailing points to be considered when updating an existing 10/100 Mb/s Ethernet design, using National Semiconductor's DP83847 Ethernet Physical Layer (PHY) product, to the new DP83848 PHYTER® product. Although the basic functions of the device are similar, differences include feature set, pin functions, package and pinout, and possibly register operation. The impact to a design is dependant on which, and how, features of the previous device are used or implemented.

1.0 Required Changes

This section documents the hardware changes required to transition to DP83848C/I/YB. There are three minor but required circuit changes, which are required for proper operation of the device.

1.1 PACKAGE

DP83848C/I/YB uses 48LQFP package. The differences in package between DP83848C/I/YB and DP83847 are shown in *Table 1*. For more information on the 48–LQFP package please visit http://www.national.com/packaging/folders/vbh48a.html.

TABLE 1. Packaging Differences

	DP83848C/I/YB	DP83847
Package	48-LQFP	56-LLP
Footprint	7x7mm	9x9mm
Package Drawing	VBH48A	LQA56A

1.2 PINOUT

DP83847 has 56 pins while DP83848C/I/YB has 48 pins. Please see Appendix A for the list of pins not applicable in DP83848C/I/YB and the pinmap from DP83847 to DP83848C/I/YB.

1.3 PCB MODIFICATION

This section describes the DP83847 circuit design modification required to use the DP83848C/I/YB in a similar PCB.

1.3.1 PFBOUT

Parallel capacitors (10uF Tantalum capacitor and 0.1uF) should be placed close to pin 23 (PFBOUT, the output of the regulator) in DP83848C/I/YB and pin 42 (C1, the output of the regulator) in DP83847. In DP83848C/I/YB, Pin 18 (PFBIN1) and 37 (PFBIN2) should be externally connected to pin 23 as shown in *Figure 1*. A small 0.1uF capacitor should be placed close to pin 18 and pin 37. DP83847 does not require a similar connection.

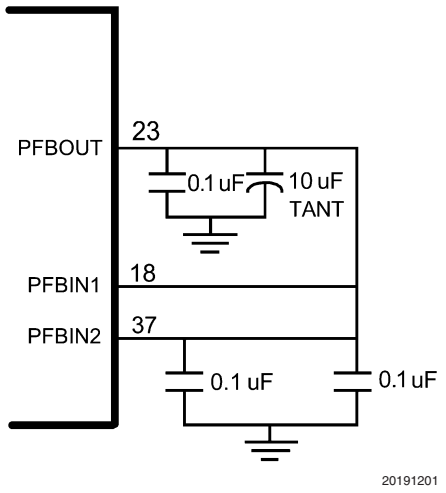

FIGURE 1. Special Connection in DP83848C/I/YB

1.3.2 Bias resistor

Internal circuitry biasing of the DP83848C/I/YB has changed from previous devices.

TABLE 2. Bias Resistor Values

	DP83848C/I/YB	DP83847
Bias Resistor Value	4.87K Ohm	10K Ohm

1.3.3 Termination and PMD Biasing

Termination of the PMD receive pair (TPRD+/-) on previous Physical Layer devices consisted of a pair of 54.9 Ohms, AC biased to GND. This value, when seen in parallel with the internal receiver circuitry, provided an equivalent of 100 Ohms impedance. In DP83848C/I/YB the internal receiver circuitry has changed and now requires a pair of 49.9 Ohm resistors, biased to VDD of the device.

This matching of the termination resistors and common biasing between the receiver and transmitter of the DP83848C/I/YB allows the addition of the Auto-MDIX feature to the device.

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1.0 Required Changes (Continued)

TABLE 3. Termination and Biasing Differences

	DP83848C/I/YB	DP83847
TX Termination	49.9 Ohms	49.9 Ohms
TX Bias	3.3V	3.3V
RX Termination	49.9 Ohms	54.9 Ohms
RX Bias	3.3V	AC to GND

Refer to the next set of figures for a graphic explanation of this.

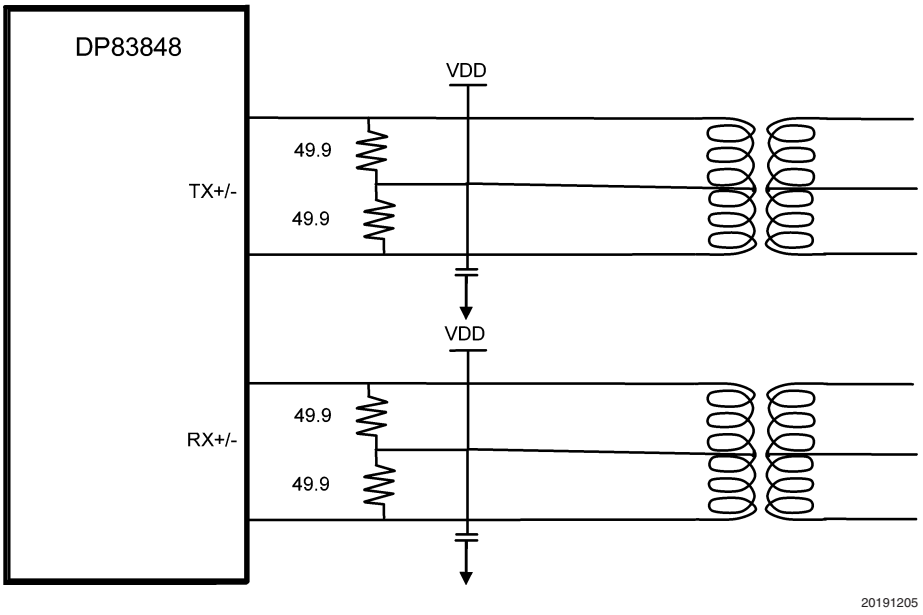

FIGURE 2. DP83848C/I/YB PMD Connections (Termination & Biasing)

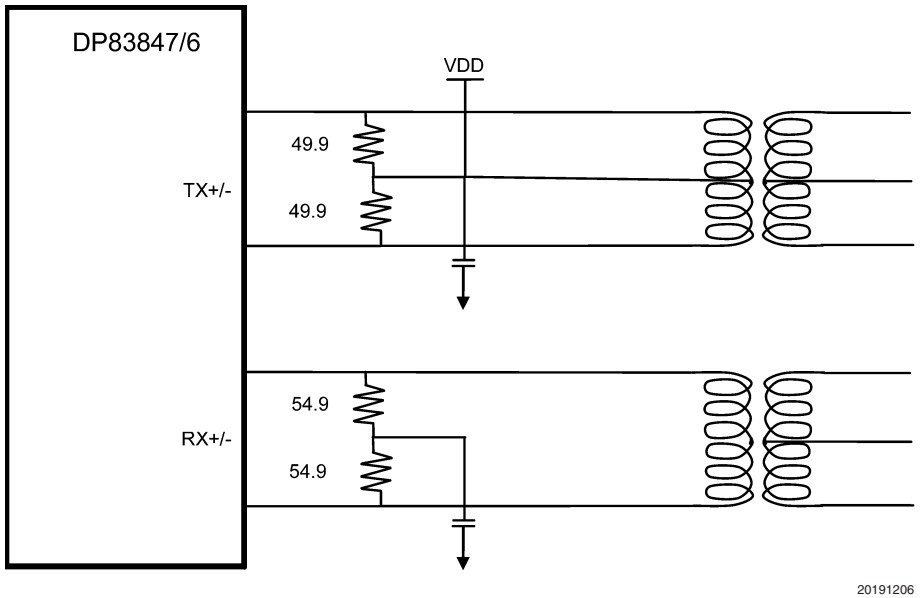

FIGURE 3. DP83847 PMD Connections (Termination & Biasing)

2.0 Potential Changes

The following section describes the specific changes that may be implemented in DP83848C/I/YB depending on the application.

2.1 TX_ER

Older designs using the DP83847 may use the TX_ER pin. This signal allows the system MAC to force DP83847 to deliberately corrupt the transmitted packet by inserting bad symbol codes. A similar function can be accomplished by having the MAC signal the PHY to stop transmission mid-packet. By stopping mid-packet, the receiving node will interpret the packet as having a bad CRC. Upper layers can then decide to receive or reject the packet in question. Since the function on the TX_ER pin can be more easily attained with the latter method, the TX_ER pin was not included on the DP83848. If the TX_ER pin is used as an input to any device, the pin should be pulled low to ensure that it does not float.

2.2 MII INTERFACE

The MII interface is used to connect the PHY to the MAC in 10/100 Mbps systems. For a 5V MII application, it is recommended to use 33 Ohm series resistor between the MAC and DP83848C/I/YB. The MII interface is a nibble-wide interface which consists of a transmit interface, receive interface and control signals. The transmit interface is comprised of the following signals:

- Transmit data bus, TXD[0:3] (pins 3,4,5 and 6 in DP83848C/I/YB)
- Transmit enable signal, TX_EN (pin 2 in DP83848C/I/YB)
- Transmit clock , TX_CLK (pin 1 in DP83848C/I/YB) which runs at 2.5MHz in 10Mbps mode and 25MHz in 100Mbps mode

The receive interface is comprised of the following signals:

- Receive data bus, RXD[0:3] (pin 43,44,45 and 46 in DP83848C/I/YB)
- Receive error signal, RX_ER (pin 41 in DP83848C/I/YB)
- Receive data valid, RX_DV (pin 39 in DP83848C/I/YB)
- Receive clock, RX_CLK (pin 38 in DP83848C/I/YB) for synchronous data transfer which runs at 2.5MHz in 10Mbps mode and 25MHz in 100Mbps mode

2.3 PHY ADDRESS

In a given system, multiple PHYs may be controlled by a single MII management interface. In order to support this, each PHY must have a unique address. DP83848C/I/YB facilitates this with PHY address strap options.

In DP83848C/I/YB, RXD0:3 and COL are used to set the PHY address. While DP83847 requires external 5K Ohm pull-ups or pull-downs to set the PHY address, pin COL has a weak internal pullup and RXD0:3 have weak internal pull-_downs in DP83848C/I/YB. Hence, the default setting for PHY address in DP83848C/I/YB is 01h. External 2.2K Ohm pull_ups and pull_downs can be added to change the PHY address from the default.

2.4 FLOW CONTROL

In DP83847, pin RX_ER may be strapped low to indicate Full Duplex Flow control support and left floating otherwise. Since flow control is a function of MAC layer, the MAC must set the bit in ANAR register in order to indicate Full Duplex Flow Control support in DP83848C/I/YB.

2.5 PHYSICAL LAYER ID REGISTER

The PHYsical Layer ID (PHYID) register allows system software to determine applicability of device specific software based on the vendor model number. The vendor model number is represented by bits 9 to 4 in PHYIDR2. The vendor model number in DP83848C/I/YB is 001001b. In DP83847, the vendor model number is 000011b.

TABLE 4. Register Change for Vendor Model Numbers

Register Address	Register Name	Register Description	Device	
Hex			**DP83848C/I/YB**	**DP83847**
03h	PHYIDR2	PHY ID 2	5C90h	5C30h

2.6 SOFTWARE RESET

A soft reset in the DP83848C/I/YB by setting bit 15 in the BMCR, will reset the device and set all the registers to their default or strapped settings. This includes Power Down, bit 11 in the BMCR, unless the PWR_DOWN/INT pin is externally strapped. For previous National devices, such as the DP83847 and DP83846, asserting software reset, by setting BMCR, bit 15, the Power Down register setting, BMCR, bit 11, does not get reset.

3.0 Informational Changes

This section describes the new features offered in DP83848C/I/YB and the changes required to implement them.

TABLE 5. New Features of DP83848C/I/YB

	DP83848C/I/YB	DP83847
System_Interfaces		
RMII	Yes	No
SNI	Yes	No
JTAG	Available in DP83848I and DP83848YB	No
Auto-MDIX	Yes	No
Energy Detect	Yes	No
LED Outputs	3	No
CLK-to-MAC Output	Yes	No
Power Down/Interrupt	Yes	No
Temperature Range		
0_to_70˚C	Yes	Yes
-40_to_85˚C	Available in DP83848I	No
-40_to_125˚C	Available in DP83848YB	No
Power Consumption		
Active Power (Typ)	264mW	351mW

3.1 AUTO-NEGOTIATION AND LED PINS

DP83847 has dedicated AN0, AN1 and AN_EN (pins 15, 16 and 17) for enabling and configuring Auto_Negotiation. In addition, LED pins 18 to 23 were used to indicate Speed, Receive, Transmit, Link, Collision and Duplex status. DP83848C/I/YB has only 3 pins multiplexed for auto-negotiation function and LED status indication. Pin 26 has multiple functions, indicating Activity and Collision status, combined with enabling Auto_Negotiation. Pin 28 indicates link status and controls the advertised and forced mode (AN0) of DP83848C/I/YB. Pin 27 indicates speed status and controls the advertised and forced mode (AN1) of DP83848C/I/YB. DP83848C/I/YB does not have separate pins to indicate transmit and receive activity status.

TABLE 6. DP83848C/I/YB Pin for Auto-Negotiation and LED

DP83848C/I/YB Pin Number	Auto-Negotiation function	LED function
26	Auto-Negotiation enable	Activity and collision status
27	Controls the advertised and forced mode (AN1)	Speed status
28	Controls the advertised and forced mode (AN0)	Link status

TABLE 7. DP83848C/I/YB Auto-Negotiation Modes

AN_EN	AN0	AN1	Forced mode
0	0	0	10 Base-T, Half-Duplex
0	0	1	10 Base-T, Full-Duplex
0	1	0	100 Base-TX, Half-Duplex
0	1	1	100 Base-TX, Full-Duplex
AN_EN	**AN0**	**AN1**	**Advertised mode**
1	0	0	10 Base-T, Half/Full-Duplex
1	0	1	100 Base-TX, Half/Full-Duplex
1	1	0	10 Base-T, Half/Full-Duplex 100 Base-TX, Half/Full-Duplex
1	1	1	10 Base-T, Half/Full-Duplex 100 Base-TX, Half/Full-Duplex

3.0 Informational Changes (Continued)

3.2 RMII interface

The RMII interface can be used to connect the MAC to PHY in 10/100 Mbps systems using a reduced number of pins. By utilizing this feature, significant PCB space savings can be realized within the system, especially one with a large number of Physical layer devices.

DP83848C/I/YB uses an external 50MHz clock (X1) as reference for both tranmsit and receive in the RMII mode. This is provided by an external oscillator. RX_DV should be pulled high using a 2.2K Ohm resistor to enable RMII mode.

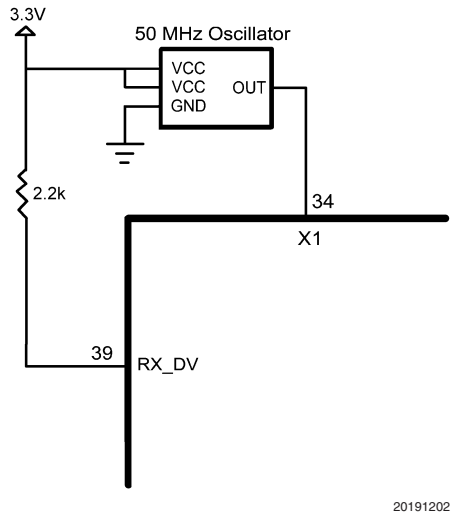

FIGURE 4. RMII Selection on DP83848C/I/YB

3.3 SNI mode

DP83848C/I/YB incorporates a 10Mb Serial Network Interface (SNI) which allows a simple data interface for 10Mb only system. While there is no defined standard for this interface, it is based on the earlier National Semiconductor's 10Mb physical layer devices. The following pins are used in SNI mode:

- TX_CLK
- TX_EN
- TXD_0
- RX_CLK
- RXD_0
- CRS
- COL

3.4 AUTO_MDIX SETTING

Auto_MDIX removes cabling complications and simplifies end customer applications by allowing either a straight or a cross-over cable to be used without changing the system configuration. Auto_MDIX is enabled by default in the DP83848C/I/YB. In order to disable Auto_MDIX, pin 41 (RX_ER) should be pulled to ground using a 2.2 K Ohm resistor. When enabled, this function utilizes Auto_Negotiation to determine the proper configuration for transmission and reception of data and subsequently selects the appropriate MDI pair for MDI/MDIX operation.

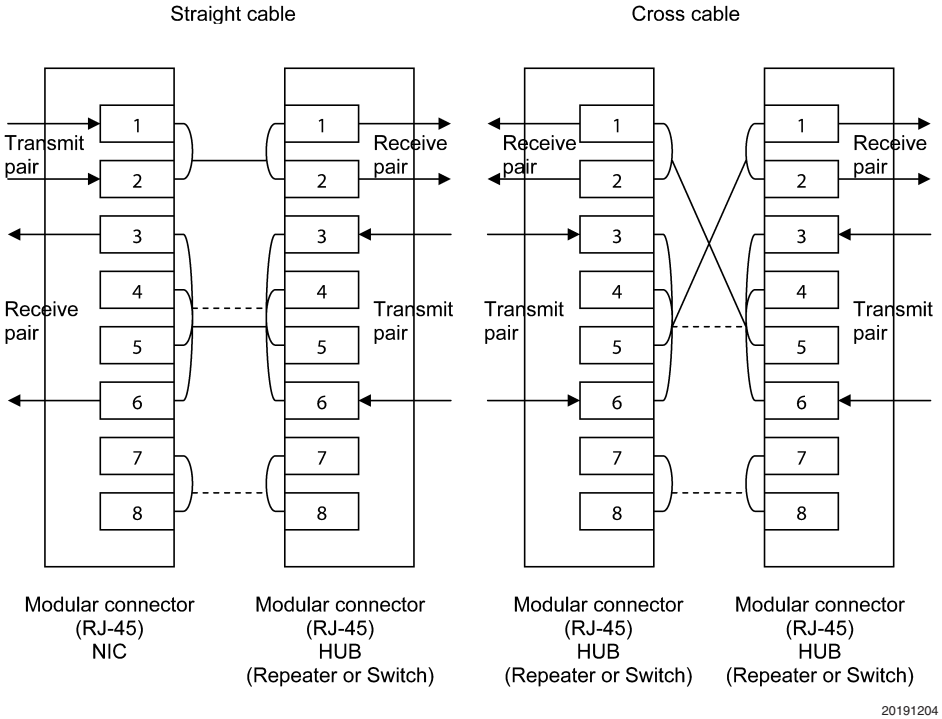

FIGURE 5. Auto_MDIX Operation

3.0 Informational Changes (Continued)

3.5 ENERGY DETECT

Energy Detect facilitates flexible and automatic power management based on detection of a signal on the cable. This enables an application to use an absolute minimum amount of power over time. Energy Detect functionality is controlled via the Energy Detect Control Register (EDCR), address 0x1Dh. When Energy detect is enabled and there is no activity on the cable, DP83848C/I/YB will remain in a low power mode while monitoring the receive pair in the transmission line. Activity on the line will cause the DP83848C/I/YB to return to the normal power mode.

3.6 CLK_to_MAC OUTPUT

DP83848C/I/YB offers a clock output of 25 MHz that can be routed directly to the MAC and act as the MAC reference clock, eliminating the need, and hence space and cost, of an additional MAC clock source.

3.7 Power Down/ Interrupt

DP83848C/I/YB offers a separate pin to indicate an interrupt based on various criteria defined by MISR and MICR registers. In DP83848C/I/YB, the PWR_DOWN/INT pin (pin 7) may be asserted low to put the device in a power down state. In the Interrupt mode, this pin is an open drain output and will be asserted low when an interrupt condition occurs. It is recommended to use an external pull_up resistor for proper operation of this function.

Appendix A

TABLE 8. Pinmap

DP83848C/I/YB Signal Name	DP83848C/I/YB Pin #	DP83847 Pin #	Description
MII Interface Pins			
MDC	31	25	MGMT DATA CLOCK
MDIO	30	24	MGMT DATA I/O
RXD0:3/PHYAD1:4	43,44,45,46	30,29,27,26	MII RX DATA
RX_CLK	38	32	MII RX CLOCK
RX_ER/MDIX_EN	41	33	MII RX ERROR
RX_DV/MII_MODE	39	31	MII RX DATA VALID
TXD0:3	3,4,5,6	38,39,40,41	MII TX DATA
TX_CLK	1	36	MII TX CLOCK
TX_EN	2	37	MII TX ENABLE
TX_ER	n/a	35	MII TX ERROR
COL/PHYAD0	42	43	MII COL DETECT
CRS/LED_CFG	40	45	MII CARRIER SENSE
PMD Interface Pins			
RD-/+	13,14	6,7	RX DATA
TD-/+	16,17	11,10	TX DATA
Clock Interface Pins			
X1	34	49	XTAL/OSC INPUT
X2	33	48	XTAL OUTPUT
LED Interface Pins			
LED_ACT/COL/AN_EN	26	22	COL LED STATUS
LED_ACT/COL/AN_EN	26	23	DUPLEX LED STATUS
LED_LINK/AN_0	28	21	LINK LED STATUS
LED_SPEED/AN_1	27	18	SPEED LED STATUS
LED_ACT/COL/AN_EN	26	n/a	ACT LED STATUS
LED_RX/PHYAD4	n/a	19	RX ACTIVITY LED
LED_TX/PHYAD3	n/a	20	TX ACTIVITY LED
Reset Function Pin			
RESET_N	29	46	RESET
Strap Pins			
PHYAD0:4	42,43,44,45,46	23,22,21,20,19	PHY ADDRESS
MDIX_EN/RX_ER	41	n/a	AUTO MDIX ENABLE
MII_MODE/RX_DV	39	n/a	MII MODE SELECT
SNI_MODE	6	n/a	MII MODE SELECT
LED_CFG/CRS	40	45	LED CONFIGURATION
PAUSE_EN/RX_ER	n/a	33	PAUSE ENABLE
Bias Function Pins			
RBIAS	24	3	BIAS RES CONNECTION
C1	n/a	42	REF BYPASS CAP
Test Mode Pins			
AN_0/LED_LINK	28	15	TEST MODE SELECT
AN_1/LED_SPEED	27	16	TEST MODE SELECT
AN_EN/LED_ACT/COL	26	17	TEST MODE SELECT
Special Function Pins			
25MHz_OUT	25	n/a	25 MHz CLOCK OUTPUT
PWR_DOWN/INT	7	n/a	POWER DOWN/INT
PFBIN1:2	18,37	n/a	POWER FEEDBACK IN

Appendix A (Continued)

TABLE 8. Pinmap (Continued)

DP83848C/I/YB Signal Name	DP83848C/I/YB Pin #	DP83847 Pin #	Description
PFBOUT	23	n/a	POWER FEEDBACK OUT
Supply Pins			
VDD	22,32,48	14,28,56, 57,59,63	3.3V
GND	15,19,35,36,47	58,60,62,64,65	GROUND
Reserved Pins			
RESERVED	8,9,10,11,12,20	1,2,4, 5,8,9, 12,13,34, 44,47,50, 51,52,53, 54,55, 61	RES

Appendix B

This section covers differences between the registers in DP83848C/I/YB and DP83847 applicable to software configuration of these devices.

REGISTER DIFFERENCES

All the IEEE specified registers of National Semiconductor Physical Layer devices comply with the respective IEEE standards. Only vendor specific registers have functions that may vary from device to device. If none of the vendor specific registers are modified for operation in the system application, the devices will have similar operation. In designs that do access or adjust any of these optional registers, the system may use the PHY_ID register, offset 03h, to detect which device is being used and make the appropriate changes in settings of device registers. Specific functions of these vendor defined registers, may be available in another register,or possibly in a different bit within the same register location. For additional information, or more specific definitions, please refer to the applicable datasheet(s).

DP83848C datasheet - http://www.national.com/pf/DP/DP83848C.html

DP83848I datasheet - http://www.national.com/pf/DP/DP83848I.html

DP83848YB datasheet - http://www.national.com/pf/DP/DP83848YB.html

DP83847 datasheet - http://www.national.com/pf/DP/DP83847.html

TABLE 9. Register Bit Definitions

Register Address	Register Name	Register Description	Device	
Hex			**DP83848C/I/YB**	**DP83847**
00h	BMCR	Basic Mode Control	Bit 15 – Reset (See Section *2.6 SOFTWARE RESET* for the difference in software reset)	Bit 15 – Reset (See Section *2.6 SOFTWARE RESET* for the difference in software reset)
03h	PHYIDR2	PHY ID 2	5C90h	5C30h
04h	ANAR	Auto-Neg Adv	Bit 11 - ASM_DIR	Bit 11 - Res
05h	ANLPAR	Auto-Neg Link Partner Ability	Bit 11 - ASM_DIR	Bit 10 and 11 - Res
			Bit 10 - Pause	
10h	PHYSTS	PHY Status	Bit 14 MDI-X mode	Bit 14 Res
			Bit 7 MII Interrupt	Bit 7 - Res
11h	MICR	MII Interrupt Control	Register to control test Interrupt, Interrupt Enable and Interrupt Output Enable	Res
12h	MISR	MII Interrupt Status	Register for Interrupt enable and status	Res
16h	PCSR	PCS Sub-Layer cfg and sts	Bit 12 Res	Bit 12 BYP_4B5B
			Bit 11 Res	But 11 FREE_CLK
			Bit 7 DESC_TIME	Bit 7 Res
			Bit 1 Res	Bit 1 SCRAM_BYPASS
			Bit 0 Res	Bit 0 DESCRAM_BYPASS
17h	RBR	RMII and Bypass	Configure or bypass RMii mode	Res
18h	LEDCR	LED Direct Control	Control LED outputs	Res
19h	PHYCR	PHY Control	Register changes (See datasheet)	Register changes (See datasheet)
1Ah	10BTSCR	10 Base-T Status/Control	Bit 15 10BT serial	Bit 15:9 - Res
			Bits 14 to 12 Res	
			Bits 11:9 - SQUELCH	
1Bh	CDCTRL1	CD Test Control	Register changes (See datasheet)	Register changes (See datasheet)
1Dh	EDCR	Energy Detect Control	Enable and control Energy Detect	Res

Notes

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