

Designing a Multi-Phase Asynchronous Buck Regulator Using the LM2639

Overview

The LM2639 provides a unique solution to high current, low voltage DC/DC power supplies such as those for fast microprocessors. The two major features of the LM2639-based solutions are multiphase and ultra-high switching frequency, which result in the following three advantages when compared to a conventional buck and a high frequency single-phase buck.

The first advantage is thermal. Since the load current is evenly shared among multiple channels, the heat generated is greatly reduced for each channel due to the fact that power loss is proportional to square of current. Surface mount MOSFETs and diodes (such as DPAK and D2PAK packages) can be used to handle a fairly high load current such as 20A or even higher. Physical size of the output inductor shrink significantly because of a similar reason.

The second advantage is reduced input and output ripple current. Since the channels are phase shifted, the AC components of the currents tend to cancel. This eases the burden of ripple RMS current requirement on input capacitors. Output voltage ripple is also reduced.

The third advantage, and probably the most prominent for microprocessors is, the solution enables the use of ceramic capacitors for output filtering. This is because in such an application, the output inductance is usually the gating factor in slowing the supply current during a fast load transient. Duty cycle usually saturates. However, a LM2639-based solution not only can use low output inductance values (because of high switching frequency), but the inductors are like paralleled during a load transient event (because of multi-phase operation). That makes the solution not only faster than a conventional buck, but also faster than a single-phase high switching-frequency buck. Because of that, small surface mount multi-layer ceramic capacitors can be used as output capacitors. This advantage is especially attractive to low voltage, high current processors such as K7 and Pentium III, because countless number of bulky low-ESR aluminium capacitors can be completely replaced by small, surface-mount ceramic capacitors.

The LM2639 helps accurate load current sharing by guaranteeing a 1% duty cycle match among the channels. Two, three or four phase operation can be configured. It can also be configured to use internal clock or to use an external clock signal.

The LM2639 also features a precision 5-bit DAC whose output voltages comply with Intel's VRM specifications.

Current limit is realized through a current sense resistor at the input end.

Soft Start

The LM2639 has an initial digital soft start function. Upon VCC5V pin exceeding power-on-reset level (about 4.2V), duty cycle will grow from 0 to maximum value gradually, in a

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manner of 16 steps (see Figure 1). It takes about 12,800 clock cycles to go through all 16 steps. For a typical clock frequency of 8MHz it takes 1.6ms to finish all 16 steps, 100 μ s each step.

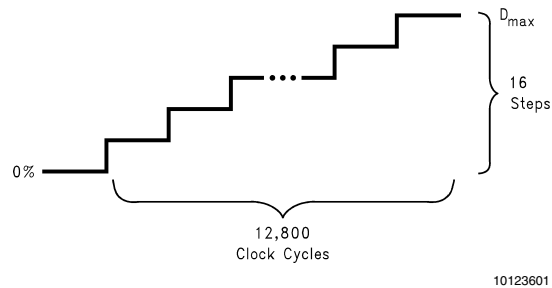


FIGURE 1. Digital Soft Start

Clock Signal

The clock signal can be generated internally or it can be synchronized to an external source. The internal clock can be set to run at 40kHz to 10MHz by adjusting the value of the resistor connecting from R_{ref} pin to the ground. To use the internal clock, connect the Clksel and Extclk pins to V_{CC} 5V pin. To use external clock, connect Clksel pin to ground and the Extclk pin to the clock source. To generate an 8MHz internal clock, use a 8.06k Ω resistor at the R_{ref} pin. To lower the internal clock frequency, increase the resistor value.

Three-Phase Operation

The regulator can be configured to operate in 3-phase mode instead of 4-phase mode. The phase associated with DRV3 will be disabled, and the rest three phases will be 120° apart. To enable 3-phase mode, pull the Divsel to logic high. The 3-phase mode can be used for relatively low current applications to save cost.

Two-phase operation is the same as 4-phase operation - just use any two channels that are 180° out of phase.

Loop Compensation

The purpose of loop compensation is to tailor the dynamic characteristics of the regulator so that it meets both the steady-state and transient response requirements. The error amplifier inside the LM2639 is of transconductance type. The typical compensation network is a lag compensation and is formed by a capacitor and a resistor in series (C_c and R_c in Figure 2). The function of the lag compensation network is two folds. One is to enhance the DC gain so that the regulator will have a highly precise output voltage in the steady

Loop Compensation (Continued)

state over all line and load ranges. The other is to boost the total gain of the loop transfer function so that the regulator will have a higher control bandwidth and gain.

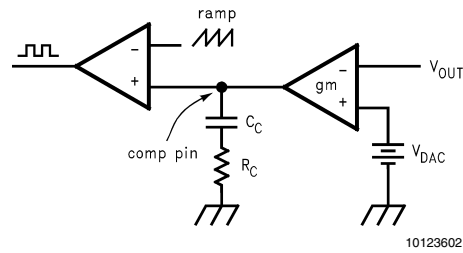


FIGURE 2. Loop Compensation

As an example, let us go through the loop compensation process of the typical application circuit. The loop can be broken into two parts. That is, control-to-output transfer function (also known as power stage transfer function), and output-to-control transfer function. The small signal model for the control-to-output portion of the circuitry is illustrated in Figure 3.

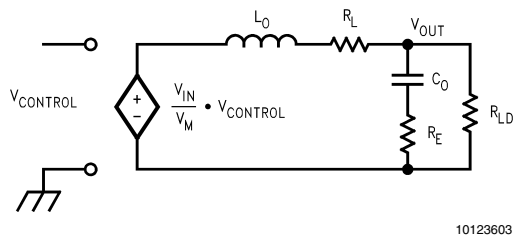


FIGURE 3. Small Signal Model of Power Stage

In the model, L_o is the equivalent output conductor, which is output inductance of each channel by number of channels. R_L is the MOSFET $R_{ds(on)}$ divided by number of channels is output capacitance and R_o is the total combined ESR. R_{LD} is load resistance. $V_{control}$ is the voltage at COMP pin. V_m is the peak-to-peak value of the PWM ramp appearing at the PWM comparator, which is 2V in the case of LM2639.

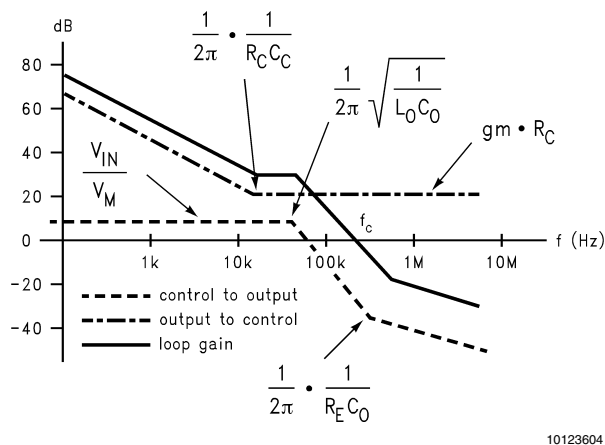


FIGURE 4. Bode Plots of Transfer Functions

It is easy to see that the DC gain of the control-to-output transfer function is:

$$G_{dc} = \frac{V_{IN}}{V_M}$$

In our case, it is $5V \div 2V = 2.5$ or 8dB. A double pole occurs at:

$$f_{dp} = \frac{1}{2\pi} \sqrt{\frac{1}{L_O C_O}}$$

In our case, $L_o = 300nH \div 4 = 75nH$, and $C_o = 22\mu F \times 12 = 264\mu F$. So the double pole is at 35kHz.

The next significant parameter in the power stage transfer function is the ESR zero:

$$f_{ESR} = \frac{1}{2\pi} \times \frac{1}{R_E \cdot C_O}$$

In our case, $R_E = 15m\Omega \div 12 = 1.3m\Omega$. So ESR zero is at 464kHz.

Refer to Figure 4 for asymptotic bode plot of the power stage (broken line).

The lag compensation has one pole-zero pair. The pole occurs at zero frequency. The location of the zero is determined by:

$$f_{zero} = \frac{1}{2\pi} \times \frac{1}{R_C \cdot C_C}$$

In our case, it is important to place the zero before the power stage double pole to avoid stability issue. The trade-off between a higher zero frequency and a lower one is the mid-frequency gain and the phase margin. In our specific case, the higher the zero frequency the less the phase margin but the higher the mid-frequency gain. This, in time domain, will translate into a faster load transient recovery speed. If we choose 17kHz, and a compensation gain of 20dB beyond the zero frequency, the output-to-control and the final loop transfer functions will be like those shown in Figure 4.

The cut off frequency (f_c in Figure 4) is where the loop transfer function has a 0dB gain and is usually referred to as control bandwidth. In this case, we have a control bandwidth of 200kHz. In a LM2639-based solution, the control bandwidth is pretty important in load transient response.

Loop Compensation (Continued)

To calculate the compensation values, use the following equations:

$$R_C = \frac{G_{\text{comp}}}{g_m}$$

and

$$C_C = \frac{1}{2\pi \cdot f_{\text{zero}}} \times \frac{g_m}{G_{\text{comp}}}$$

where G_{comp} is the compensation gain beyond the compensation zero frequency. In our case, G_{comp} is 20dB or 10, g_m is 1.3m mho, so $R_C = 7.7\text{k}\Omega$, and $C_C = 1.2\text{nF}$.

Since the loop transfer function bode plot crosses the 0dB line at a slope of -40dB/decade, phase margin can be pretty low. A phase margin of 30° to 40° is typical. The phase margin is determined by how far the cutoff frequency is from the double pole, how far it is from the ESR zero and the damping of the system. A low phase margin tends to give an under-damped transient response. Fine-tuning on the bench is necessary to determine what compensation values make the best trade-off.

The user might be tempted to further increase the compensation gain G_{comp} by increasing R_C value so as to have a higher cutoff frequency and a better phase margin (because the cutoff frequency is getting closer to the ESR zero). He should be cautioned that there are parasitic parameters that start to take effect when it gets close to 1MHz. So he may lose phase margin instead by doing so. The best way to find out is still to fine-tune R_C on the bench.

The ESR of the same type of capacitor may differ from different vendors. Sometimes this may make one set of compensation values good for one brand of capacitor and bad for another. The solution is either stick with the working brand of capacitor or change the compensation values that work for both. However, the latter usually results in a compromise of the performance of load transient response.

Current Limit

The LM2639 can be configured to provide input current limit (see Figure 5). The way the circuit works is as follows. OC- pin draws a fixed amount of current from external resistor R_{LIM} . So the voltage of OC- pin can be preset to be any value below V_{IN} by adjusting the value of R_{LIM} . When I_{IN} is high enough, OC+ pin voltage will be lower than OC- pin, which will trigger the internal current limit comparator. A PCB trace can be used to act as the current sense resistor. To set the current limit, use an R_{LIM} value as calculated by the following equation:

$$R_{\text{LIM}} = \frac{I_{\text{LIM}} \cdot R_{\text{sense}} + V_{\text{offset}}}{I_{\text{OC-}}}$$

where I_{LIM} is the desired current limit value, R_{sense} is the resistance of the sense resistor value, V_{offset} is the input offset voltage of the current limit comparator (see data sheet), and $I_{\text{OC-}}$ is the current drawn by OC- pin. The capacitor is used to get rid of possible high frequency noise. A value of 0.1μF is usually good enough.

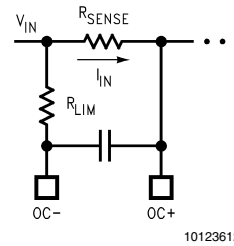


FIGURE 5. Current Limit Setup

Output Inductor Selection

There are several considerations when selecting the output inductors. The inductance should not be too high so as to hinder the load transient response. The inductance should not be too low to avoid high output voltage ripple and high hysteresis loss. To find out about the load transient response aspect, simulate the circuit operation using the average model of the regulator and see if the duty cycle saturates during a worst case load transient. If the duty cycle saturates, it means the inductor is probably too large. The most practical method to find out about the power loss is to measure it on the bench. As a first cut, use the 20% ripple current criterion to determine the inductance value.

Falco has some inductor designs that are very suitable for high frequency multi-phase operation. Popular models include the T02502 and T025A2. The former is 400nH, 10A nominal. The latter is 300nH, 10A nominal. Falco can be reached at (305) 662-9076 Ext. 206. Coiltronics also has some low inductance drum core inductors that are suitable for this type of applications.

Output Capacitor Selection

Output capacitor selection is closely related to loop stability, ripple voltage and load transient response. As has been discussed in the loop compensation section above, the ESR zero created by the output capacitors is important to phase margin and thus loop stability. Different vendors may have different ESR values for the same amount of capacitance. For multi-layer ceramic capacitors, ESR is usually determined by the number of layers.

Due to high frequency operation, the output ripple voltage is usually dominated by ESL rather than ESR or capacitance. So if ESR zero frequency is the same, to reduce the total ESL it is desirable to have more capacitors in parallel than fewer, even if they have the same total capacitance and ESR. It is probably a good idea to use some smaller capacitors in parallel with the larger ones to reduce the combined ESL.

Adding more capacitors will definitely help load transient response but the effect is not very significant unless the duty cycle tends to saturate during a large and fast load transient. The most effective way to reduce load transient excursions of output voltage is to increase the control bandwidth and make sure the output impedance is low enough so that duty cycle will not saturate.

Since multi-layer ceramic capacitors have very low ESR values, they seem to be more suitable for fast load transient applications. It would take too many low ESR tantalum or aluminum capacitors to achieve the same amount of com-

Output Capacitor Selection

(Continued)

bined ESR. The landscape changes with the speed of the regulator as compared to the load slew rate. In low switching frequency regulators, the speed of the regulator is slow anyway, the load transient response solely depends on the combined ESR of the output bulk capacitors. The high speed LM2639-based regulator enables the use of low value capacitors, and the load transient response is a combination of voltage across the ESR and the delta voltage caused by the capacitor discharge. The ESR becomes less and less important as the speed difference of the load and the regulator diminishes.

Murata and Taiyo Yuden offer some high capacitance multi-layer ceramic capacitors that are very suitable for LM2639-based solutions. As an example, both offer 22 μ F, 10V, Y5V ceramic capacitors in a 1210 package. Murata's part number is GRM235Y5V226Z and Taiyo Yuden's part number is LMK325F226ZN. They also have higher capacitance parts.

Input Capacitor and Inductor

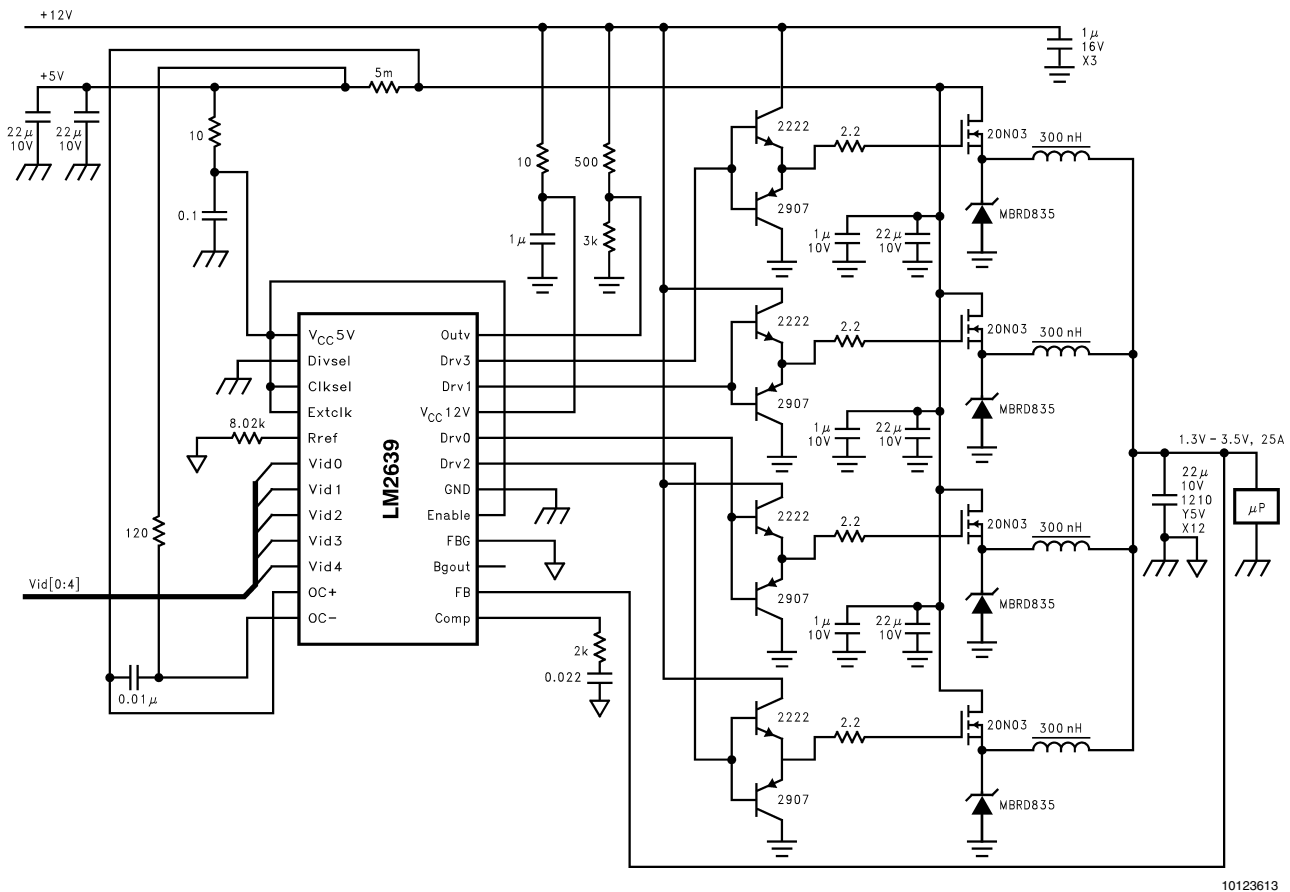
An input filter is necessary if the input rail is also shared by other loads. The input capacitors will experience significant current when large load transient occurs. To limit the input rail di/dt, an input inductor is necessary. Refer to Intel VRM documents for input rail di/dt specification and LM2636 data sheet for input filter design.

PCB Layout Guidelines

1. Put grounding via the output capacitors as close to the ground as possible to reduce the ESL.

2. Use two or more via each ground pad when grounding the output capacitors.
3. Try to arrange the output capacitors as symmetrical as possible as appeared to the output inductors so that the output voltage ripple will be minimized.
4. Consider using some of the board areas to provide a heat sink to the MOSFETs and diodes.
5. DO not place the LM2639 too close to the MOSFETs, diodes and inductors so that the IC will not be over-heated.
6. Keep the compensation components close to the LM2639 to minimize noise.
7. Use large pads for the external bipolar drivers to reduce temperature rise on them.
8. When designing the input rail current sense resistor using the PCB trace, use an inner layer to have good tolerance.
9. Keep the output inductors and capacitors close to the load to reduce distribution loss.
10. The DRV:4 traces do not have to be very short. They can be 10mil and can go a long way (such as a few inches) from the pins to the discrete drivers.
11. The traces from the discrete driver outputs to the MOSFETs can be 20mil to 30mil wide, and as long as 1 or 2 inches.
12. Connect the feedback ground pin (FBG) to the copper that is local to the load ground to have a good load regulation.

Typical Application



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