PCB Layout for National Semiconductor's SIMPLE SWITCHER® Power Modules

National Semiconductor's Simple Switcher® Power Modules offer an alternative to complex power designs and the PCB layout issues typically related to DC – DC converters. Nonetheless, there is still some engineering to be done when designing with and laying out these power modules. This Application Note will discuss the best PCB layout methods, practices and techniques to maximize the module's performance.

When planning a power converter layout, the first thing to consider is the physical loop area of the two switched current



National Semiconductor Application Note 2078 Don Rhodes and Marc Davis-Marsh September 16, 2010



loops. Even though these are primarily hidden from view in a power module it's important that we understand the current paths in each of the two loops since they do extend beyond the module. In Loop 1, shown in *Figure 1*, current flow originates at the energized input bypass capacitor, Cin1 and then continues through the internal high side MOSFET during its on-time, followed by the internal inductor and the output bypass capacitor CO1, finally returning to the input bypass capacitor.



High Current Loops on Demo Board

FIGURE 1.

Loop 2 is formed during the off-time of the internal high side MOSFET and the on-time of the low side MOSFET. The energy stored in the internal inductor flows through the output bypass capacitor and the low side MOSFET returning to GND as shown. The area where these two loops don't overlap, and including the boundary between the loops, is a high di/dt current area. The input bypass capacitor Cin1 plays a critical role in supplying high frequency currents to the converter and returning them to their source. The output bypass capacitor Co1 does not supply large ac current but does act as a high frequency filter for switching noise. For these reasons the input and output capacitors should be placed as close as possible to their respective VIN and VOUT pins on the module. As shown in Figure 1, make the traces between the bypass capacitors and their respective VIN and VOUT pins as short and wide as possible; thereby minimizing the inductance of these connections.

There are two primary benefits in minimizing the inductance of the layout. The first benefit is improving part performance, by enhancing the transfer of energy to and from Cin1 and CO1 respectively. This will make sure the module has good high frequency bypassing to minimize inductive voltage spikes from the high di/dt currents. This minimizes noise and voltage stress to the device, ensuring proper operation. The second benefit is minimized EMI. A capacitor connected with less parasitic inductance will exhibit low impedance to much higher frequencies, and consequently reduce conducted emissions. Ceramic (X7R or X5R) or other low ESR type capacitors are recommended. Adding more input capacitance is only effective if additional caps are placed close to GND and VIN. The Simple Switcher® Power Modules have inherently lower radiated and conducted EMI as a result of their design. However, maximum performance will be achieved by following the layout guidelines discussed in this application note.

The routing of return currents are often overlooked and yet play an essential role in the optimization of any power design. Again, ground traces from Cin1 and CO1 should be kept as short and wide as possible, with a direct connection of the exposed pad (EP). This is especially important for the ground connection of the input cap Cin1 which carries large ac currents.

The ground connected pins of the module (including the EP), input and output capacitors, soft start cap and feedback resistor should all be connected to a return plane on your PCB. This return plane serves as a very low inductance current return path and a heat spreader as discussed in the following section.

The feedback resistors should also be placed as close as possible to the FB (feedback) pin of the module. Keeping the trace between the FB pin and the center tap of the feedback

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resistors as short as possible is important in minimizing potential noise pick-up on this high impedance node. The compensation components or feed forward capacitor, as applicable, should be placed as close as possible to the upper feedback resistor. See the PCB Layout Diagrams in the respective module datasheets for examples.

See AN-2024 for a layout example of the LMZ14203.

Thermal Design Recommendations

The electrical benefit derived from the compact layout of a module finds its tradeoff in thermal design. The same amount of power needs to be dissipated from a smaller space. With this in mind the Simple Switcher® power modules were de-



signed with a single large exposed pad on the back of the package that is electrically connected to ground. This pad provides very low thermal impedance from the internal mosfets, (where most of the heat is generated) to the printed circuit board. θ JC, the thermal impedance from the junction of the semiconductor to the case for these devices is 1.9 °C / W. An industry leading θ JC is great, but if the thermal impedance from the case to the ambient air, θ CA, is too large, then a low θ JC means nothing! The heat becomes trapped at the exposed pad when no low resistance thermal path is offered to the ambient air. And what determines θ CA? The thermal resistance from the exposed pad to the ambient air is completely controlled by the design of the printed circuit board and any associated heat sinks.





FIGURE 2. Circuit Designed using SMS4.2.1

Let's quickly look at how to do a simple thermal design with a printed circuit board and no heat-sink. Figure 3 illustrates the module and the printed circuit board as thermal resistances. Due to the relatively high thermal impedance between the junction and the case top, compared to the thermal impedance from the junction to the exposed die attach pad, the θ JT thermal path can ignored for our first pass estimate of the thermal resistance from the junction to the ambient air, θ JA.

The first step in a thermal design is to determine how much power we need to dissipate. The power dissipated by a module, PD, can be easily calculated from the efficiency graphs, η , published in the datasheet.

$$P_{D} = V_{OUT} \times I_{OUT} \times (\frac{1}{\eta} - 1)$$

We then use our design's temperature constraints, the maximum TAmbient and the rated junction temperature TJunction, (125°C) to determine the required thermal resistance of the module mounted on a printed circuit board.

$$\theta_{JA} = \frac{T_{JUNCTION} - T_{AMBIENT}}{Power Dissipation}$$

Finally, we can use a greatly simplified approximation for the convective heat transfer from the surface of a printed circuit board (which has unbroken one-ounce copper heat-sinking on both the top and bottom layers and infinite thermal vias) to determine the board area required for heat sinking.

Board Area (cm²)
$$\ge \frac{500 \frac{\circ C \times cm^2}{W}}{\theta_{JA} - \theta_{JC}}$$

Board Area (in²) $\ge \frac{77.5 \frac{\circ C \times in^2}{W}}{\theta_{JA} - \theta_{JC}}$

This approximation of required PCB board area does not include the effect of thermal vias, which are used to transfer heat from the top layer metal, where the package connects to the PCB, to the bottom layer metal. The bottom layer is used as a second surface where convection can transfer heat away from the board. For the board area approximation to be effective, use at least 8-10 thermal vias. The thermal resistance for vias is approximated in the equation below.

$$\theta_{\text{VIAS}} \approx \frac{261 \frac{\text{°C}}{\text{W}}}{\text{\# of Thermal Vias}}$$

This approximation is for a typical 12 mil diameter through hole via with a 0.5 ounce copper sidewall. Use as many vias as will fit underneath the exposed pad using 1 to 1.5 mm spacing to form an array.

See application notes; AN-2020 and AN-2026 for further information.

National Semiconductor's Simple Switcher® Power Modules offer an alternative to complex power designs and the PCB layout issues typically related to DC – DC converters. While

the layout headaches have been eliminated, there is still some engineering to be done to maximize the performance of the modules through good bypassing and thermal design.

Notes

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