Use of the LMV112 to Reduce Reference Clock Interaction in Handheld Device

National Semiconductor
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Barry Yuen
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Introduction

The cellular phone and wireless Personal Digital Assistant are continuing to integrate new features and applications. Wireless technologies across IS-95, CDMA2000, W-CDMA, UMTS, GSM, PHS, Wi-Fi, WiMax, Bluetooth and GPS are needed in the same handheld portable device. The LMV112 clock buffer amplifier can resolve clock interference issue among different chipsets.

The 3rd generation cellular product is not only a wireless communication device, but it also provides multimedia performance for the users. These multimedia features are driven by demand for mobile entertainment, gaming and gambling, and on-the-go productivity in the business world. Current and emerging 3G mobile units have high-resolution color displays, integrated video cameras, streaming audio and video content, MP3 players, worldwide web access at broadband speeds, and location-based services such as E911, and multi-user 3-dimensional gaming. All these added features require different communication, computation and control application-specific integration circuits to perform the needed functions.

Whatever the function of each specific integration circuit, they all need some kind of reference clock signal. In an RF chip with a phase-locked loop, the reference clock is multiplied up to radio frequency. In a digital signal process or a microcontroller, the clock signal is used to time each computational cycle. Any other sequential circuit needs a clock signal as a reference. Although there may still be some combinational logic circuits used in electronics, it is very safe to claim that the use of a reference clock signal is ubiquitous as far as portable or wireless equipment is concerned.

Figure 1 illustrates the need of systems clock in contemporary portable electronics. The electronic hardware can be functionally partitioned into three categories. These include the systems clock circuitry, pure digital electronics usually implemented in submicron CMOS technology, and Analog/RF electronics usually in BiCMOS mixed signal process.

For the system clock circuitry, either a stand-alone module or a built-in circuit can be used in the CMOS or BiCMOS chips with an external crystal as a resonator. Either approach has advantages and disadvantages. The main issue to resolve involves the interaction of the clock signal with different chipsets in the portable electronics. As a system reference clock, the clock signal needs to be clean and accurate. This refers to frequency stability, phase noise and distortion of the clock signal. As shown in *Figure 1*, the loading effects between different chips and the clock circuit degenerates the original fidelity of the clock signal. A clock buffer amplifier, such as the LMV112, will reduce the interaction and keep the original performance of the crystal oscillator circuit.

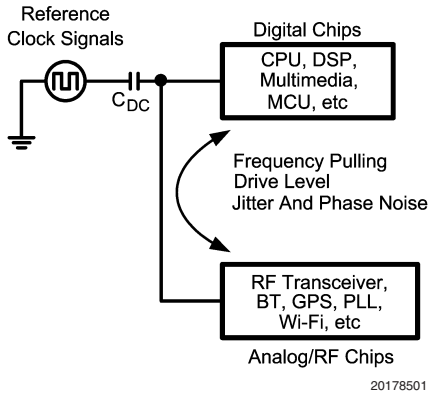

FIGURE 1. System Function Partitions in Wireless/Portable Electronics

Reference Clock Implementation

In general, there are two ways to generate a reference clock in a portable electronic device. One is to use an external crystal oscillator module as shown in *Figure 2*. The other way is to add capacitors and a parallel mode crystal to the reference circuits in the main chipset as shown in *Figure 3*.

Figure 2 shows a typical Colpitts Crystal oscillator circuit used with an off-the-shelf crystal oscillator module. The quartz crystal is used and specified for parallel mode operation. A parallel mode crystal is preferred in the high frequency band, which is 3 MHz to 30 MHz, because the induction in this frequency range is large and has a low Q factor. Together with the loading capacitors Ca and Cb and transistor Q1, this circuit will generate a sine wave at the desired resonance frequency. Transistor Q2 is used to make a buffer amplifier. Varactor diode and temperature compensation circuits can be added to make this circuit become a

Reference Clock Implementation

(Continued)

Voltage Control Temperature Compensated Crystal Oscillator (VCTCXO) as required for GSM/GPRS and CDMA handsets.

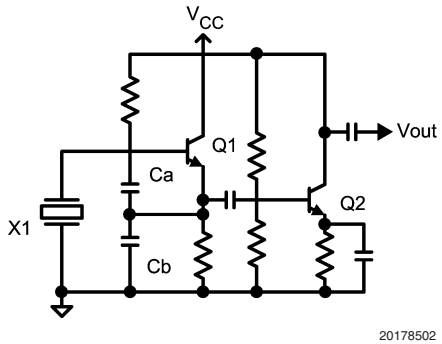

FIGURE 2. Typical Colpitts Crystal Oscillator Circuit in an Off-the-Shelf Oscillator Module

Figure 3 shows another example of a clock reference circuit. This circuit makes use of the inverter gate in a digital CMOS chip. External load capacitors Ca and Cb are needed to generate the right resonance frequency. Usually, the crystal manufacturers will specify their values. The advantage of this approach is that it is inexpensive and it requires low power consumption. The CMOS is relatively limited in its output drive capability. *Figure 4* displays a typical CMOS inverter logic gate. The output current is

EQ_1:

$$I_{OUT} = i_{Dmax} = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS} - V_{TH})^2$$

where

μ is mobility of charge carrier (electrons or positive charge)

C_{OX} is the gate oxide capacitance per unit area

V_{GS}–V_{TH} is the overdrive voltage

W/L is the aspect ratio, W is the width and L is the length of the source-drain path.

Equation EQ_1 expresses the dependence that the driving current i_{Dmax} has on the constants of technology μ and C_{OX}, the device dimensions W and L, and the gate and drain potentials with respect to the source V_{GS}–V_{TH}. Once the process technology and supply voltage is chosen for the CMOS design, the CMOS IC designer can only increase the i_{Dmax} by increasing the width of the CMOS device. This larger width will not be very cost effective because the chip will be bigger.

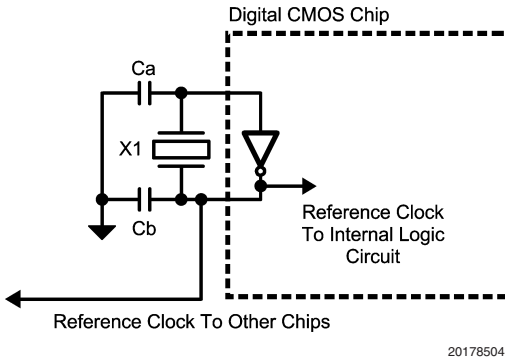

FIGURE 3. Reference Clock Circuit Inside a Digital CMOS Chip

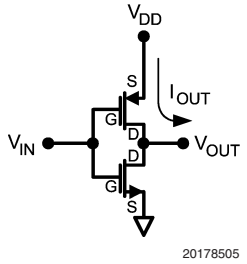

FIGURE 4. CMOS Inverter

Unwanted Interaction in the Clock Circuit

Both digital and analog/RF circuits are needed to achieve the features and functions required by customers in the wireless world. Particularly for RF electronics, a reference clock signal with good phase noise and jitter performance is required to achieve the needed radio performance. Since the same clock signal is distributed to other chips as a reference, the interaction between different chips at the clock circuits degrades the quality of the reference clock signal. There are a few things that systems engineers must be aware of in the clock distribution circuitry.

Since the crystal resonance frequency and its external capacitance determine the clock frequency, loading effect presented to the crystal will pull the clock frequency to a different value. This phenomenon is known as a pulling effect or frequency pulling. Unfortunately, most of the crystal oscillator modules on the market do not provide specifications of this performance.

Unwanted Interaction in the Clock Circuit (Continued)

The external load of a crystal oscillator can cause the drift of frequency in two different ways. The first is related to the loading capacitors. The second is related to the needed sourcing current or drive level.

Load Capacitance

Differences in the load capacitance of the oscillation circuit may result in a variation from the desired frequency. The needed load capacitance C_{LOAD} for the crystal is found with the following equation:

EQ_2:

$$C_{LOAD} = \frac{Ca \times Cb}{Ca + Cb} + Cs$$

Typically, the stray capacitance Cs is about 5 pF.

An approximation of the pulling limit due to the external load capacitors is found using the following equation:

EQ_3:

$$\frac{\Delta f}{f} = 0.5 \frac{C1}{C0 + C_{Total\ LOAD}}$$

Here the C0 is the capacitance formed by the crystal electrodes plus any holder or package capacitance and C1 is the fundamental motional capacitance. $C_{Total\ LOAD}$ is the needed load capacitance C_{LOAD} plus any loading capacitances from different chipsets. As this equation shows, a decrease in total load capacitance causes an increase in frequency, and an increase in total load capacitance causes a decrease in frequency.

Drive Level

The drive level for the crystal denotes the electric power required to oscillate a quartz crystal. This can be calculated with the following formula:

EQ_4:

$$\text{Drive Level } P = I^2 \bullet Re$$

Here 'I' is the amount of current to pass through the quartz crystal. Re is the effective resistance of the quartz crystal. The following equation will provide Re:

EQ_5:

$$Re = R1 \times \left(1 + \frac{C0}{C_{Total\ LOAD}}\right)^2$$

Here R1 is the fundamental motional resistance. If the drive level exceeds the specified level from the crystal manufacturers then the oscillation frequency will shift. This occurs because an excessive level of power causes stress for the quartz crystal and consequently its temperature rises. If an excessive power drive level is applied to the quartz crystal oscillator, this will deteriorate or damage the characteristics. In other words, the fundamental motional resistance and capacitance will be shifted and then the resonance frequency is shifted. On the other hand, if the current I is too small, oscillation will not occur. Since the mechanical properties of crystal are fixed, the current passing through the crystal is a function of the voltage across it. In order to keep the drive level under specification, peak-to-peak voltage across the crystal has to be within the window specified by the crystal manufacturers and this limits the driving capability of the clock circuitry.

Use of the LMV112 to Resolve the Problem

In order to achieve the right resonance frequency, it is obvious that the circuit design should eliminate the frequency pulling effect by setting the correct loading capacitance and drive level for the crystal.

This means that a sufficiently high input impedance must be presented to the output of a crystal oscillator circuit so that the total load is not considered a significant "loading" to the oscillator. On the other hand, a sufficiently low output impedance is needed from the crystal oscillator to drive successive chipsets so that this crystal oscillator is not representing a "loading" to the successive chipsets. *Figure 5* is used to illustrate this concept and the LMV112 from National Semiconductor can provide this function.

Use of the LMV112 to Resolve the Problem (Continued)

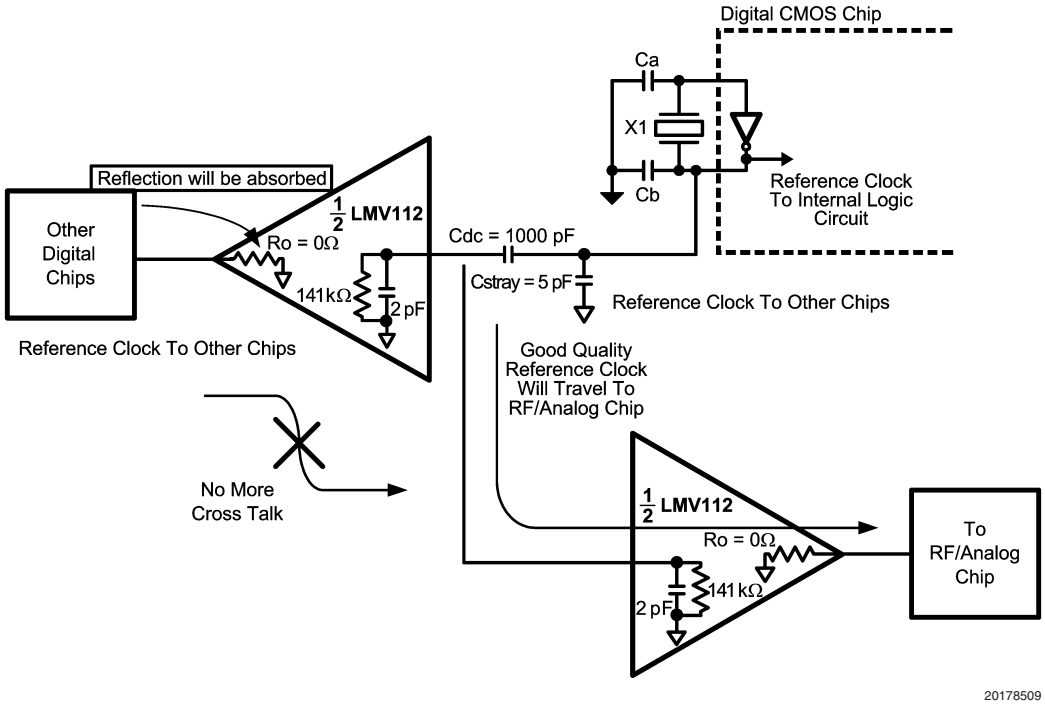

FIGURE 5. Implementing the LMV112 to Reduce Clock Circuit Interaction

Implementing the LMV112 in Design

The input impedance of the LMV112 is 141 kΩ in parallel with 2 pF at low frequency. If a reference clock similar to the one shown in *Figure 3* is used and the crystal manufacturer has specified that the needed load capacitance for its parallel mode crystal is 30 pF, then the following is the method for finding the values of Ca and Cb.

Since the stray capacitance is in parallel with the Cin of the LMV112 and the DC blocking capacitor Cdc = 1000 pF is a short circuit in 10 MHz, then Cin is considered to be in parallel with stray capacitance and ignores the effect of the DC blocking capacitor, Cdc.

Then, from equation EQ_2:

EQ_6:

$$C_{Total\ LOAD} = C_{LOAD} + Cin = \frac{Ca \times Cb}{Ca + Cb} + Cs + Cin$$

$$= \frac{Ca \times Cb}{Ca + Cb} + 5\ pF + 2\ pF$$

$$= \frac{Ca \times Cb}{Ca + Cb} + 7pF$$

If Ca = Cb = C is chosen:

EQ_7: $C_{Total\ LOAD} = 0.5C + 7\ pF = 30\ pF$

$C = (30 - 7) / 0.5\ pF$

$C = 46\ pF$

As a matter of fact, systems engineers can request that the crystal manufacturers make crystal at the needed clock frequency with specified load capacitors. In the above example, 46 pF is not a standard ceramic chip capacitor. It is better to choose standard capacitor values throughout the design.

Here is another example of how to design can design a crystal oscillator circuit with the LMV112 as a buffer amplifier. Assume that the designer would like to choose 22 pF as Ca and Cb, The data sheet of the LMV112 shows that the input capacitance is 2 pF and it is in parallel with the stray capacitance of 5 pF.

The designer can use EQ_2 to find that $C_{total\ LOAD}$ = 22 pF * 22 pF / (22 pF + 22 pF) + 5 pF + 2 pF = 18 pF. In this case, the system designer should request that the crystal manufacturer make a parallel mode crystal at the desired resonant frequency with CLOAD = 18 pF.

Conclusion

In summary, the LMV112 is a unity gain buffer amplifier and is suitable for wireless and portable applications. It can be used in a clock system circuit and will provide enough isolation, driving capability and frequency range for buffering a crystal-based oscillator. A design example for using the LMV112 together with on-the-chip crystal oscillator has been detailed. Any system designers can use this method to develop their robust clock systems.

Notes

National Semiconductor
Americas Customer
Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560