SCAN90CP02 Design for Test Features

National Semiconductor
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The SCAN90CP02 has several Design-for-Test (DfT) features intended to lower development and manufacturing test costs:

- IEEE 1149.1
- IEEE 1149.6
- StuckAt fault insertion

These features also enable fast debug and isolation of faults in fielded equipment, improving the equipment availability and uptime.

IEEE 1149.1

The IEEE 1149.1 standard for Boundary Scan Test is a basic building block of DfT. Also known as JTAG, this standardized approach provides built-in testability access on digital ICs and printed circuit boards. Adding JTAG to an IC requires 4 or 5 additional test pins, a Test Access Port (TAP) of ±1000 gates, and additional logic to allow the test circuitry to access each pin of the device. When included in VLSI devices, such as microprocessors or complex ASICs, the JTAG feature can be used to initiate and record the results of Built-In Self-Test, or BIST. The primary purpose of JTAG, however, is the ability to perform boundary scan or interconnect tests.

Interconnect testing at the board level is done by sending signals from one JTAG IC to another to verify that the correct ICs are in place, that they are oriented properly, that the solder bonds are good and free of defects (i.e., shorts), and that PC board traces are sound. These board-level tests represent the most common mechanical defects that are detected during manufacturing test. For Digital boards with a high percentage of Boundary Scan ICs, JTAG testing alone is sufficient to ensure a high level of quality.

Systems that use JTAG have superior diagnostics for reduced overall time to market. JTAG devices allow increased access to test nodes – particularly those JTAG functions that are housed in fine-pitch packages and BGA packages – that results in better fault coverage and improved quality. Implementation of JTAG also allows the use of automated test generation and inexpensive PC-based testers, reducing the need for expensive in-circuit testers (ICTs). In markets where high availability is critical, (e.g., systems which are virtually always in use, such as Telecom and Datacom), extensive use of JTAG has become routine. In fact, IEEE 1149.1 is now so integral to digital board and system test that many ICs are available only with JTAG.

Recently, FLASH and FPGA/CPLD Configuration has extended the utility of the JTAG bus and it's support infrastructure. All of the leading FPGA and CPLD suppliers offer in-system programming (ISP) using JTAG. In addition, several vendors offer software and hardware tools that use the JTAG bus to program FLASH memory. In situations where the JTAG bus has been included for test purposes, the added benefit of configuring programmable components comes at almost no cost.

Another feature that is being promoted by the programmable logic community is the potential to reconfigure components over the life of the system using the JTAG bus. This again takes advantage of an existing JTAG infrastructure.

National also provides a number of infrastructure support devices for partitioning the JTAG bus in a system for better programming access or fault isolation, including the 'STA111 and 'STA112 multidrop JTAG multiplexers. These devices allow the serial IEEE-1149.1 bus to be used in a multidrop configuration. Both devices feature multiple local scan ports to improve isolation of JTAG-accessible components.

For more details on the IEEE 1149.1 standard, refer to Application Note AN-891, Non-contact Test Access for Surface Mount Technologies, IEEE 1149.1-1990, or the IEEE standards web site.

IEEE 1149.6

The IEEE 1149.6 Standard extends the capabilities of IEEE 1149.1, while maintaining compatibility with existing test standards and their infrastructures. The goal of the Standard is to increase testability of interconnects between high-speed differential AC-coupled devices. AC coupling of differential signals is becoming increasingly common as transmission frequencies exceed 1 Gbps. The AC-coupling technique eliminates problems with DC offsets and differing bias voltages.

The AC-coupled nets on printed circuit boards are difficult, if not impossible, to test with conventional DC-based methods, creating a need for a solution that would extend Boundary Scan into the AC domain. In addition, the 1149.6 implementation must not interfere with the transmission path, or in other words, with the mission mode of the high-speed device in which it is implemented. By meeting its requirements, the implementation of this Standard also offers interoperability between technologies and vendors.

The basic implementation of IEEE 1149.6 requires the addition of a pulse generator in the signal path driver and a pulse detector in the signal path receiver. The pulse train is initiated via IEEE 1149.6 instructions delivered through the IEEE 1149.1 interface, and the pulse train is propagated thru the transmission media to the receiver. The receiver observes it's inputs for the presence of the pulse train.

In an AC-coupled interconnect, the only part of the pulse train that will pass thru the coupling capacitors are the edge transitions, so the receiver will see a string of narrow pulses at each transition, and must be able to detect these transitions and provide a pass/fail indication at the receiver's IEEE 1149.1 port.

The SCAN90CP02 is the worlds first commercially available product supporting the IEEE 1149.6 standard.

For more details on the IEEE 1149.6 standard, refer to the IEEE standards web site.

Fault Insertion

In critical computing applications, fault detection and recovery are often designed-into the system to enable temporary recovery from fault conditions autonomously. Conventional office client computing systems have very little capability to recover from faults – the user typically reboots the computer to clear the fault. This is acceptable in most situations as long as the computer controls non-critical processes.

In other applications where it is critical that computer control be maintained during a fault event, fault tolerance must be designed into the system and evaluated to ensure fault events do not become catastrophic to life or property. A truly fault tolerant system might use redundancy to maintain control of the process. The system is constructed with redundant components and if a fault is encountered control is switched to the backup system. High availability systems are similar to fault tolerant systems, but their application may tolerate one or more failure modes without catastrophic results. For example, a typical email system in larger corporations has a fail-over capability to a redundant server to ensure communication is not interrupted.

One method of testing fault tolerance of a system is to provide a way to inject faults into the system in a controlled manner and to observe the system for an appropriate response. Fault insertion, which is a partially intrusive operating mode, is very useful to validate fault-tolerant systems, where it is important to be able to verify that correct operation continues to take place even when some fault conditions exist or interconnects are defective.

The typical fault condition encountered occurs when bits are stuck high or stuck low. These faults are collectively referred to as “stuck-at” faults, and it is often desirable that a system has the capability to inject stuck-at faults as part of the fault insertion and fault recovery strategy for a fault tolerant application.

In support of fault tolerant system designs, the SCAN90CP02 features the ability to insert typical interconnect faults via the IEEE 1149.1 (JTAG) port. The StuckAt feature enables the user to override logic values on any of the external pins during normal operation.

StuckAt can be thought of as having the same capabilities as the IEEE-1149.1 EXTEST instruction but on a per pin basis. Because this feature occurs on a per-pin basis, normal device operation (mission mode) is possible with the exception of the desired faults. This feature is used to emulate stuck-at faults in a system so that fault detection, isolation, and mitigation can be evaluated.

For an input, this feature will emulate a short to VDD or VSS as well as a faulty upstream driver. For the outputs, shorts to VDD or VSS and faulty drivers can be emulated. Outputs that are tri-stated via an input pin can also emulate an open to the downstream receiver. This is accomplished by forcing the tri-state controlling input to the appropriate value. Note: Outputs are not able to force a 1 or 0 if the associated tri-state control pins are asserted.

To activate the StuckAt feature, instructions and data are shifted into the device via the IEEE-1149.1 interface. There are three instructions that are associated with this feature, SA, SA_PRELOAD, and SA_BYPASS. SA and SA_PRELOAD access the StuckAt data register, whereas the SA_BYPASS accesses the BYPASS register. The StuckAt feature is only active when either the SA or SA_BYPASS instruction is active. Each input and each output has two associated bits in the StuckAt data register, one for the data that is to be driven and one for control. Information is shifted into the StuckAt data register when the active instruction is SA or SA_PRLOAD and the TAP state machine is in the SHIFT-DR state. The update (U) register is clocked as the TAP enters the UPDATE-DR state. (Refer to *Figure 1* and *Figure 2*). The order of the bits in the StuckAt data register is shown in *Table 2*.

Note that fault vaues can be forced on any pin in any combination. Between each output condition change, $\overline{\text{TRST}}$ must be asserted and de-asserted

TABLE 1. Fault Insertion Instructions

Instruction	Register Accessed	Notes
SA_PRELOAD	StuckAt	Works like the PRELOAD instruction in 1149.1 but with access to the StuckAt data register. The StuckAt feature is not active when SA_PRELOAD is the active instruction
SA	StuckAt	StuckAt is activated with the instruction
SA_BYPASS	BYPASS	StuckAt is activated with the instruction

TABLE 2. StuckAt Data Register Order

Cell Number	Function	Pin
0 (TDO)	Control	OUT1±
1	Data	OUT1±
2	Control	OUT0±
3	Data	OUT0±
4	Control	PEM11
5	Data	PEM11
6	Control	PEM10
7	Data	PEM10
8	Control	PEM01
9	Data	PEM01
10	Control	PEM00
11	Data	PEM00
12	Control	$\overline{\text{EN1}}$
13	Data	$\overline{\text{EN1}}$
14	Control	$\overline{\text{EN0}}$
15	Data	$\overline{\text{EN0}}$
16	Control	SEL0
17	Data	SEL0
18	Control	SEL1
19 (TDI)	Data	SEL1

Fault Insertion (Continued)

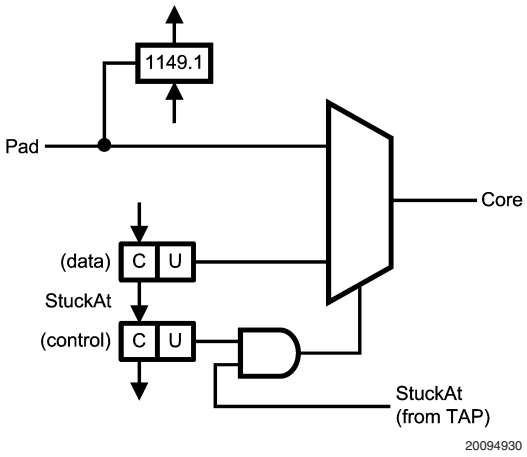

FIGURE 1. StuckAt Input Cell

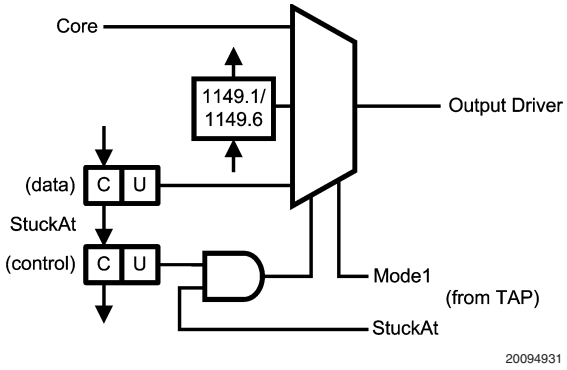

FIGURE 2. StuckAt Output Cell

National Semiconductor
Americas Customer
Support Center
Email: new.feedback@nsc.com
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www.national.com

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