# 551600234 - LMP8100 Evaluation Board User Guide

This demo board contains a footprint for the LMP8100, along with input, output, power and control circuitry. The evaluation board is unstuffed allowing the user to install the circuit that is needed.

## Connectors, Jumpers, Test Points

### POWER SUPPLY

There are three holes for banana plugs labeled GND, V+, and V− to power the evaluation board. Power can also be applied on pins 7, 8, and 9 on header J5. A single supply of +5V or a dual supply of ±2.5V can be used. If a single supply is used, the V− pin can be grounded by shorting JP2.

### SIGNAL CONNECTORS

J1    is a BNC labeled IN for the input signal.

J2    is a BNC labeled OUT for the output signal.

J5    pins 1 and 3 can also be used for the output and input signals.

J4    is a 5-pin header that can be connected to an SPI bus to write the register of the LMP8100.

J3    is a hole for a banana plug to provide a low impedance voltage to the GRT pin. This voltage can also be input on J5 pin 5. If GRT is to be grounded, short JP1.

## Schematics

### TEST POINTS

The evaluation board has the following test points.

TP1 – IN pin
TP2 – GRT pin
TP3 – SDI pin
TP4 – SDO pin
TP5 – SCK pin
TP6 – $\overline{CS}$ pin
TP7 – OUT pin
TP8 – GND
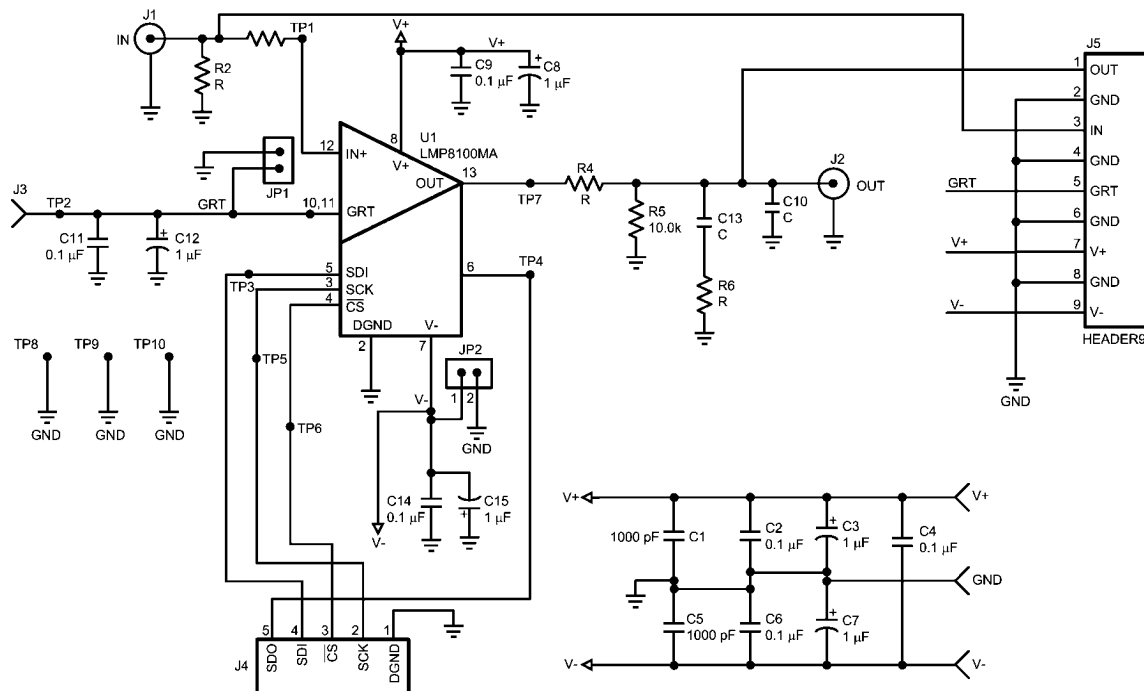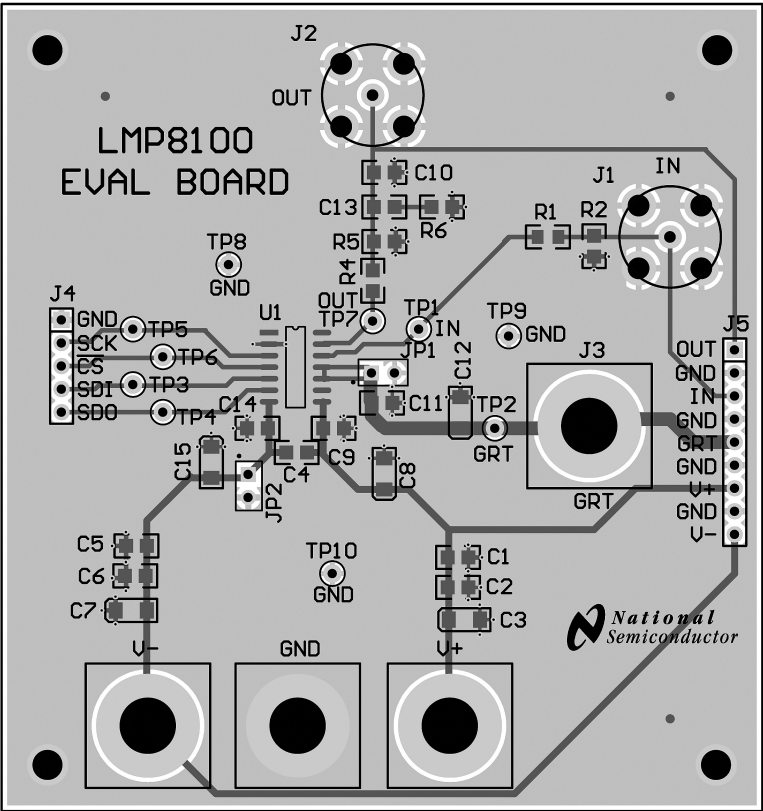TP9 – GND
TP10 – GND



**FIGURE 1. Schematic**

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# Board Layout



30075702

**FIGURE 2. View of Top and Bottom of Evaluation Board**

# Notes

# Notes

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