LMH0356 Customization with SMBus

National Semiconductor
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Introduction

The LMH0356 3G HD/SD SDI Reclocker provides excellent jitter performance for 2.97 Gbps digital video streams that comply with the SMPTE 424M standard. The reclocker's 4:1 input multiplexer, excellent jitter performance, and low power make it ideal for applications such as routers, video switchers, and distribution amplifiers.

The LMH0356 provides pin-accessible features such as: 4:1 input multiplexer with 0-30" FR4 equalization, two differential serial data outputs (one programmable as a data-rate clock output), auto or manual rate select, auto or manual data bypass, SD/HD rate indicator, output mute, lock detect indicator, and device enable.

Additional features of the LMH0356 can be accessed through special SMBus register access. Care must be taken when controlling the device using the registers as normal pin-control functionality of the device is disabled in this mode.

This document includes an overview of SMBus, followed by details on how to enable SMBus access on the LMH0356. Information on using the LMH0356 SMBus to accomplish the following three useful tasks is included at the end of the document:

- Read back the detected data rate (2.97 Gbps, 1.485 Gbps, or 270 Mbps)
- Modify the CDR loop bandwidth
- Disable the second CML output driver to minimize power

SMBus Overview

The System Management Bus (SMBus) is a two-wire serial interface through which various system component chips can communicate with each other and with the rest of the system.

The SMBus is controlled through two lines: a clock line (SCL) and a data line (SDA). SCL is the clock output from the master (i.e. FPGA host) to the slave devices on the bus. SDA is the bidirectional data signal between the host and the slave devices on the bus. SCL and SDA are both open drain and require external pullup resistors. (On the LMH0356, the BYPASS/AUTO BYPASS pin is used for SDA, and the OUTPUT MUTE pin is used for SCL.)

Most microcontrollers support SMBus. Please refer to the SMBus Specification version 2.0 for implementation details.

TRANSFER OF DATA VIA THE SMBus

During normal operation the data on SDA must be stable during the time when SCL is high. Data can only change state when SCL is low. Two unique states define the message START and STOP conditions:

START: A high-to-low transition on SDA while SCL is high indicates a message START condition.

STOP: A low-to-high transition on SDA while SCL is high indicates a message STOP condition.

The host generates START and STOP patterns at the beginning and end of each transaction.

SMBus TRANSACTIONS

Each byte (8 bits) is transferred MSB first, followed by an acknowledge bit. The acknowledge bit is "0" for acknowledge (ACK), or "1" for not acknowledge (NACK). The host generates nine clock pulses for each byte transfer, and the ninth clock pulse constitutes the acknowledge cycle. The transmitter releases the SDA line during the acknowledge clock cycle to allow the receiver to send the ACK (or NACK). See *Figure 1*.

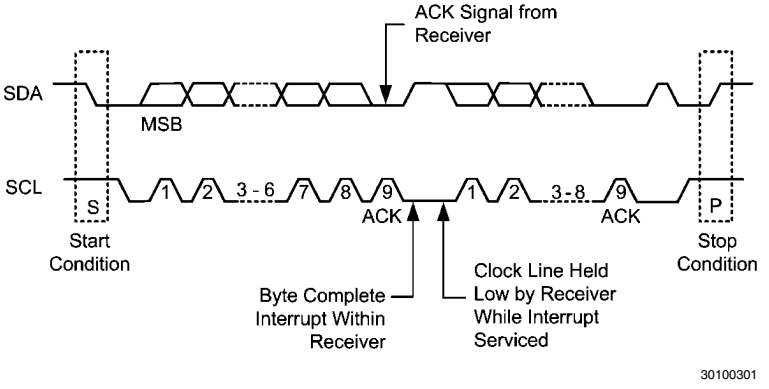


FIGURE 1. SMBus Transaction Format

WRITING A REGISTER

To write a register, the following protocol is used (refer to *Figure 2*, and also see the SMBus 2.0 specification).

1. The host drives a START condition, the 7-bit SMBus address, and a "0" indicating a WRITE.
2. The device (slave) drives the ACK bit ("0").
3. The host drives the 8-bit Register Address.
4. The device drives an ACK bit ("0").
5. The host drives the 8-bit data byte.
6. The device drives an ACK bit ("0").
7. The host drives a STOP condition.

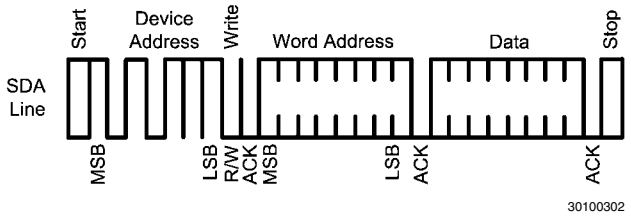


FIGURE 2. SMBus Register Write

READING A REGISTER

To read a register, the following protocol is used (refer to *Figure 3*, and also see the SMBus 2.0 specification).

1. The host drives a START condition, the 7-bit SMBus address, and a “0” indicating a WRITE.
2. The device (slave) drives the ACK bit (“0”).
3. The host drives the 8-bit Register Address.
4. The device drives an ACK bit (“0”).
5. The host drives a START condition.
6. The host drives the 7-bit SMBus Address, and a “1” indicating a READ.
7. The device drives an ACK bit (“0”).
8. The device drives the 8-bit data value (register contents).
9. The host drives a NACK bit (“1”) indicating end of the READ transfer.
10. The host drives a STOP condition.

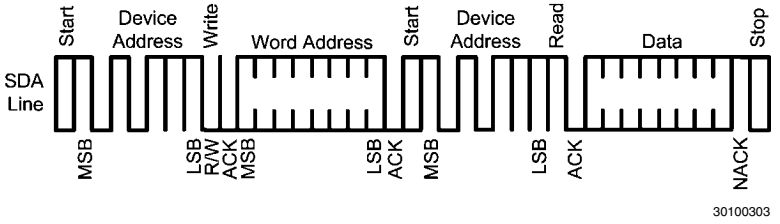


FIGURE 3. SMBus Register Read

Enabling SMBus Access for the LMH0356

The LMH0356 SMBus registers were intended for production test control and device monitoring. These registers are not documented in the LMH0356 datasheet and their performance has not been characterized. However, some of these registers are useful in certain applications.

Please note the following important points about using the LMH0356 SMBus mode:

- A dedicated SMBus is required per reclocker.
- The LMH0356 SMBus pins must be driven from a 3.3V source (they are not 5V compliant).
- When the SMBus mode is enabled, the hardware power-on-reset function in the LMH0356 is disabled. When using the LMH0356 SMBus features, the registers and state machine must be initialized by first powering up in Auto Rate mode and then switching to SMBus mode.
- The 7-bit address for the LMH0356 is **57h**. The LSB is set to 0b for a WRITE and 1b for a READ, so the 8-bit default address for a WRITE is AEh and the 8-bit default address for a READ is AFh.

The following steps explain how to enable SMBus access for the LMH0356:

- Connect RATE0 pin to VCC (nominally 3.3V), while maintaining the ability to drive this pin high or low to properly reset the device.
- Connect RATE1 pin to VCC (nominally 3.3V), while maintaining the ability to drive this pin high or low to properly reset the device.
- Connect SCO_EN pin to ground. (Note that enabling the serial clock output while using SMBus access requires a register bit to be set.)
- Access SDA (SMBus serial data input/output) through the BYPASS/$\overline{\text{AUTO BYPASS}}$ pin of the LMH0356. This pin requires an external 10 kΩ pullup resistor to VCC. Voltage levels are LVCMOS.
- Access SCL (SMBus serial clock input) through the OUTPUT $\overline{\text{MUTE}}$ pin of the LMH0356. This pin requires an external 10 kΩ pullup resistor to VCC. Voltage levels are LVCMOS
- Power up the LMH0356 in Auto Rate mode (RATE0=0, RATE1=0) and then change it into SMBus mode (RATE0=1, RATE1=1) after power up. The LMH0356 should be held in Auto Rate mode for approximately 300 ms prior to entering SMBus mode. This procedure ensures a proper reset of the SMBus registers and reclocker state machine.

Figure 4 shows the SMBus implementation for the 48-pin LLP version of the LMH0356. *Table 1* and *Figure 5* show the recommended SMBus Timing.

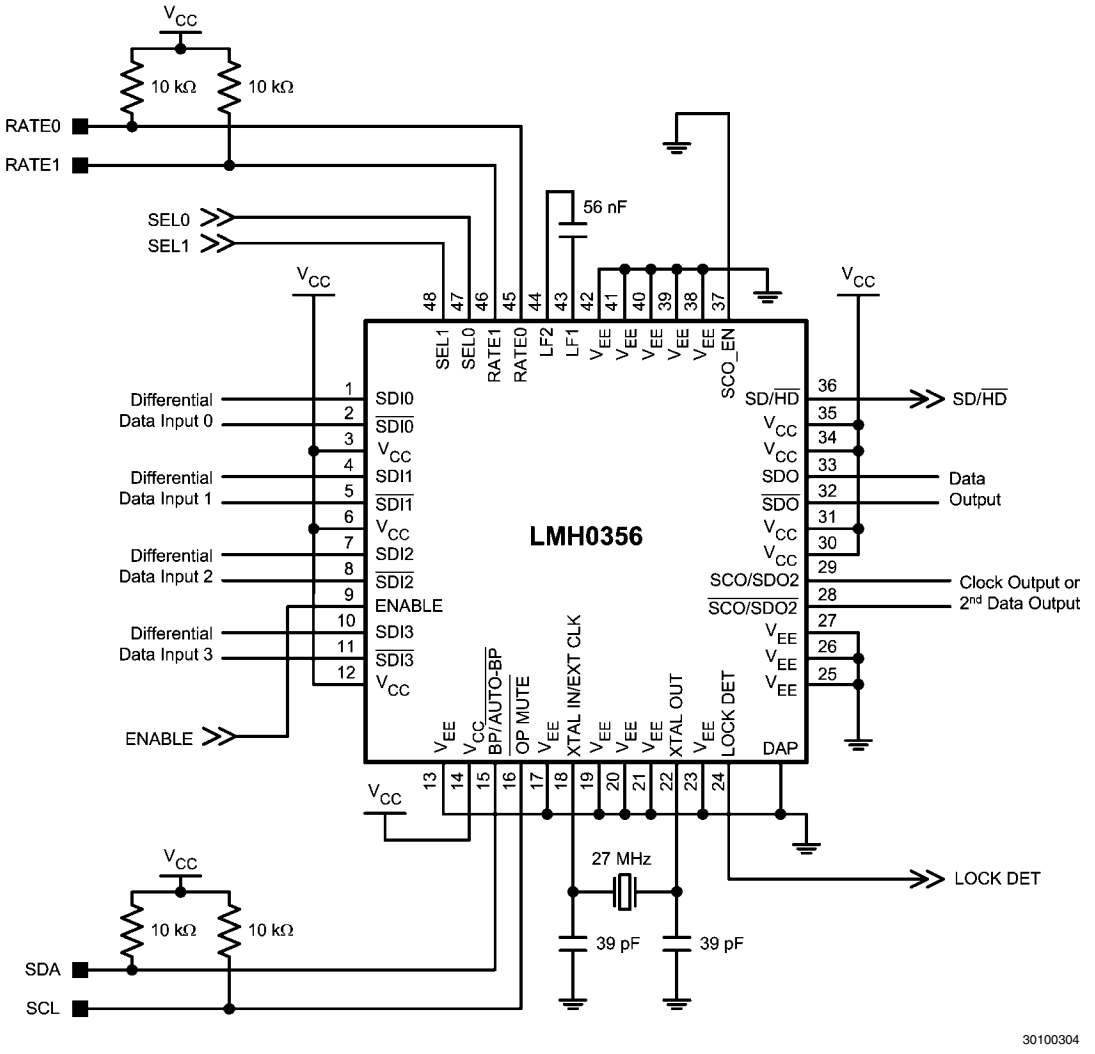
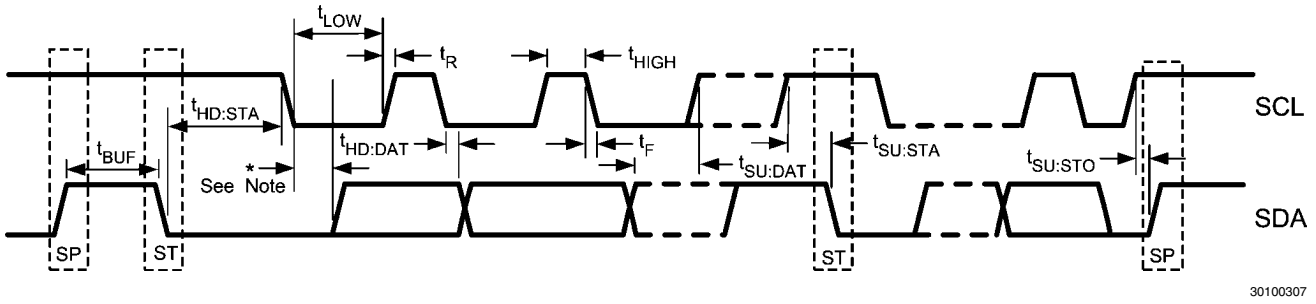


FIGURE 4. LMH0356 SMBus Implementation

TABLE 1. Recommended SMBus Timing

Symbol	Parameter	Min	Typ	Max	Units
f_{SMB}	Bus Operating Frequency	10		100	kHz
t_{BUF}	Bus free time between Stop and Start Condition	4.7			µs
$t_{HD:STA}$	Hold time after (repeated) Start Condition. After this period, the first clock is generated.	4.0			µs
$t_{SU:STA}$	Repeated Start Condition setup time	4.7			µs
$t_{SU:STO}$	Stop Condition setup time	4.0			µs
$t_{HD:DAT}$	Data hold time	300			ns
$t_{SU:DAT}$	Data setup time	250			ns
t_{LOW}	Clock low period	4.7			µs
t_{HIGH}	Clock high period	4.0		50	µs
t_F	Clock/Data Fall Time			300	ns
t_R	Clock/Data Rise Time			1000	ns
t_{POR}	Time in which device must be operational after power on			500	ms



* Note: SDA and SCL should be held low for 2 µs after a Start condition to properly de-assert the Start indicator.

FIGURE 5. SMBus Timing Parameters

Description of a Subset of LMH0356 Registers

NOTE: When writing to the LMH0356 registers, RSVD bits must be written with the indicated default values. Only the non-reserved register bits should be modified.

REGISTER 00h – BASIC CONTROL

Register 00h is used to invoke the pin control modes that aren't accessible when the SMBus is enabled, as shown in *Table 2*.

TABLE 2. Register 00h – Basic Control

Address	R/W	Bits	Name	Default	Description
00h	R/W	7:6	RATE	00	Rate select (bit 6 = RATE0, bit 7 = RATE1). 00: Auto rate select (default) 01: 270 Mbps. 10: 1.483, 1.485, 2.967, 2.97 Gbps. 11: 2.967, 2.97 Gbps.
		5:3	RSVD	000	Reserved. These bits must always be 000.
		2	BYPASS	0	Bypass/$\overline{\text{Auto Bypass}}$. 0: Normal operation. Reclocking automatically bypassed when reclocker is unlocked or data rate is not supported. 1: Reclocking is bypassed.
		1	OPMUTE	0	Output Mute. 0: Normal operation (outputs not muted). 1: Outputs are muted.
		0	SCO_EN	0	SCO Enable. 0: SCO/SDO2 output is data. 1: SCO/SDO2 output is clock.

Bits [7:6] can be controlled to force the rate detection mode.

When SMBus mode is used, the SCO_EN and OUTPUT $\overline{\text{MUTE}}$ pins are not available. In order to observe the serial clock, bit 0 must be set high. Similarly, in order to mute the outputs, bit 1 must be set high.

REGISTER 0Eh – MODIFYING THE CDR LOOP BANDWIDTH VIA THE CHARGE PUMP CURRENT

The default settings of the LMH0356 registers have been set to minimize output jitter while meeting SMPTE 424M specifications for jitter tolerance. It may be useful in some applications to increase the loop bandwidth of the CDR to extend input jitter tolerance to higher frequencies. Register 0Eh can be used to increase the LMH0356's CDR charge pump current, as shown in *Table 3*. Increasing the charge pump current will, in turn, increase the loop bandwidth.

TABLE 3. Register 0Eh – Modifying the CDR Loop Bandwidth

Address	R/W	Bits	Name	Default	Description
0Eh	R/W	7:4	RSVD	0001	Reserved. These bits must always be 0001.
		3:2	CHARGE PUMP	00	Charge Pump current. 00: Current = 25 µA, CDR BW @ 2.97 Gbps = 2.7 MHz. 01: Current = 50 µA, CDR BW @ 2.97 Gbps = 5.3 MHz. 10: Current = 75 µA, CDR BW @ 2.97 Gbps = 7.8 MHz. 11: Current = 100 µA, CDR BW @ 2.97 Gbps = 9.5 MHz.
		1:0	RSVD	11	Reserved. These bits must always be 11.

Figure 6 and *Figure 7* show 2.97 Gbps Jitter Transfer and Jitter Tolerance, respectively, for the LMH0346 with different charge pump current settings. This data applies to the LMH0356 as well since both devices have the same reclocker core.

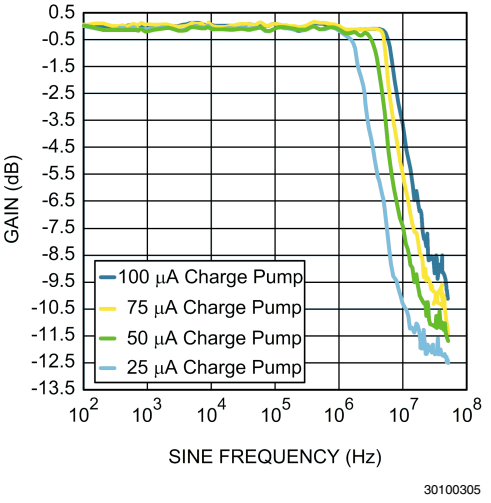


FIGURE 6. LMH0346 2.97 Gbps Jitter Transfer with Different Charge Pump Current Settings

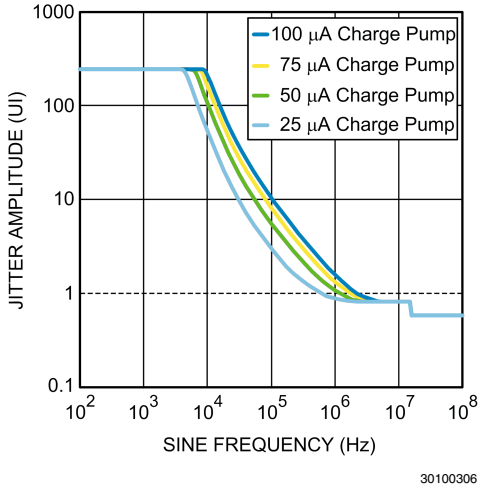


FIGURE 7. LMH0346 2.97 Gbps Jitter Tolerance with Different Charge Pump Current Settings

REGISTER 10h – POWERING DOWN THE SDO AND SCO/SDO2 CML DRIVERS TO SAVE POWER

The LMH0356 has two separate CML output drivers. These drivers can be independently powered down if not required in the system (i.e. if the system needs only one CML driver), as shown in *Table 4*. Approximate power savings is 24 mA/buffer.

TABLE 4. Register 10h – Powering Down the SDO and SCO/SDO2 CML Drivers

Address	R/W	Bits	Name	Default	Description
10h	R/W	7:3	RSVD	10000	Reserved. These bits must always be 10000.
		2	PD SDO	0	Power down SDO output driver. 0: Normal operation. 1: SDO output driver is powered down.
		1	PD SCO/ SDO2	0	Power down SCO/SDO2 output driver. 0: Normal operation. 1: SCO/SDO2 output driver is powered down.
		0	RSVD	0	Reserved. This bit must always be 0.

REGISTER 2Bh – ENABLE CONTROL

Register 2Bh is used for SMBus control of the ENABLE pin, as shown in *Table 5*.

TABLE 5. Register 2Bh – Enable Control

Address	R/W	Bits	Name	Default	Description
2Bh	R/W	7:6	RSVD	00	Reserved. These bits must always be 00.
		5:4	ENABLE	00	Device enable control. 00, 10: Enable is controlled by the ENABLE pin. 01: LMH0356 is powered down. 11: LMH0356 is enabled.
		3:0	RSVD	0000	Reserved. These bits must always be 0000.

REGISTER 2Ch – INPUT MUX CONTROL

Register 2Ch is used for SMBus control of the multiplexer select pins (SEL1, SEL0), as shown in *Table 6*.

TABLE 6. Register 2Ch – Input MUX Control

Address	R/W	Bits	Name	Default	Description
2Ch	R/W	7:4	RSVD	1000	Reserved. These bits must always be 1000.
		3:0	SEL	0000	Multiplexer select. 0000: Multiplexer select is controlled by the SEL1 and SEL0 pins. 0001, 0010, 0011, 0100: Reserved. **0101: SDI0 is selected.** 0110: Reserved. **0111: SDI1 is selected.** 1000, 1001, 1010, 1011, 1100: Reserved. **1101: SDI2 is selected.** 1110: Reserved. **1111: SDI3 is selected.**

REGISTER 32h – DETECTING THE LOCKED RATE AND DISTINGUISHING BETWEEN 3G, HD, AND SD

Register 32h can be read to determine the status of the lock detection state machine – and which data rate has been detected. While acquiring lock at a given frequency, the LMH0356 will automatically cycle through the following states:

1. Coarse acquisition (adjusts VCO center frequency with the control voltage held to mid-supply).
2. Frequency acquisition (tunes the VCO to a multiple of the 27 MHz crystal frequency).
3. Phase acquisition (tunes the VCO phase to optimally clock the data input to the LMH0356).
4. Locked.

The register values are shown in *Table 7*.

TABLE 7. Register 32h – Reading Back the Detected Rate

Address	R/W	Bits	Name	Default	Description
32h	R	7:4	STATE	0000	Status of Lock Detection State Machine. 0000, 0001, 0010, 0011: Reserved. 0100: Rate = 270 Mbps, Coarse acquisition. 0101: Rate = 270 Mbps, Frequency acquisition. 0110: Rate = 270 Mbps, Phase acquisition. **0111: Rate = 270 Mbps, LOCKED.** 1000: Rate = 1.483/1.485 Gbps, Coarse acquisition. 1001: Rate = 1.483/1.485 Gbps, Frequency acquisition. 1010: Rate = 1.483/1.485 Gbps, Phase acquisition. **1011: Rate = 1.483/1.485 Gbps, LOCKED.** 1100: Rate = 2.967/2.97 Gbps, Coarse acquisition. 1101: Rate = 2.967/2.97 Gbps, Frequency acquisition. 1110: Rate = 2.967/2.97 Gbps, Phase acquisition. **1111: Rate = 2.967/2.97 Gbps, LOCKED.**
		3:0	RSVD	0000	Reserved.

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