# Mixed Signal Testing Using the IEEE 1149.4 STA400

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## Introduction

Use of the IEEE 1149.1 (JTAG) standard is pervasive and has become established best practice for board debug, manufacturing test, and even remote test and diagnostics. Although very successful with digital devices, the standard deliberately ignored Analog and Mixed-Signal components, leaving those for IEEE 1149.4 to address. Extensive use of digital components with JTAG has in some cases eliminated the need for external test points and in-circuit testing. Analog circuitry in particular would benefit from additional shielding and the removal of test-points, potential benefits of the use of IEEE 1149.4.

The IEEE 1149.4 standard is intended to supplement the IEEE 1149.1 standard by adding provisions for mixed signal test capability. The two standards are very similar, with IEEE 1149.4 as a superset of the IEEE 1149.1. The IEEE 1149.4 standard requires additional circuitry, but then provides the means to measure passive component values, sample point voltages, and monitor low frequency signals. Since the standards are complimentary, boards can consist of a mix of 1149.1 and 1149.4 components on the same JTAG chain, and perform interconnect tests as previously done with just 1149.1 devices.

Let's Compare the Standards:

- Both include a TAP controller with identical pins and functionality.
- Mandatory instructions apply to both, BYPASS, EXTEST, SAMPLE.
- Optional instructions include HIGHZ, CLAMP, INTEST, and user defined.

IEEE 1149.4 also includes the following:

- Each pin has a 4 bit Analog Boundary Module (ABM)
- The 4 bits in the ABM: 2 bits for control of IEEE1149.1 force/capture, and 2 bits to control Analog switches. Analog switches are less than 30Ω nominal resistance.
- Two on-chip Analog Buses, AB1 and AB2 are connected to two off-chip Analog Buses, AT1 and AT2 through Analog switches in the Test Bus Interface Circuit (TBIC).
- The Analog Bus AT1/AB1 is used primarily as a current drive path.
- The Analog Bus AT2/AB2 is used primarily as a Voltage sense path.
- The PROBE instruction allows real time monitoring of Voltages.

## STA400 Description

The STA400 contains up to eleven ABMs and is fully compliant to IEEE 1149.4. Refer to the datasheet for the specific device details regarding pinout, functionality, and electrical characteristics. The BSDL model for the device describes the scan chain but for reference this information is listed below.

The purpose of this applications note is to provide a very basic description of how fundamental measurements can be made using the STA400, including:

- Monitoring of voltage at a pin
- Measuring a resistance, R, between a pin and Analog Ground
- Measuring a resistance, R, between two pins
- Measuring a resistence, R, between pin A and pin B, using a stimulus voltage source, $V_S$, and a sense resistor, $R_S$
- Measuring a resistance, R, between pin A and pin B, using a stimulus current source, $I_S$, and a precision resistor, $R_P$ (1%)
- Measuring a capacitance, C, between a pin and Analog Ground
- Measuring a inductance, L, between a pin and Analog Ground
- Measuring a capacitance, C, between pin A and pin B
- Measuring a inductance, L, between pin A and pin B

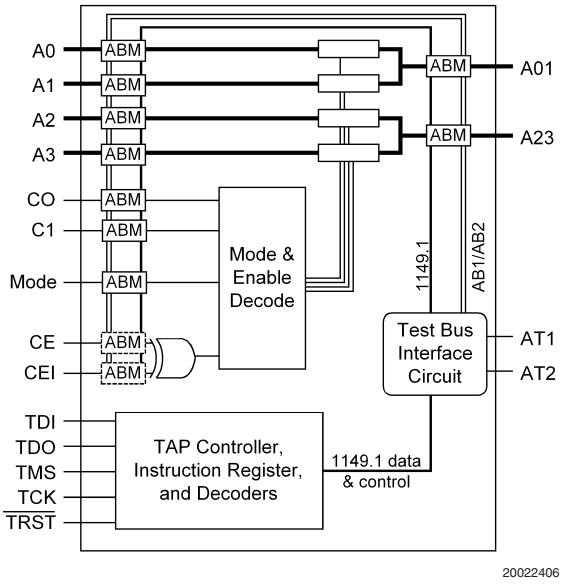


**FIGURE 1. Block diagram of STA400 device**

**Enabling ABM analog switches**

1. The instruction register has 20 bits; all data changes at falling edge of TCK (valid on rising edge); all data applied in sequence shown (left-most bit first).
2. Put the TAP controller into Test-logic-reset by applying momentary logic 0 on $\overline{\text{TRST}}$, or five logic 1's on TMS, on consecutive rising edges of TCK.





 

3. Put the TAP controller in Run-test/idle (if not already there from a previous sequence), by applying 0 to the TMS pin.
4. Next put the TAP controller into EXTEST, by applying 11100 on the TMS pin, immediately followed by 0000 0000 0000 0000 0000 on the TDI pin (and constant 0's on the TMS pin), then 110 on the TMS pin to return to Run-test/Idle.
5. Scan bits into the boundary scan register, via TDI, to enable appropriate switches, by applying 100 on the TMS pin, followed by (e.g, to enable AB2 switch of A0 pin, and AT2-AB2 switch in TBIC) 0000 0000 0000 0000 0000 0000 1000 0000 0000 0000 0000 0100 on the TDI pin (and constant 0's on the TMS pin).

**Monitoring of Voltage at a Pin**

1. Enable TBIC and ABM switches for AT2-to-pin path
2. Monitor voltage at AT2 with voltmeter. (Note 1)

**Note 1:** The frequency (MHz) of the monitored signal should be less than $16/C_{AT2}$, where $C_{AT2}$ is the total capacitance (pF) connected to AT2 due to the voltmeter and wire.

**Measurement scheme for a resistance, R, between a pin and Analog Ground**

1. Connect 1kΩ sense resistor, $R_S$, between stimulus signal source voltage and AT1
2. Enable TBIC and ABM switches for AT1-to-pin and AT2-to-pin paths
3. Into resistor, apply 200 mVp-p @ $f_S$=1 kHz with a DC offset equal to analog ground voltage. (Notes 2, 3)
4. Measure $V_S$: peak-to-peak AC voltage across sense resistor ($I_S = V_S / R_S$ ).
5. Measure voltage $V_1$ (voltage of pin, via AT2): peak-to-peak AC voltage at AT2. (Note 4)
6. $R = V_1 / I_S = R_S \times V_1/V_S$

**Note 2:** AC+DC stimulus is recommended to ensure that all offset voltages are cancelled. DC stimulus could be used if offset voltages are negligible, in which case, apply a DC voltage sufficiently different from analog ground to cause <100µA to flow, and measure DC voltage instead of peak-to-peak AC.

**Note 3:** A stimulus voltage is simpler to generate accurately, but a 200µAp-p AC (or 100µA DC) stimulus current could be used instead.

**Note 4:** Capacitance between AT1 and AT2 must be minimized (<10 pF), so ensure a DC wire is always placed between these signal wires.

## Measurement scheme for a resistance, R, between two pins

In order to measure an unknown resistance between two pins, we need to connect the pins to two ABM pins. The stimulus current source has to be connected to AT1, then we need to enable the TBIC and the ABM switches (AB1) to create a path for the current. The current flows through two switches, the resistor under test, and through the second pin to the second ABM. In order to create a full circuit for the current flow, we have to enable the virtual ground on the second ABM (the 0V buffer) with putting 0 on the Data bus (D, see BSDL) and 1 on the Control bus (C, see BSDL). Then the known current will introduce a voltage drop which we can measure with a voltmeter connected to the AT2 pin. For that, we need to open the AB2 switch in the TBIC and enable the AB2 bus and switches to reach the point of measure. We also have to measure the virtual ground by enabling the AB2 switches on the second ABM, so that the value of the unknown resistor would be obtained with the following equation:

$$R = [V_1 - V_2] / I_{current\ stimulus}$$

There are several ways to ensure the constant current stimulus. One is to use a voltage source and a sense resistor. For that, a third measuring point is introduced which is the sense resistor voltage drop used to calculate the stimulus current (I = Vs / Rs). Then, the unknown resistance becomes:

$$R = [V_1 - V_2] / I_S$$

or

$$R = Rs \times [V_1 - V_2] / V_S \text{ (voltage source)}$$

A second method to produce the desired current is to use a constant current source/generator. In order to ensure that the value of our current is what we intend it to be, a high precision resistor is included in parallel to our measuring scheme. The high precision resistor will give the value of the current after we measure its two nodes using the same methodology, previously explained. Then, the stimulus current is known to certain level of accuracy, and the measurement may proceed.

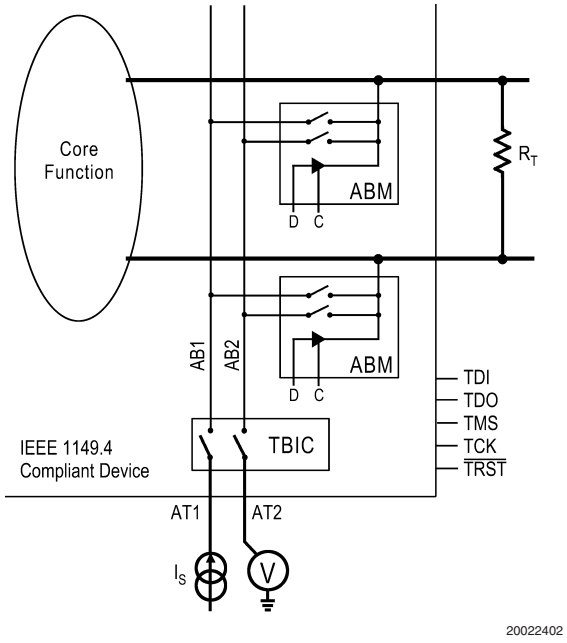


**FIGURE 2. Block diagram of device configuration for measuring a resistance between two pins**

## Measurement scheme for a resistance, R, between two pins

(Continued)

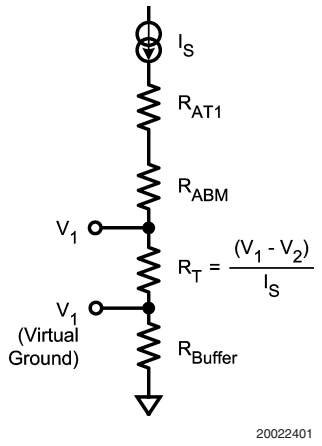


**FIGURE 3. Equivalent circuit for measuring a resistance between two pins**

**Measurement scheme for a resistance, R, between pin A and pin B, using a stimulus voltage source, $V_S$, and a sense resistor, $R_S$**

1. Connect 1kΩ sense resistor, $R_S$, between stimulus signal source voltage and AT1
2. Enable TBIC and ABM switches for AT1-to-pin A and AT2-to-pin A paths
3. Connect pin B to analog ground (logic 0) using 1149.1 boundary scan.
4. Into resistor, apply 200 mVp-p @ $f_S$=1 kHz with a DC offset equal to analog ground voltage. (Notes 2, 3)
5. Measure $V_S$: peak-to-peak AC voltage across sense resistor ($I_S = V_S / R_S$ ) using a third ABM pin for reaching the node of the $R_S$ voltage drop.
6. Measure voltage $V_A$ (voltage of pin A, via AT2): peak-to-peak AC voltage at AT2.
7. Disable ABM switch for AB2-to-pinA, and enable ABM switch for AB2-to-pinB
8. Measure voltage $V_B$ (voltage of pin B, via AT2): peak-to-peak AC voltage at AT2. (Note 4)
9. Calculate

$$R = (V_A - V_B) / I_S = R_S \times (V_A - V_B) / V_S$$

**Measurement scheme for a resistance, R, between pin A and pin B, using a stimulus current source, $I_S$, and a precision resistor, $R_P$ (1%)**

1. Connect the current source to the AT1 pin.
2. Enable the AB1 bus and two ABM switches on the respective pins to reach the two nodes of the precision resistor $R_P$ (one terminal to $I_S$, the other to analog ground). All in order to enable the current path thru $R_P$ to produce a voltage drop.
3. Enable the virtual ground (logic 0 on ABM bit "data" and logic 1 on ABM bit "control") on the second ABM, the one measuring the second terminal. This is done using 1149.1 boundary scan.
4. Connect your DAQ or measuring instruments to the AT2.
5. Measure the two nodes of the $R_P$ using two ABM pins with enabling their respective switches and read the values on AT2 (connected to your voltage measuring instrument or DAQ system). Record current value

$$I_S = [V_1(\text{first node}) - V_2(\text{second node})]/R_P$$

6. Connect the current source to the resistor under test following the same procedure as for the precision resistor. Let the current thru the resistor.
7. Enable the virtual ground on the second terminal ABM pin *Step 3*
8. Enable the ABM switches and AB2 and measure the node voltages on the resistor.
9. Calculate:

$$R = [V(\text{on the first pin}) - V(\text{virtual ground})] / I_S$$

**Measurement scheme for a capacitance, C, between a pin and Analog Ground**(Notes 5, 6, 7)

- Same as for a resistance, except

$$C = 1 / (2\pi f R) = V_S / (2\pi f_S R_S V_1)$$

**Note 5:** The stimulus must contain AC.

**Note 6:** The stimulus must be a voltage (or a current source in parallel with a large resistance).

**Note 7:** Be sure to provide time for any transient voltage across the capacitance to decay.

**Measurement scheme for an inductance, L, between a pin and Analog Ground**(Notes 8, 9, 10)

- Same as for a resistance, except

$$L = 2\pi f R = 2\pi f_S R_S V_1 / V_S$$

**Note 8:** The stimulus must contain AC.

**Note 9:** The stimulus must be a current (or a voltage source in series with a large resistance).

**Note 10:** Be sure to provide time for any transient voltage across the capacitance to decay.

**Measurement scheme for a capacitance, C, between pin A and pin B**(Notes 5, 6, 7)

- Same as for a resistance, except

$$C = 1 / (2\pi f R) = V_S / (2\pi f_S R_S (V_A - V_B))$$

**Measurement scheme for an inductance, L, between pin A and pin B**(Notes 8, 9, 10)

- Same as for a resistance, except

$$L = 2\pi f R = 2\pi f_S R_S (V_A - V_B) / V_S$$

For greater accuracy measurement, especially when measuring impedances less than 10Ω or more than 100kΩ, calibration of the analog buses is recommended. The DC leakage (current) and AC leakage (capacitance) between the analog buses and ground should be measured and accounted for using the calibration modes of the TBIC. Details of how to do this are documented in the 1149.4 standard (Chapter 9).

## Summary

As has been described in the last several pages, IEEE 1149.4 provides the ability to create virtual Analog test points. These test points may be used to monitor Voltages or AC signals, or in conjunction with a current source, accurately measure the impedance values of passive components. Since the standard is compatible with IEEE 1149.1, it also supports all of the IEEE1149.1 commands and capabilities.

The IEEE1149.4 standard is new and at present there are only a few ICs offering this capability. Devices such as the STA400 allow design and test engineers a vehicle to explore the potential benefits of this contactless mixed signal test capability. Continue to check the National Semiconductor s website at http://www.national.com/scan for current developments of this exciting new technology.

**ABM Bit Description**

| | |
|---|---|
| D | Data |
| C | Control/enable data output |
| B2 | AB2 switch enable |
| B1 | AB1 switch enable |

**TBIC Bit Description**

| | |
|---|---|
| D2 | AT2-AB2 switch enable, if CA=0 and CO=0 |
| D1 | AT1-AB1 switch enable, if CA=0 and CO=0 |
| C0 | Control/enable D2 & D1 output, if CA=0 |
| CA | Calibrate paths, if CO=0 |

**TBIC Bit Functions** (Note 11)

| D2 | D1 | C0 | CA | Function |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Disables both the AT1-AB1 switch and the AT2-AB2 switch |
| 0 | 1 | 0 | 0 | Enables only the AT2-AB2 switch (and disables the AT1-AB1 switch) |
| 1 | 0 | 0 | 0 | Enables only the AT1-AB1 switch (and disables the AT2-AB2 switch) |
| 1 | 1 | 0 | 0 | Enables both the AT1-AB1 switch and the AT2-AB2 switch |
| 0 | 1 | 0 | 1 | Connects AT1 to AT2 via AB1, for characterization |
| 1 | 0 | 0 | 1 | Connects AT1 to AT2 via AB2, for characterization |
| 0 | 0 | 1 | 0 | Drives both AT2 and AT1 to logic 0 |
| 0 | 1 | 1 | 0 | Drives only AT2 to logic 0, and AT1 to logic 1 |
| 1 | 0 | 1 | 0 | Drives only AT2 to logic 1, and AT1 to logic 0 |
| 1 | 1 | 1 | 0 | Drives both AT2and AT1 to logic 1 |

**ABM Bit Functions** (Note 11)

| D | C | B2 | B1 | Function |
|---|---|---|---|---|
| - | - | 0 | 0 | Disables both the AT1-AB1 switch and the AT2-AB2 switch |
| - | - | 0 | 1 | Enables only the AT1-AB1 switch (and disables the AT2-AB2 switch) |
| - | - | 1 | 0 | Enables only the AT2-AB2 switch (and disables the AT1-AB1 switch) |
| - | - | 1 | 1 | Enables both the AT1-AB1 switch and the AT2-AB2 switch |
| 0 | 0 | - | - | Tristates the pin |
| 0 | 1 | - | - | Drives a logic 0 at the pin |
| 1 | 0 | - | - | Drives a logic 0 at the pin (analog ground) |
| 1 | 1 | - | - | Drives a logic 1 at the pin |

**TAP Controller Instructions** (Note 11)

| Instruction | Binary Code | Description |
|---|---|---|
| BYPASS | 1111111111111111111 | Boundary scan bypassed, 1 bit between TDI-TDO |
| EXTEST | 00000000000000000000 | All pins controlled by boundary scan register |
| EXTEST | 11111111111111101000 | Alternative binary code for EXTEST |
| SAMPLE | 01111111111111111000 | Boundary scan register accessible but no update |
| FASTACC | 11111111111111001011 | Accesses registers and suppresses Capture-DR |
| INTESTD | 11111111111111110000 | Similar to 1149.1 INTEST |
| INTESTA | 11111111111111111000 | Same as INTESTD, but all pins connected to core |
| PROBE | 11111111111111111000 | 1149.4 instruction |
| HIGHZ | 01111111111111001111 | All pins tristate |
| CLAMP | 11111111111111101111 | All pins hold logic state |

**Note 11:** Right-most bit shifted into device first.

**Scan Chain Sequence**

According to BSDL Convention, Bit 0 is shifted in last.

| Pin Label | Scan Bit Number | Bit Label |
|---|---|---|
| A0 | 0 | D |
| | 1 | C |
| | 2 | B2 |
| | 3 | B1 |
| A2 | 4 | D |
| | 5 | C |
| | 6 | B2 |
| | 7 | B1 |
| C1 | 8 | D |
| | 9 | C |
| | 10 | B2 |
| | 11 | B1 |
| A1 | 12 | D |
| | 13 | C |
| | 14 | B2 |
| | 15 | B1 |
| A3 | 16 | D |
| | 17 | C |
| | 18 | B2 |
| | 19 | B1 |
| CE | 20 | D |
| | 21 | C |
| | 22 | B2 |
| | 23 | B1 |

According to BSDL Convention, Bit 0 is shifted in last.

| Pin Label | Scan Bit Number | Bit Label |
|---|---|---|
| AT1 | 24 | D2 |
| AT2 | 25 | D1 |
| | 26 | C0 |
| | 27 | CA |
| Mode | 28 | D |
| | 29 | C |
| | 30 | B2 |
| | 31 | B1 |
| CEI | 32 | D |
| | 33 | C |
| | 34 | B2 |
| | 35 | B1 |
| A23 | 36 | D |
| | 37 | C |
| | 38 | B2 |
| | 39 | B1 |
| C0 | 40 | D |
| | 41 | C |
| | 42 | B2 |
| | 43 | B1 |
| A01 | 44 | D |
| | 45 | C |
| | 46 | B2 |
| | 47 | B1 |



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