LMZ1050x SIMPLE SWITCHER® Power Module - Quick Compensation Component Design

National Semiconductor
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Introduction

Feedback loop system stability is one of the most important design aspects of switching power supplies. Stabilizing the feedback loop requires control theory knowledge and its design can be an intimidating and daunting task. Fortunately, the LMZ1050x simplifies the compensation design by integrating type II compensation which reduces the number of external compensation components to two. A few equations can be used to easily optimize transient performance and stability for any application.

Furthermore, this application note provides the power supply designer with verification and design support for stabilizing the LMZ1050x using any type of output capacitor material. This means the LMZ1050x can achieve stability with a wide range of output capacitances (C_O) and equivalent series resistances (ESR). Additionally, LMZ1050x is fully supported by WEBENCH® for a complete design solution.

Below are several equations to quickly calculate the compensation components for the LMZ1050x. Following the Quick Start section is background information showing how these equations were derived.

Quick Start Compensation Component Equations

First solve the equations below:

$$f_{LC} \cong \frac{1}{2\pi\sqrt{L_O C_O}}$$

$$f_{ESR} = \frac{1}{2\pi R_{ESR} C_O}$$

where C_O is the output capacitance value appropriately derated for applied voltage and operating temperature, R_{ESR} is the total equivalent series resistance of the output capacitor (s), L_O is 1.5 µH for LMZ10504/5 device, and L_O is 2.2 µH for LMZ10503 device.

$$C_{comp}(\text{pF}) = 7.5 \times \frac{L_O(\mu\text{H}) \times C_O(\mu\text{F})}{V_{IN\,(MAX)}\,(\text{V})}$$

where $V_{IN\,(MAX)}$ is the maximum operating voltage. The final two component values can be calculated:

$$R_{comp} = \frac{1}{2\pi C_{comp} f_{ESR}}$$

$$R_{fbt} = \frac{1}{2\pi C_{comp} f_{LC}}$$

The equations are set to achieve a loop gain bandwidth of 100 kHz and approximately 50° of phase margin.

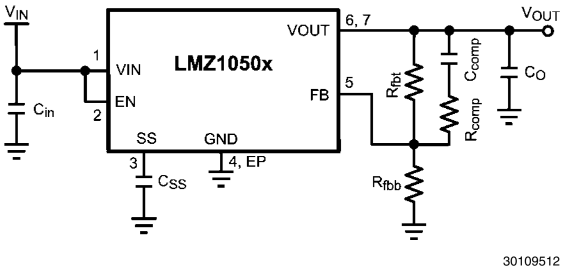

FIGURE 1. Typical Application Circuit

Compensation Component Equation Background

Our ultimate goal for designing the compensation stage is to provide an optimized transient performance and stability for any application. In general, a bandwidth of 200 kHz will provide a fast transient performance and a lower bandwidth will generally have a higher phase margin. The first step is to determine power stage transfer function poles and zeros. The power stage transfer function of a voltage mode buck converter has a complex double pole related to the LC output filter and a left half plane zero due to the output capacitor ESR, denoted R_{ESR}. The locations of these singularities are given respectively by

$$f_{LC} \cong \frac{1}{2\pi\sqrt{L_O C_O}}$$

$$f_{ESR} = \frac{1}{2\pi R_{ESR} C_O}$$

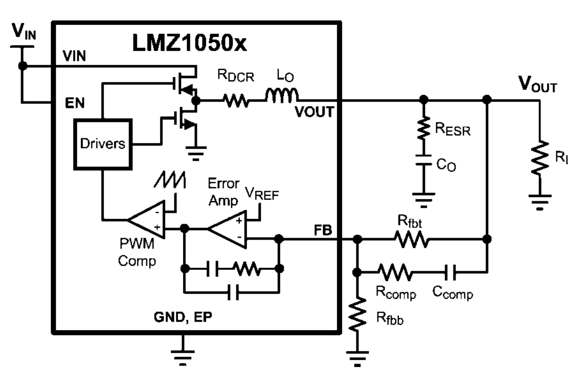

FIGURE 2. Complete Loop Gain Schematic

The conventional compensation strategy employed with voltage mode control is to use two compensator zeros to offset the LC double pole (f_{LC}), one compensator pole located to cancel the output capacitor ESR zero (f_{ESR}), and one compensator pole located at one half switching frequency ($f_{0.5 \times fsw}$) for high frequency noise attenuation.

The LMZ1050x internal compensation frequency locations are designed to locate a pole at the origin and a pole at high frequency as mentioned above. Furthermore, a zero is located at 17.6 kHz, to approximately cancel the likely location of one LC filter pole.

The three external compensation components, R_{fbt}, R_{comp}, and C_{comp} are selected to position a zero at the f_{LC} and a pole to cancel f_{ESR}. *Figure 3* and *Figure 4* depict the compensation strategy as explained above.

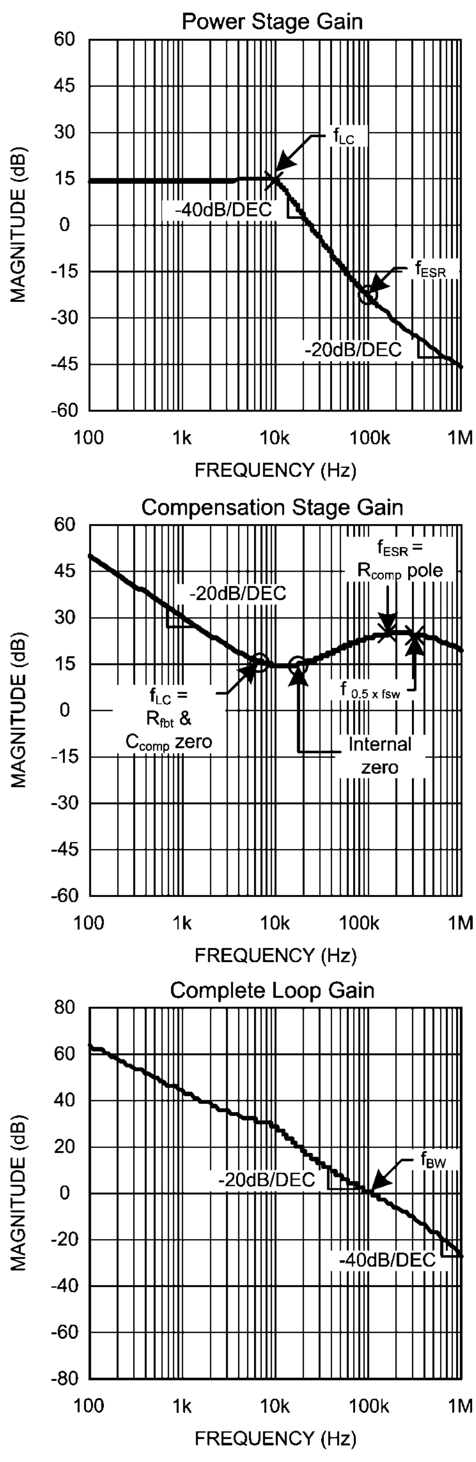

FIGURE 3. Gain Curves

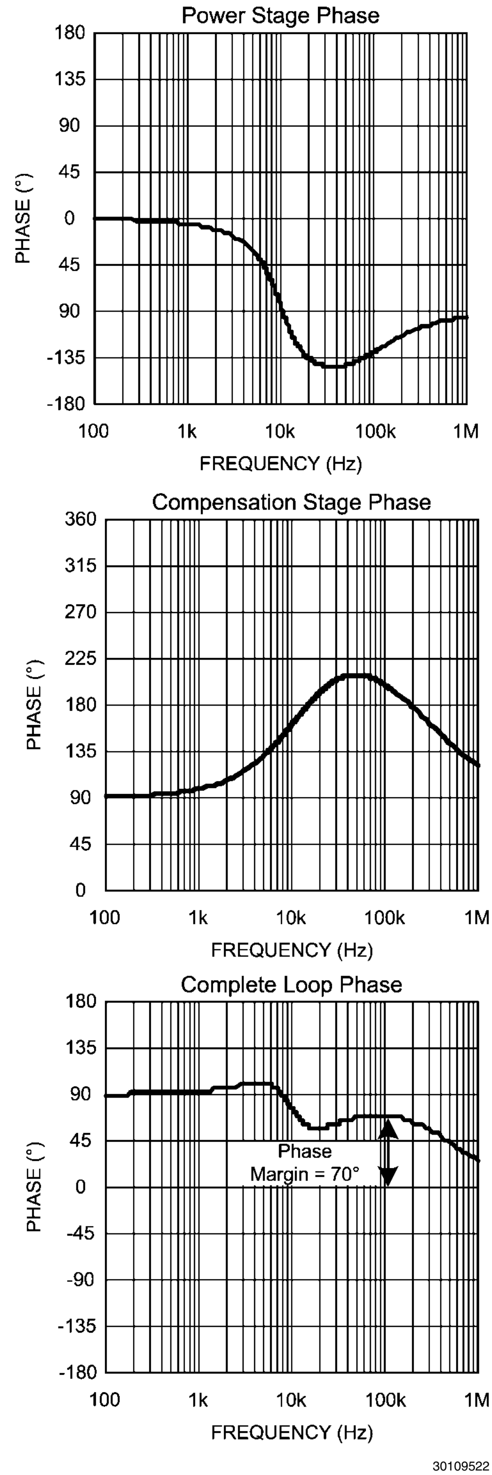

FIGURE 4. Phase Curves

The loop gain bandwidth frequency, f_{BW}, is suggested between one tenth to one fifth of the switching frequency, this range will provide a quick feedback loop response with 30 to 60 of phase margin. Phase margin will vary depending on the proximity of the f_{BW} to $f_{0.5 \times fsw}$.

$$0.1 \times 1\ \text{MHz} \geq f_{BW} \geq 0.2 \times 1\ \text{MHz}$$

As presented earlier the required external compensation capacitor, C_{comp} for type III compensation can be expressed as

$$C_{comp}(pF) = \alpha \times \frac{L_O(\mu H) \times C_O(\mu F)}{V_{IN\,(MAX)}\,(V)} \times f_{BW}\,(kHz)$$

where the constant α is nominally 0.075 and $V_{IN\,(MAX)}$ is the maximum operating voltage. This assumes a compensator pole will cancel f_{ESR}, which will be achieved with R_{comp}. Thus, it is recommended to design the loop at maximum expected $V_{IN\,(MAX)}$, since the modulator gain is proportional to V_{IN}, f_{BW} increases with increase in V_{IN}. The series resistor, R_{comp}, is selected to locate a pole at f_{ESR}. Thus

$$R_{comp} = \frac{1}{2\pi C_{comp} f_{ESR}}$$

The upper feedback resistor, R_{fbt}, is selected to provide adequate mid-band gain and to locate a zero at f_{LC}.

$$R_{fbt} = \frac{1}{2\pi C_{comp} f_{LC}}$$

Having calculated R_{fbt} with the equation above, R_{fbb} is then selected for the desired output voltage.

$$R_{fbb} = R_{fbt} \times \frac{V_{FB}}{V_{OUT} - V_{FB}}$$

where V_{FB} = 0.8V.

Note that the lower feedback resistor, R_{fbb}, has no impact on the control loop from an AC standpoint since the FB pin is the input to an error amplifier and effectively at AC ground. Hence, the control loop can be designed irrespective of output voltage level, V_{OUT}. The only caveat here is the necessary derating of the output capacitance with applied voltage.

The LMZ1050x data sheet provides a look up table of compensation components that work well with common output capacitor material to ensure stable operation. Values different than those listed may be used, but the compensation components may need to be recalculated to avoid reduction in bandwidth and phase margin. Note that the capacitance values in Table 2, Compensation Component Values, in LMZ1050x data sheet are adequately derated by 80% .

The LMZ1050x provides simplified type III compensation for the voltage mode control architecture and is flexible enough to allow all types of output capacitor material designs. The LMZ1050x is well balanced to support a wide range of R_{ESR} and C_o values while reducing the number of compensation components to two. For datasheet, WEBENCH®, evaluation board, application note, and reference design information go to: http://www.national.com/pf/LM/LMZ10504.html

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