PHYTER 100 Base-TX Reference Clock Jitter Tolerance

National Semiconductor
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1.0 Introduction

The use of a reference clock that is less stable than those directly driven from an oscillator may be required for some applications. In addition, some customer applications may require partnering with devices that operate outside of the IEEE 802.3 standard for transmitted jitter.

The PHYTER family is designed for robust operation and optimized for cable length and jitter tolerance performance far exceeding the IEEE specifications.

This application note is applicable to the following products:

DP83848C	DP83849C
DP83848I	DP83849I
DP83848YB	DP83849ID
DP83848M	DP83849IF
DP83848T	DP83640
DP83848H	
DP83848J	
DP83848K	

2.0 Summary

Although National Semiconductor recommends the use of stable clock sources with a minimum of jitter to achieve the best performance, the PHYTER family is capable of error free operation using imperfect reference sources and partners with excessive amounts of transmit jitter.

With up to 3.5 ns of jitter on the reference clock, the DP83849 PHYTER is capable of error free reception from a typical partner over 150 m of CAT5 cable. The DP83849 PHYTER, with a reference with nominal jitter, can recover data from signals transmitted with over twice the maximum allowable jitter at a cable length of 150 m.

Transmit tolerance of reference clock jitter is measured against the IEEE transmit jitter specification of 1.4 ns. Based on the measured data the DP83849 PHYTER can tolerate up to 1.1 ns of reference clock jitter before exceeding the IEEE requirement.

3.0 Theory

Clock jitter impairs any communication system and may have a severe impact on serialized data streams. Random jitter on the reference clock results in a frequency dependent noise component with energy spread across the spectrum, which impairs signal quality through the degradation of signal to noise ratio.

For random jitter, the ratio of peak to standard deviation depends on the bit error rate (BER) at which the system must operate. For a given BER, the magnitude of the Gaussian noise, on average, will not exceed the stated peak value more often than once every 1/BER. Therefore, as the peak to peak variation of random jitter increases, the BER degrades.

In designing a system, reference clock jitter is often specified in RMS units. For a Gaussian distribution, to convert between peak-to-peak (Pk-Pk) and RMS jitter, BER must be specified.

Table 1 lists common BER conversion factors from Pk-Pk to RMS.

TABLE 1. Peak-to-Peak to RMS Jitter Conversion Factor vs. BER

BER	10^{-10}	10^{-12}	10^{-14}	10^{-16}
Pk-Pk/ RMS Ratio	12.72	14.1	15.3	16.5

4.0 Receiver Architecture Review

When transmitting data at high speeds over copper twisted pair cable, frequency dependent attenuation becomes a concern. In high-speed twisted pair signaling, the frequency content of the transmitted signal changes significantly based on the transmitted data stream, in particular, the randomness of the scrambled data. The variation in signal attenuation caused by frequency variations must be compensated for to ensure the integrity of the transmission and accurate recovery and decoding of the received data stream.

Figure 1 illustrates the triple data histogram for a typical MLT-3 data stream. This signal would provide good BER because the tails of each distribution are far apart, providing ample room for properly decoding the three levels.

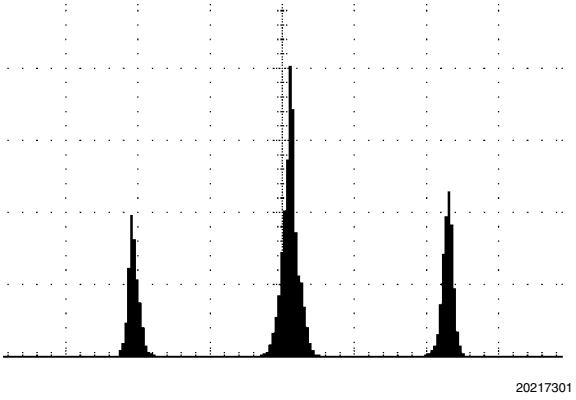

FIGURE 1. Transmit MLT-3 Waveform Histogram

In order to ensure quality transmission when employing MLT-3 encoding, the compensation must be able to adapt to various cable lengths and cable types depending on the installed environment. Therefore, the compensation or equalization must be adaptive to ensure proper conditioning of the received signal independent of the cable length.

The PHYTER family utilizes an extremely robust DSP equalization scheme with tightly coupled continuous Analog and Digital Adaptive Equalization. This is illustrated, along with a simplified view of the Analog Front End (AFE), in *Figure 2*.

The equalizer removes inter-symbol interference from the receive data stream by continuously adapting both the analog and digital equalizers to provide a filter with the inverse frequency response of the channel. When used in conjunction with a gain stage, the equalization enables the receive 'eye

pattern' to be opened sufficiently to allow very reliable data recovery and very robust noise tolerance.

An advanced Clock Recovery Loop ensures the data is always captured at the center of the equalized data pattern, minimizing jitter impairments that close the eye.

The equalizer is truly adaptive to any length of cable up to 150 meters.

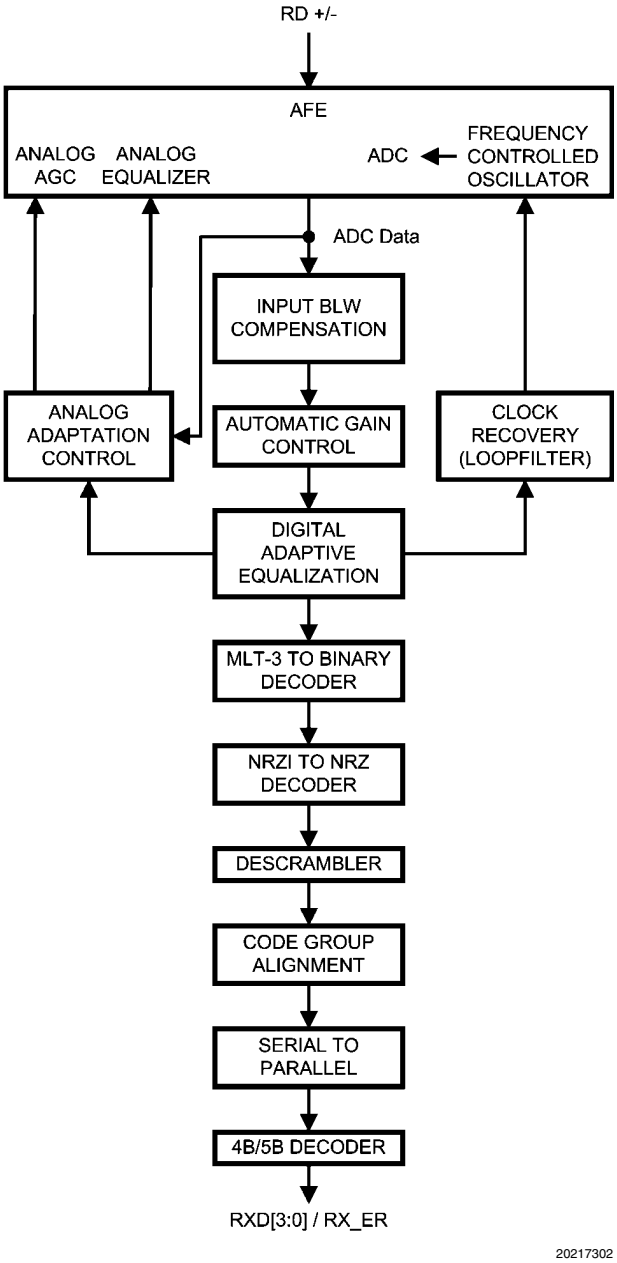

FIGURE 2. Receiver Architecture

5.0 Jitter Measurement

To validate the robustness of the PHYTER jitter tolerance, two DP83849 devices were linked together in 100 Base-TX mode across an adjustable length cable box of CAT5 cable. Jitter was induced to the reference clock of one of the devices at various levels. The performance of both short-term and long-term jitter was characterized.

Short-term jitter, caused by high frequency noise content, is typically defined as cycle-to-cycle jitter. For the purposes of this test, short-term jitter testing was performed with a 12 cycle interval. Long-term jitter, which is low frequency in nature, is defined such that the maximum jitter occurs after a sufficiently long time such that the system can track it. In this case, that time is 10 µs.

5.1 TEST SETUP

To induce the jitter on the reference clock, an FM modulated signal was used. The modulation frequency was set such that the peak jitter occurred at the desired measurement point (480 ns for short-term jitter, 10 µs for long-term jitter). The FM deviation controlled the amount of peak-to-peak jitter.

For short-term jitter, the signal generator was configured with a modulation frequency of 0.99 MHz and a deviation ranging from 0 kHz to 137.2 kHz. With 1 kHz of FM deviation producing approximately 25.5 ps of jitter, the total range of short-term jitter was approximately 150 ps to 3.6 ns. Long-term jitter was induced with an FM modulation of 49.9 kHz and the deviation varied from 0 kHz to 8 kHz. This produced jitter of approximately 150 ps to 4 ns with about 500 ps of jitter for each kilohertz of deviation. In both cases, using a modulation frequency that was not an even multiple of the clock frequency prevented the jitter from becoming synchronous with the clock frequency.

Reference clock and transmit signal jitter was measured with an oscilloscope using a delayed trigger, with the delay time equivalent to 12 or 250 cycles of the reference clock. In the case of transmit jitter, the Device Under Test (DUT) was programmed with auto-negotiation disabled and the RJ-45 connector terminated with a 100 ohm resistor between the transmit pair. A differential probe was used to capture the transmit idle waveform at the RJ–45 connector of the DUT.

For bit error rate testing, the digital packet generator configured the transmit packets and monitored packet counts on the DUT and its Partner, as shown in *Figure 3*. BER test results are based on 1 million packets of 1514 bytes (excluding CRC).

Several devices were tested from 3.0 V to 3.6 V and -40 °C to 85 °C to ensure robustness across environmental conditions.

5.2 TEST RESULTS

For reference, *Figure 4*, *Figure 5*, and *Figure 6* represent actual oscilloscope waveforms showing the MLT–3 waveform eye diagram with various levels of jitter. These waveforms were taken at the DUT transmitter near end and do not include the impairments of the 150 meters of cable. *Figure 5* illustrates the signal degradation with the 1.4 ns peak to peak maximum allowed by the IEEE transmit jitter specification.

The IEEE bit error rate specification for 100 Base-TX operation requires a BER of less than 10^{-7}. National Semiconductor devices are qualified to BERs of three orders of magnitude better (BER < 10^{-10}). Typical results from testing performed with a 150–meter CAT5 cable are shown in *Table 2* and *Table 3*.

Figure 7 and *Figure 8* are plots of the transmit jitter relative to the reference jitter.

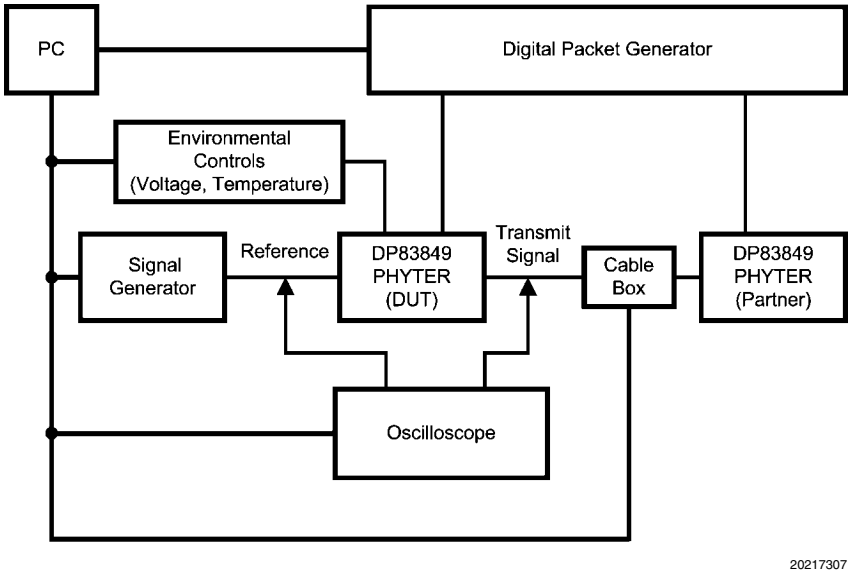

FIGURE 3. Simplified Test Setup

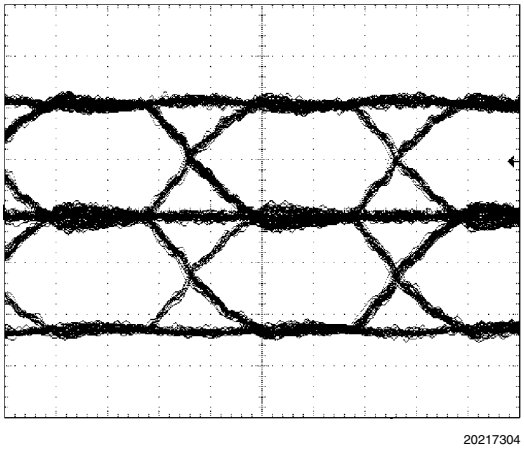

FIGURE 4. Transmit Signal Eye Diagram with Nominal Jitter

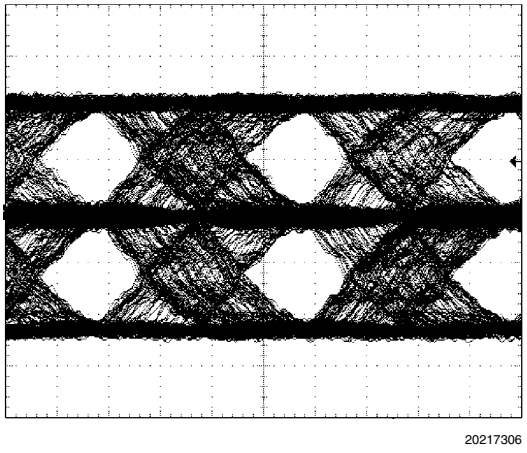

FIGURE 6. Transmit Signal Eye Diagram with 4 ns of Jitter

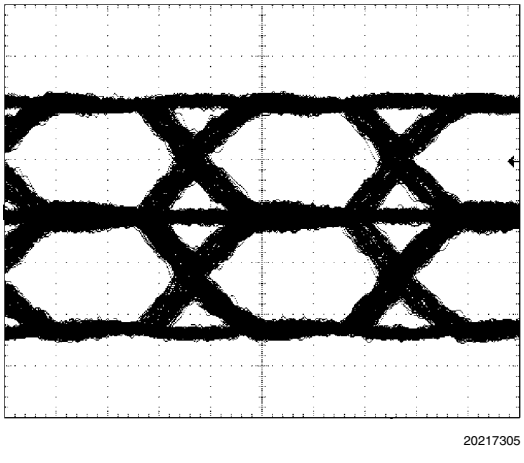

FIGURE 5. Transmit Signal Eye Diagram with 1.4 ns Jitter (Maximum Allowed by IEEE Specification)

TABLE 2. Transmit Jitter and RX Errors as Functions of Peak-to-Peak Short-Term Jitter (12 cycles, 150 m)

Reference Clock Jitter (ns)	Transmit Jitter (ns)	DUT RX Errors	Partner RX Errors
0.16	0.35	0	0
0.64	0.79	0	0
1.12	1.39	0	0
1.64	2.01	0	0
2.12	2.59	0	0
2.64	3.21	0	2 CRC
3.16	3.84	0	21 CRC
3.64	4.36	2 CRC	148 CRC

TABLE 3. Transmit Jitter and RX Errors as Functions of Peak-to-Peak Long-Term Jitter (250 cycles, 150 m)

Reference Clock Jitter (ns)	Transmit Jitter (ns)	DUT RX Errors	Partner RX Errors
0.14	0.35	0	0
0.60	0.77	0	0
1.10	1.25	0	0
1.62	1.75	0	0
2.12	2.27	0	0
2.63	2.79	0	0
3.16	3.30	0	4 CRC
3.66	3.81	0	33 CRC
4.19	4.31	1 CRC	277 CRC

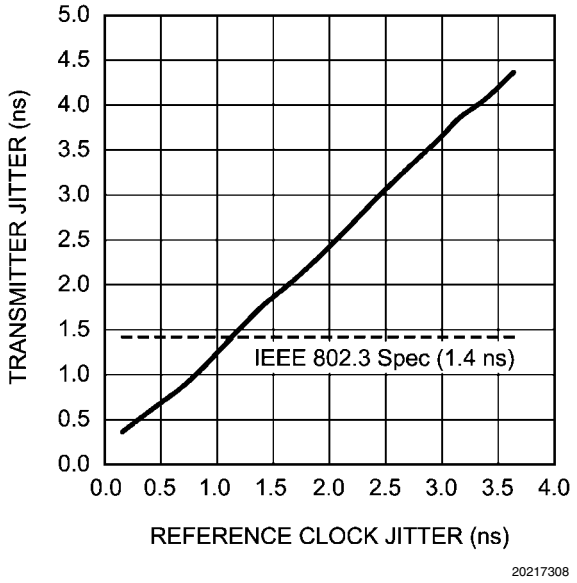

FIGURE 7. Peak-to-Peak Transmit Jitter as a Function of Peak-to-Peak Short-Term Jitter (12 cycles)

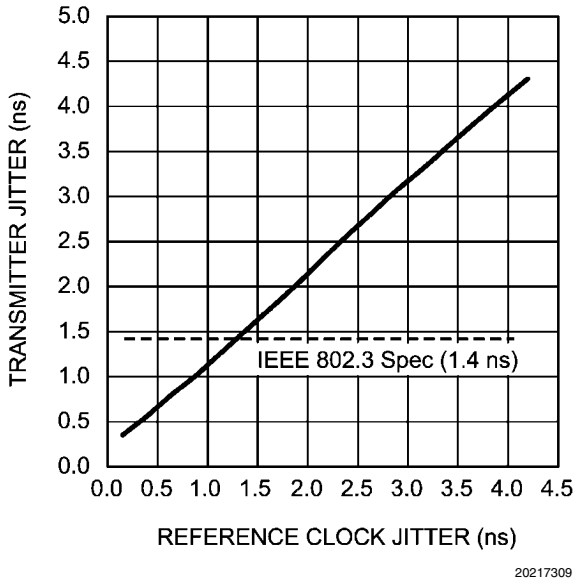

FIGURE 8. Peak-to-Peak Transmit Jitter as a Function of Peak-to-Peak Long-Term Jitter (250 cycles)

6.0 Conclusion

The PHYTER receiver architecture's DSP equalization scheme with tightly coupled continuous Analog and Digital Adaptive Equalization and advanced Timing Recovery Loop is designed to tolerate both short-term jitter and long-term jitter. It is also capable of adapting to channel impairments up to 150 meters of CAT5 cable. The system ensures data is captured at the center of the open eye, providing extremely reliable data recovery and jitter tolerance well beyond the IEEE limits.

Based on the measured data shown in *Table 2* and *Table 3*, at a BER three orders of magnitude better than IEEE specifications, BER < 10^{-10}, a DP83849 PHYTER with nominal reference jitter can detect signals with over twice the maximum allowable transmit jitter at 150 m of cable length. Even with 3.5 ns of jitter on the reference clock, the DP83849 PHYTER is capable of error free reception over 150 m of CAT5 cable from a typical partner. Increased amounts of jitter can be tolerated at shorter cable lengths.

For the transmit path the reference source is not filtered. As a result, the transmit jitter tracks the increase in the jitter of the reference. It can be seen from the plots in *Figure 7* and *Figure 8* that as the reference jitter exceeds 1 ns the transmit jitter approaches the IEEE specification limit of 1.4 ns.

Notes

Notes

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