Pspice Universal Test Circuits

National Semiconductor
Application Note 1516
Soufiane Bendaoud
January 26, 2009

There is no doubt that Spice models have gained a lot of popularity over the past years. While IC manufacturers strive to provide their customers with accurate models, it is really the system designer who dictates the trend of this accuracy and the innovation in the development of Spice macro models.

Many IC companies praise and brag about how their models are the best or offer revolutionary features but what they often fail to provide is some sort of circuit that allows the user or their customer to verify the accuracy of the macro model. Op amps macro models are probably the most sought after and while they can be extremely helpful when accurate, they can also cause serious problems, especially when they are not in the hands of experts.

Most system design engineers take the time to test the op amp macro model by itself before implementing it in a more comprehensive circuit. Unfortunately, sometimes use of non-accurate models lead designers and users to think that the amplifier is faulty, when the actual problem lies either in the model itself or in not properly setting the SPICE test environment. The truth is, all models are not the same and some may not work in a particular setting; so rather than investigating the shortcomings of op amp macro models, this document provides a collection of circuits that allow users to test any op amp model, in a way somewhat universal test circuits for op amp macro models.

What Parameters Should Be Tested?

Macro models differ in the level of complexity. Much like datasheets, the models should emulate parameters that are relevant to applications in which the op amp is thought to be appropriate. For example if a rail to rail output op amp is used, then the user should be able to test and verify the output saturation voltage versus the load current. Likewise, a low noise amplifier should have a model that emulates at least the voltage noise among other modeled parameters.

Despite their differences, amplifier macro models have a lot in common; these parameters are of the greatest interest and they are usually the starting point of the simulation. Below is a list of these parameters along with the corresponding test circuits and the simulations.

Open Loop Gain And Phase Margin

The open loop gain versus frequency is probably the very first test that engineers perform to evaluate the amplifier's macro model performance. This test is important because it shows the DC gain, the –3 dB frequency, the unity gain bandwidth and the phase margin *Figure 1* shows test circuit. The RC network ensures that the output is biased at a suitable DC voltage, (mid rail in this case). At higher frequencies, the capacitor shorts the inverting input to ground which, in turn places the op amp in open loop. The capacitor is chosen to be large to provide an early roll off ($f = 1/2\pi R_1 C_2$) so that even if the op amp tested has a very low frequency dominant pole, the simulation shows a smooth transition and 20 dB per decade roll off.

When testing open loop gain and phase, the user should choose an upper frequency limit that goes beyond the unity gain bandwidth of the amplifier.

When using rail to rail output models, it is important to use the test circuit with the same load indicated in the datasheet, otherwise the result might not reflect the actual amplifier's capabilities. This is especially true about the DC gain ($A_{OL}= g_m R_L$).

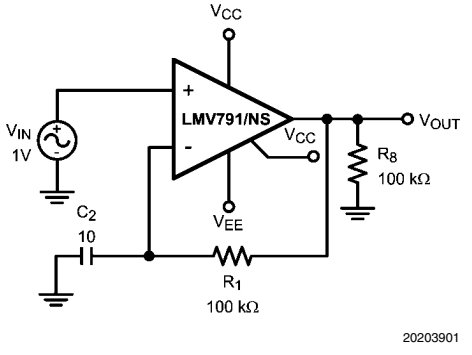

FIGURE 1. Open Loop Gain and Phase Test Circuit

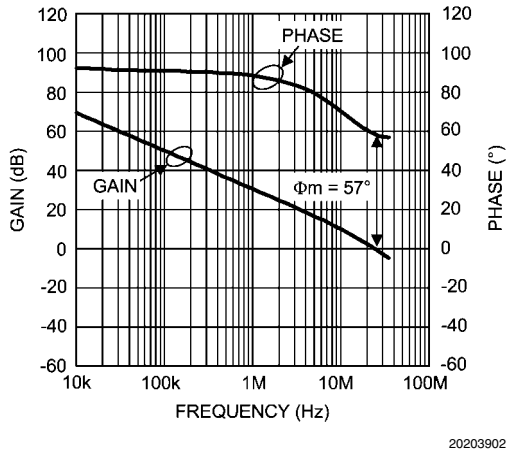

FIGURE 2. Simulated Open Loop Gain and Phase

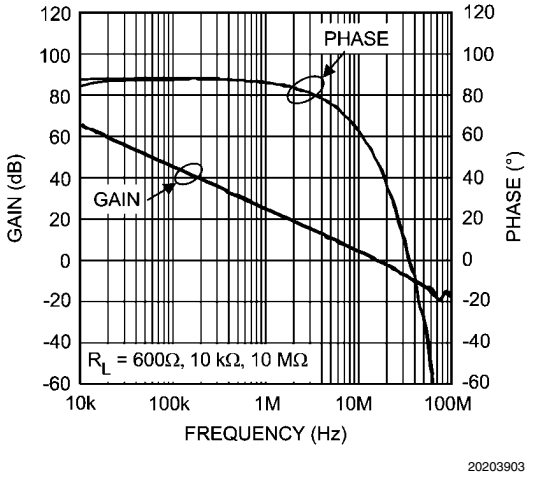

FIGURE 3. Measured Open Loop Gain and Phase

Slew Rate

This is another element that defines the amplifier's speed and is frequently modeled. Slew rate is usually determined by the ratio of the tail current and the compensation capacitance (I/C).

Since we already know the relationship I*dt = C*dv, we can simply use the circuit in *Figure 4* and take the derivative of the output to get the slew rate. Use the insert command in the probe screen of Pspice to add the letter "d" preceding the output voltage probe.

To assure this test circuit works properly, the input step function should have an amplitude large enough so that the effects of slew rate limitation are visible When running the simulation for slew rate, make sure the input signal rise and fall times are shorter the amplifier's expected slew rate. This is to ensure that the test results are dominated by the amplifier's slew rate. On the other hand, choose the input signal frequency accordingly with the op amp's speed. An input signal that's too fast will give you convergence problems.

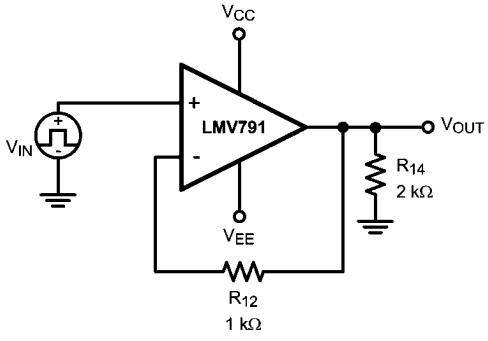

FIGURE 4. Slew Rate Test Circuit

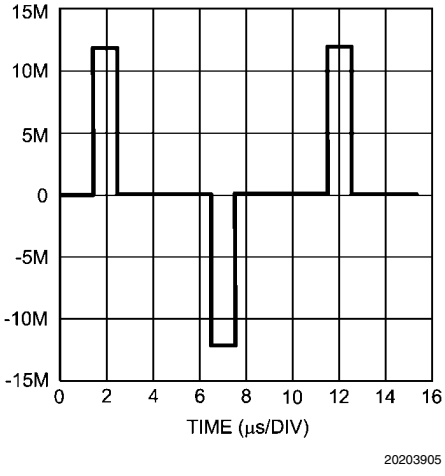

FIGURE 5. Simulated Slew Rate

CMRR and PSRR

These two parameters are not always modeled but they can be equally important. CMRR and PSRR are fairly easy to implement in a model as they usually consist of a simple RC network, a resistor divider and a voltage controlled voltage source.

CMRR is especially important in non inverting configurations because of the modulation of the non-inverting input with the input signal. PSRR on the other hand is important in any application where the voltage supply is susceptible to any interference or for DC PSRR where the supplies can experience significant variation.

The test circuits presented in *Figure 6* and *Figure 9* allow the user to simulate these two parameters. If they are modeled correctly, the pole and zero location should match the graphs in the datasheet.

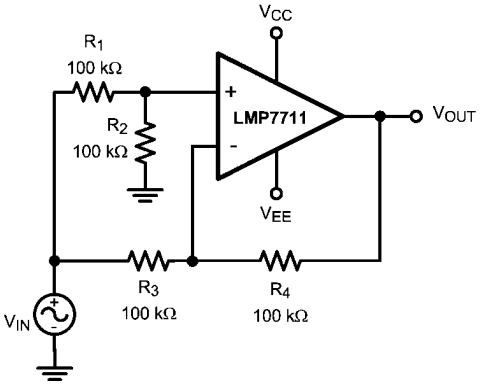

FIGURE 6. CMRR TEST CIRCUIT

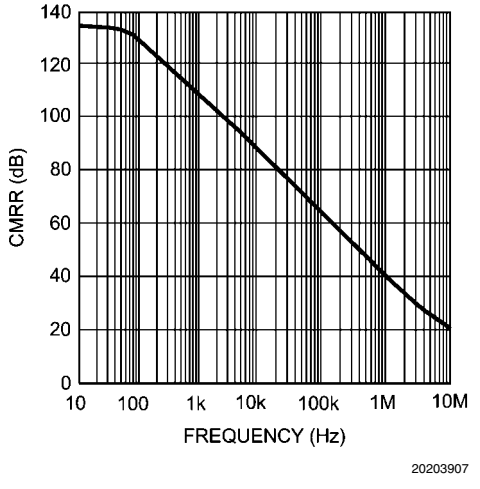

FIGURE 7. SIMULATED CMRR RESPONSE vs. FREQUENCY

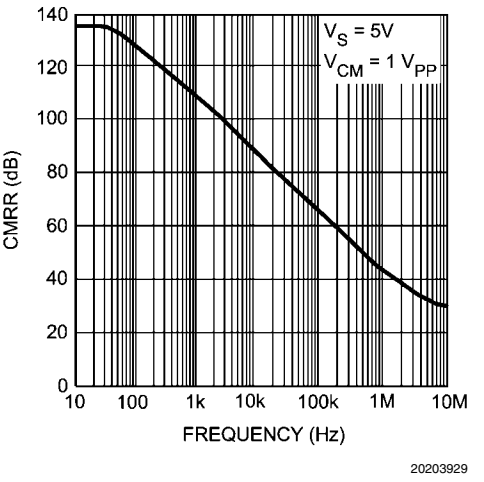

FIGURE 8. Measured CMRR vs. Frequency

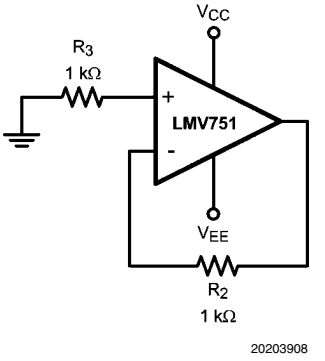

FIGURE 9. PSRR TEST CIRCUIT

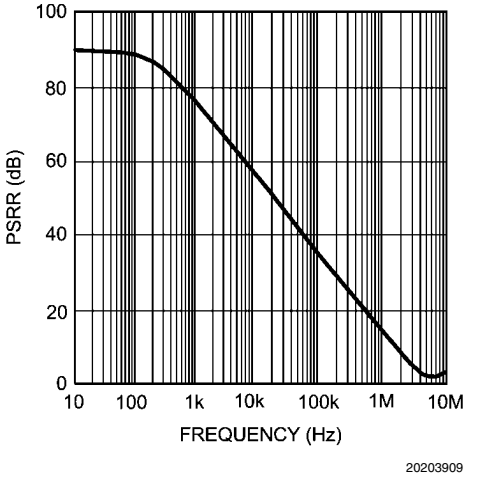

FIGURE 10. SIMULATED PSRR RESPONSE vs. FREQUENCY

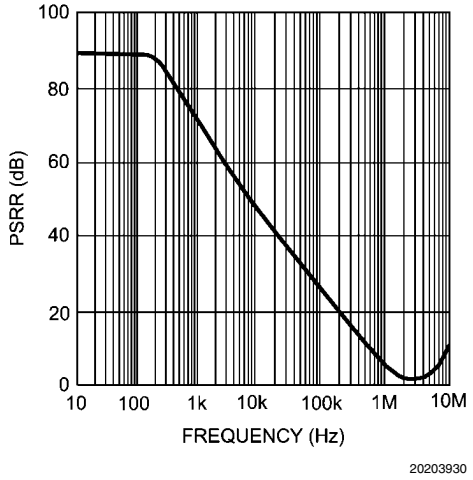

FIGURE 11. Measured PSRR vs. Frequency

Closed Loop Output Impedance

This is a specification that is often omitted from the datasheets altogether but is sometimes needed and necessary.

When modeled correctly, the output impedance helps in getting a more accurate settling time behavior under various capacitive loads.

The output impedance is also needed to calculate the proper component values when a compensation scheme is considered for stability purposes.

The test circuits of *Figure 12* provide the user with 3 curves for the output impedance vs. frequency at different gains, a gain of 1, 10 and 100. The output impedance is obtained by taking the ratio of the output voltage over the current (1A source at the output of the amplifier).

The graph in *Figure 13* shows the closed loop output impedance of the LMV791. At higher frequencies (where the curves flatten) the value is about 120Ω. Make sure to plot the curves on a log log scale.

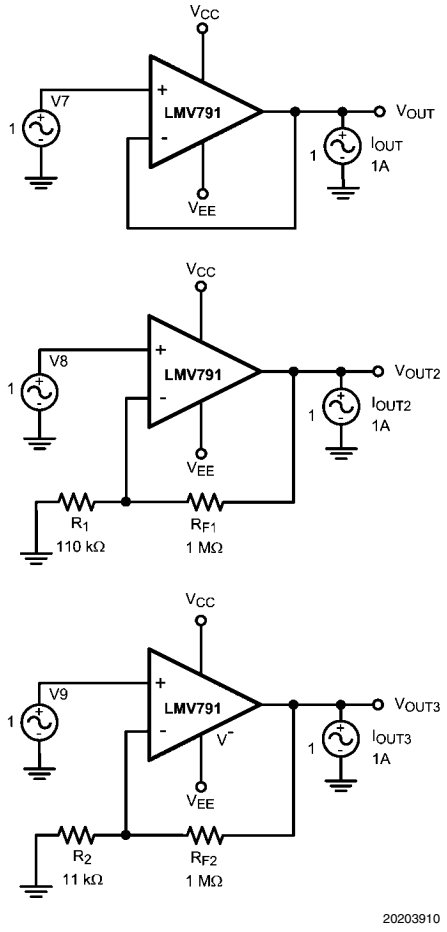

FIGURE 12. Output Impedance Test Circuits for a gain of 1, 10 and 100

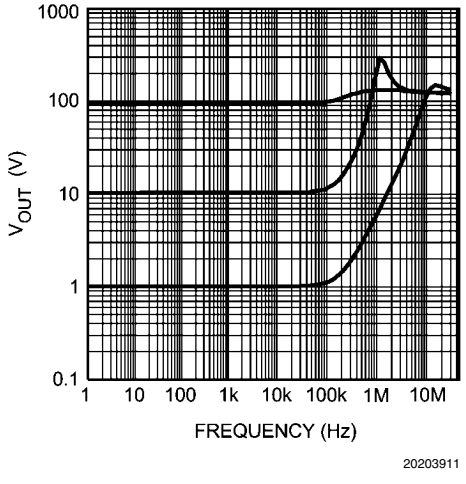

FIGURE 13. Simulated Closed Loop Output Impedance

Voltage And Current Noise

If there is an area where the folks creating amplifier macro models have made progress, this is one of them. Some of today's models allow users to simulate voltage noise with its flicker noise component and current noise with excellent accuracy. Modeling noise into the macro model doesn't take much more computing or simulation time but it is somewhat a difficult task, at least until you figure out the right equations that make the voltage noise density curve mimic the datasheet graph with the 1/f corner as well. One can easily test the voltage noise density by taking the output of a voltage follower (with a voltage source of 0 volts) on a log log scale. To simulate the current noise density, the same circuit can be used with a 100 kΩ resistor placed in series with the non inverting terminal. In the probe window, make sure to divide the result by the value of the resistor chosen, 100 kΩ in this case.

Using a large resistor value makes the current noise dominate since it is coupled into the resistance and thus voltage noise and thermal noise become negligible compared to the current noise. Of course, there are some exceptions where the current noise is very low and a higher source resistance may be needed. It's always good practice to evaluate the noise sources as a function of the source impedance. It is important to specify the output voltage in the analysis setup window of Pspice. In *Figure 14*, the output voltage is specified as V (V_{OUT}) and the input voltage as V_{IN} and box "noise enabled" is checked.

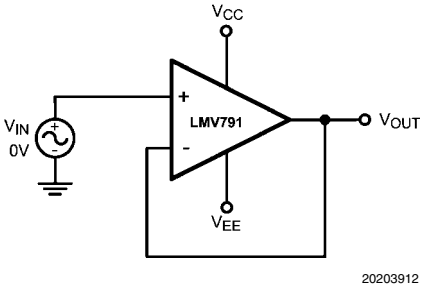

FIGURE 14. Voltage Noise Density Test Circuit

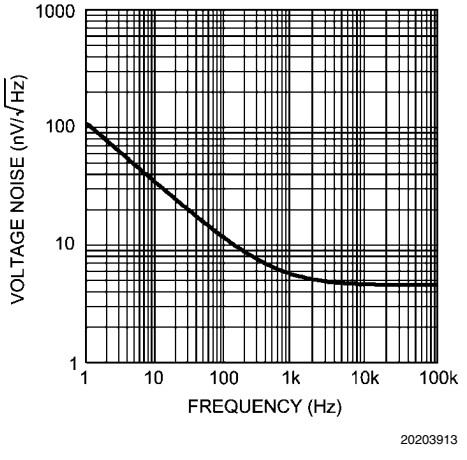

FIGURE 15. Simulated Voltage Noise Density

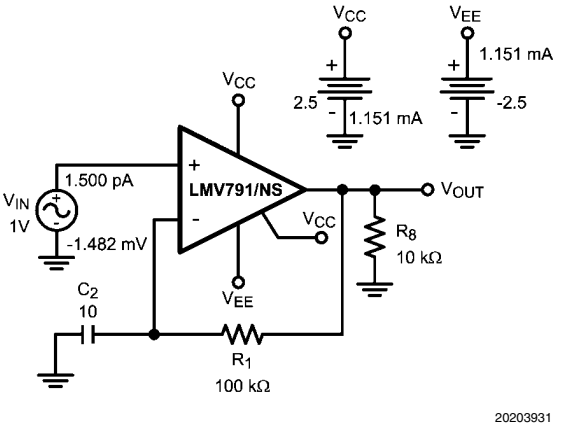

FIGURE 16. Current Noise Density Test Circuit

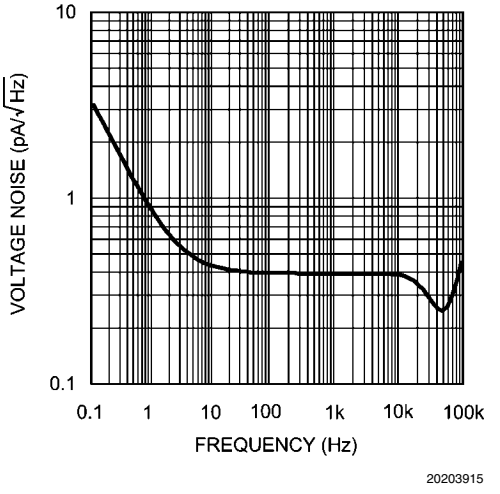

FIGURE 17. Simulated Current Noise Density

Input Bias Current and Input Offset Voltage

These parameters are probably the easiest ones to model. Input offset voltage can easily be implemented as a voltage controlled voltage source at the input whose value is taken from the datasheet.

In general, no specific test circuit is needed for testing bias current or offset voltage. Any of the circuits already discussed in this document can be used. In order to view the values of offset voltage and bias current, the user must activate voltage and current labels in SPICE. This is shown in *Figure 18* where the input bias current is 1.5 pA and the input offset voltage is 1.48 mV.

The current shown through the voltage supplies of 1.15 mA is the quiescent current.

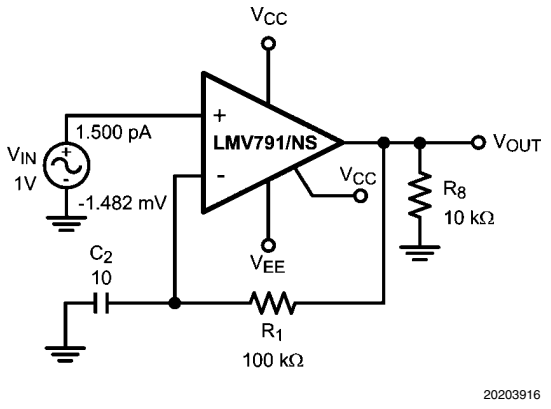

FIGURE 18. Offset Voltage and Input Bias Current

Output Saturation Voltage

This parameter is also known as the dropout voltage. It is particularly important in rail to rail output amplifier models as it represents the output voltage swing as a function of the load current and can help the system designer choose the appropriate op amp especially when driving heavy loads or when dynamic range is a concern.

The test circuit uses a simple DC sweep with 2 equal input voltages of opposite magnitude to replicate the sourcing and sinking of the load current.

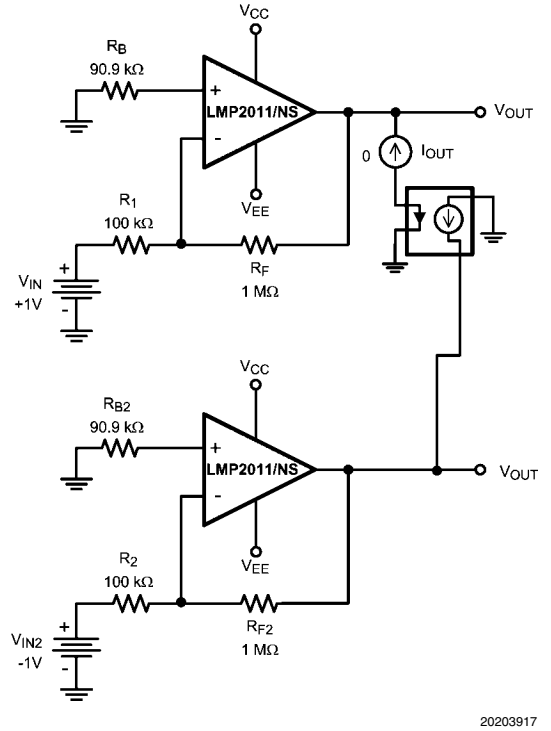

FIGURE 19. Output Saturation Voltage vs. Load Current Test Circuit

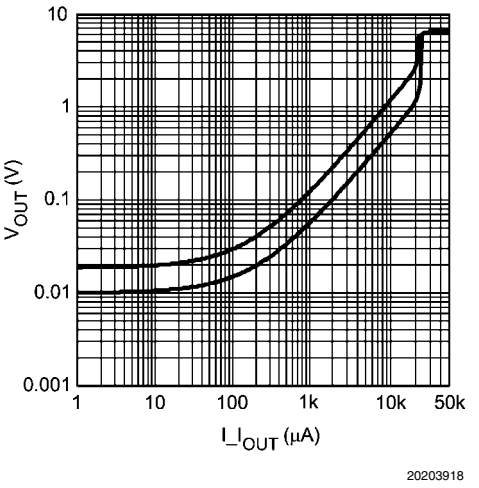

FIGURE 20. Simulated Output Saturation Voltage

Supply Current vs. Supply Voltage

The test circuit below sweeps the current across the supply and allows the user to determine how much current is drawn by the amplifier at different supply voltages. This test is particularly helpful for power conscious applications.

The slope of the supply current curve can easily be added into the model.

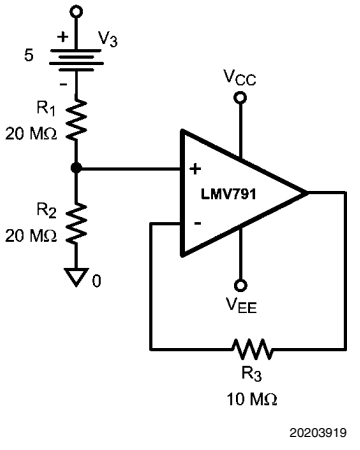

FIGURE 21. Supply Current vs. Supply Voltage

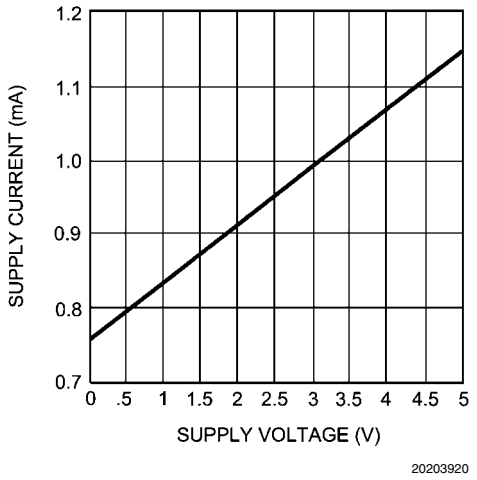

FIGURE 22. Simulated Supply Current vs. Supply Voltage

Overshoot And Transient Response

This test circuit serves 2 purposes: testing the transient response (whether small signal or large signal) and the overshoot.

Overshoot is important because it indicates how much ringing an amplifier has in the presence of a capacitive load. Overshoot is a measure of stability in time domain; it is the equivalent of what peaking is in the frequency domain.

Some macro models use extra passive components to mimic the overshoot accurately but generally, if the phase margin is accurate, the overshoot should come pretty close to what is should be.

The transient response can be tested using the test circuit used for the overshoot test, without the 100 pF capacitor. Some datasheets indicate whether a small capacitance is used as a load when measuring the small signal transient, in that case simply use the same value of capacitance.

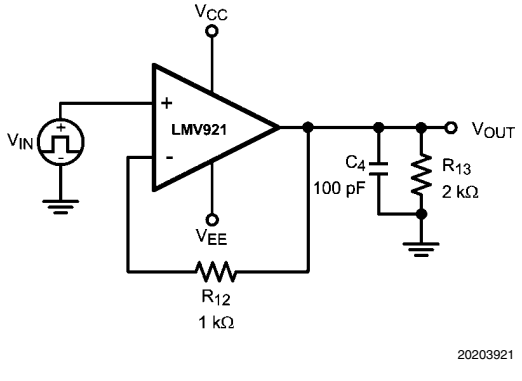

FIGURE 23. Overshoot Test Circuit

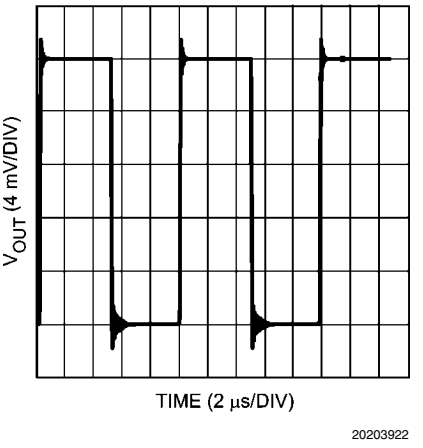

FIGURE 24. Simulated Overshoot

Common Mode Voltage Range

This parameter is important as it allows the user to see the head room or how far away the input signal needs to be from the supply.

The first test circuit in *Figure 25* uses a voltage controlled voltage source. In the second test circuit , *Figure 27*, the voltage is swept from –2.5V to 2.5V.

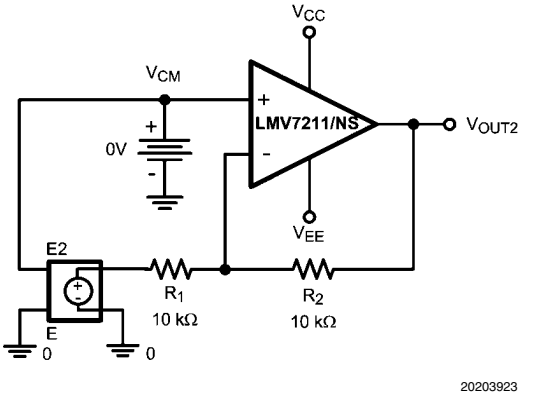

FIGURE 25. CMVR Test Circuit

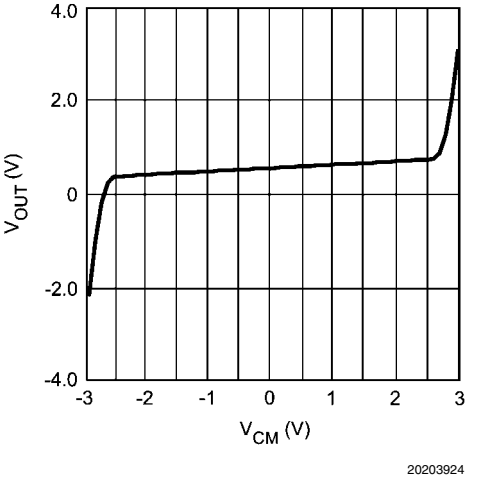

FIGURE 26. Simulated CMVR

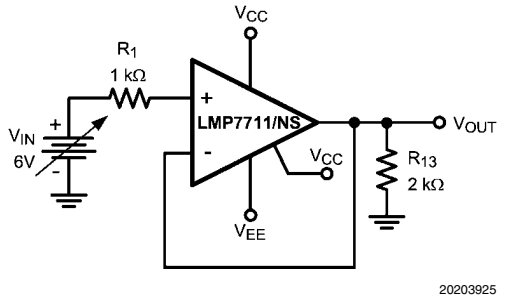

FIGURE 27. CMVR Test Circuit (optional)

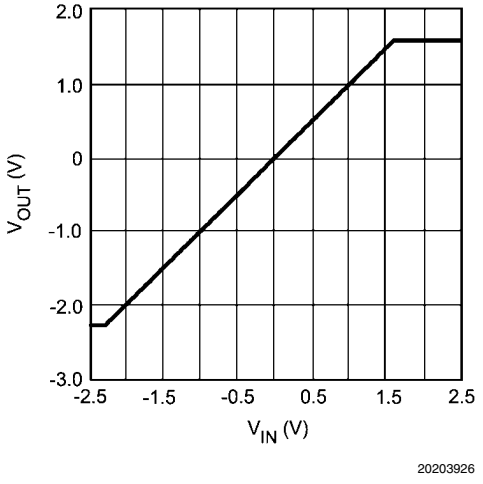

FIGURE 28. Simulated CMVR

Phase Reversal

Phase reversal occurs in some amplifiers when the input signal exceeds the input common mode voltage range. During a phase reversal, the output changes polarity and may cause damage to the op amp resulting in system lockups.

The test circuit is a simple voltage follower with a sine wave input which goes beyond the common mode voltage range of the amplifier, 6V in this example. The output waveform shown in *Figure 30* indicates that the macro model just like the op amp doesn't exhibit any phase reversal, it is clipped at ±2.5V.

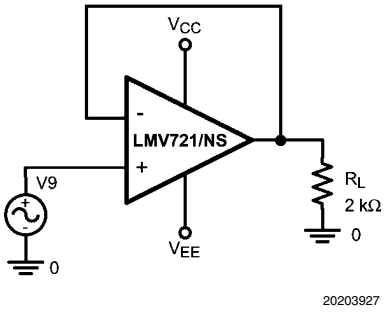

FIGURE 29. No Phase Reversal Test Circuit

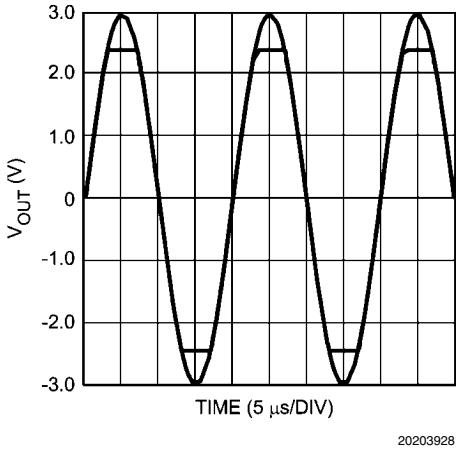

FIGURE 30. No Phase Reversal

Conclusion

The test circuits described above are not meant to replace the evaluation of the device on the bench. Rather, they provide the user with the flexibility of making quick assessments with respect to the accuracy of the macro model.

Special thanks to the applications group and the design community at National Semiconductor for their thoughtful insights.

Notes

Notes

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