

Simplified Programming of Altera FPGAs Using a SCANSTA111/112 JTAG Scan Chain Mux

National Semiconductor
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The SCANSTA111/112 Provides a Straightforward and Flexible Method of Isolating Scan Chains for Simplified Programming.

Many modern communication and networking systems incorporate a system-wide IEEE 1149.1 (JTAG) test bus. The test bus not only enables a comprehensive, life-cycle approach to system test, but it also offers a number of additional benefits to the system designer.

The utility of the JTAG bus continues to expand beyond the boundaries of just test. JTAG is now used for emulation, memory programming, and configuration of CPLDs or FPGAs. These applications of the JTAG bus are well supported by the industry.

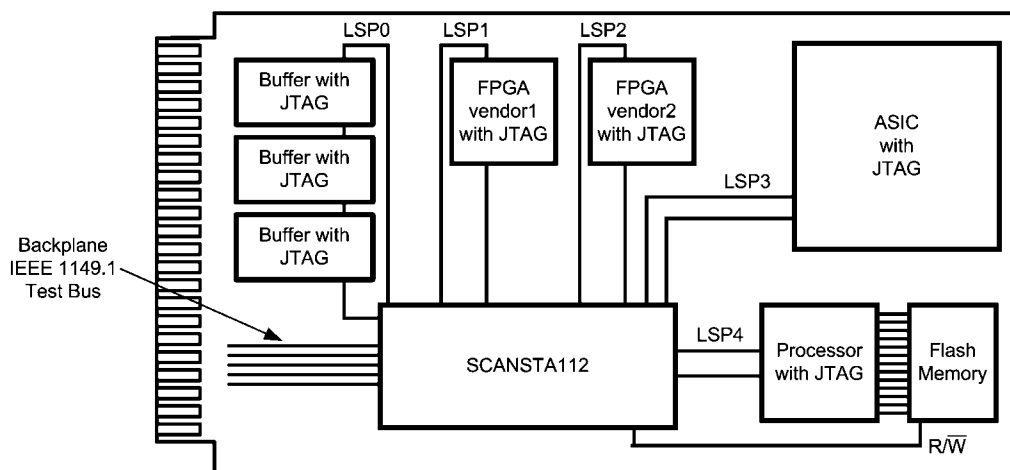
JTAG bus infrastructures continue to become more extensive, expanding to many devices on a circuit board and to multiple boards within a system. The need to manage the JTAG bus becomes apparent as the bus infrastructure expands. Grouping devices with similar technologies into smaller, local scan chains can reduce complexity and improve debug and fault isolation. Partitioning sets of components into local scan chains maximizes access for speed-critical applications, such as configuring large CPLDs or FPGAs or sets of such devices.

Systems with multiple cards and complex backplanes are designed to extend the JTAG infrastructure on each circuit card by extending the JTAG test bus across the backplane. Multiple cards can share the test bus when each card utilizes a JTAG interface device that enables multidrop addressing using the JTAG TAP.

National Semiconductor's SCANSTA111 and SCANSTA112 (STA11x) devices enable partitioning of complex scan chains. The SCANSTA111 and SCANSTA112 support multidrop addressing, and manage up to three or seven local scan chains respectively. The STA11x devices are commonly used for isolating components on a circuit board,. This is particularly useful for configuring CPLDs or FPGAs.

When developing configuration vectors for Altera CPLDs, adding the STA11x into the scan path introduces a new device that the synthesis tool is not expecting. For some STA11x operating modes, the output of the synthesis tool, either JAM STAPL or SVF (Serial Vector Format), must be modified in order to access the target device through the STA11x.

In order to configure an Altera device, a few simple additional steps are needed. The following provides a basic description of how to accomplish this.



Typical use of SCANSTA112 to manage multiple JTAG chains on a single board

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SCANSTA111/112 Operating Modes

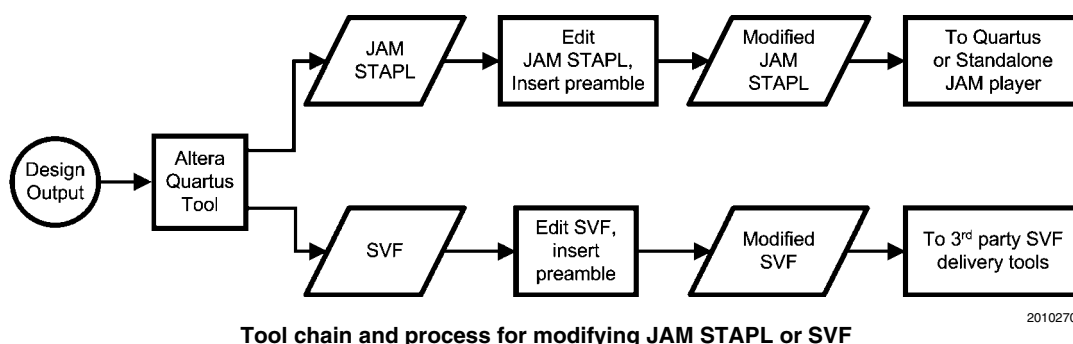
There are three basic ways to get "through" the STA11x devices: Transparent Stitcher Mode, Transparent ScanBridge Mode, and Normal ScanBridge mode.

Transparent Stitcher Mode (STA112 feature only) is activated by way of external pins, and does not require changes to the JAM STAPL or SVF. This mode does require external hardware control. Setting the SB/ \bar{S} pin to 0 selects the Stitcher mode; setting the TRANS pin to 1 puts the device into transparent mode; and the LSP select pins select the appropriate LSPs.

Transparent ScanBridge Mode requires a preamble in the vectors that are used to configure the CPLD. The Quartus tool can provide a JAM STAPL file that may be modified to add the necessary preamble. The JAM STAPL may be played by the Quartus player, or by standalone JAM STAPL players. The Quartus tool can also write out an SVF file that can be "played" later by third party SVF delivery tools. Note that when the STA11x is in transparent mode it is simply buffering the 1149.1 signals. Therefore, it is adding delay, and this may require that the clock speed be lowered.

Examples 1 and 2 below demonstrate preambles to configure the STA11x device into Transparent ScanBridge Mode. Once this is executed, the STA11x device acts as a set of buffers between the backplane side and the LSP side of the device (*i.e.*; Tester TDO → STA11x TDI → STA11x LSP TDO → local chain → STA11x LSP TDI → STA11x TDO → Tester TDI).

Normal ScanBridge Mode also requires a preamble in the vectors used to configure an Altera CPLD. When the STA11x is not in transparent mode, it adds a re-synchronization bit (pad bit) to the end of the chain. This re-times the signals and allows for operation at full clock speed, but requires the addition of the pad bit into the scan path for each LSP inserted in the path. Examples 3 and 4 below demonstrate preambles to configure the STA11x device into normal ScanBridge Mode. Once this is executed, the STA11x acts as a set of buffers between the backplane side and the LSP side of the device, with the addition of the pad bits (*i.e.*; Tester TDO → STA11x TDI → STA11x register → STA11x LSP TDO → local chain → STA11x LSP TDI → pad bit → STA11x TDO → Tester TDI). Note that this requires additional bits in the scan process for the STA11x register and the pad bits.



Example Code from Altera Modified SVF

The following section of code is modified SVF from the Quartus tool output. In this example we have an STA11x device at hex address 0x1B. The target device is located on LSP1. In the example below we have added two lines of code (the highlighted lines) that address the correct device and select the correct local port.

```

!Device #01: XXXX - f:\work\svftest.pof
!NOTE "CHECKSUM" "02CC0FCAE";
TCK frequency: 10MHz
!
TRST ABSENT;
SIR 8 TDI(1B); ! <<<-- level one protocol, STA11x at address 1B hex
SIR 8 TDI(A1); ! <<<-- level two protocol, target device on LSP 1
ENDDR IDLE;
ENDIR IRPAUSE;
STATE IDLE;
SIR 10 TDI (044);
RUNTEST IDLE 10000 TCK ENDSTATE IDLE;
!
!CHECKING SILICON ID
!
SIR 10 TDI (042);
RUNTEST 50 TCK;
SDR 32 TDI (FFFFFFFF) TDO (41393800) MASK (FFFFFFF0);
!
  
```

Example Code for Simulations and Verification

TRANSPARENT SCANBRIDGE MODE

In example 1, we have an STA11x device at address 0x11. The target device is located on LSP0. In example 2, we have an STA11x device at the same address, but the target device is on LSP1.

Example 1: Configuring an LSP of the STA11x in Transparent ScanBridge mode.

```
TRST ON;
TRST OFF;
SIR 8 TDI (11); ! Select STA11x at slot address (11) (level 1 protocol)
SIR 8 TDI (a0); ! Load instruction to enable transparent mode for LSP0 (level 2 protocol)
SIR 8 TDI (a5); ! Verify SIR
SDR 8 TDI (5a); ! Verify SDR
SIR 8 TDI (c3); ! Try to load GOTOWAIT in STA11x
SDR 8 TDI (5a); ! Verify that STA11x did not recognize GOTOWAIT
! Now TDIB→lsp0→TDOB is the scan chain configuration
```

Example 2: Configuring an LSP of the STA11x in Transparent ScanBridge mode.

```
TRST ON;
TRST OFF;
SIR 8 TDI (11); ! Select STA11x at slot address (11) (level 1 protocol)
SIR 8 TDI (a1); ! Load instruction to enable transparent mode for LSP1 (level 2 protocol)
SIR 8 TDI (a5); ! Verify SIR
SDR 8 TDI (5a); ! Verify SDR
SIR 8 TDI (c3); ! Try to load GOTOWAIT in STA11x
SDR 8 TDI (5a); ! Verify that STA11x did not recognize GOTOWAIT
! Now TDIB→lsp1→TDOB is the scan chain configuration
```

NORMAL SCANBRIDGE MODE

In example 3, we have an STA11x device at address 0x01. LSPs 0, 1, and 2 will be connected to the backplane port. In example 4, we have an STA11x device at the same address (0x01), but only LSP0 is connected to the backplane port.

Example 3: Configuring LSP's of the STA11x in "normal" ScanBridge mode.

```
TRST ON;
TRST OFF;
SIR 8 TDI (01); ! Select STA11x at slot address (01)
SIR 8 TDI (8e); ! modesel0 - Setup mode register 0 to select LSP 's
SDR 8 TDI (07); ! Set mode register bits 0,1,2 to select LSP0, LSP1, LSP2 of STA11x
SIR 8 TDI (e7); ! UNPARK to Sync LSPs to backplane port.
! MR0: X000X111
! Now TDIB→register→lsp0→pad→lsp1→pad→lsp2→pad→TDOB is the scan chain configuration
```

Example 4: Configuring LSP's of the STA11x in "normal" ScanBridge mode.

```
TRST ON;
TRST OFF;
SIR 8 TDI (01); ! Select STA11x at slot address (01)
SIR 8 TDI (8e); ! modesel0 - Setup mode register 0 to select LSP's
SDR 8 TDI (01); ! Set mode register bit 0 to select only LSP0 of STA11x
SIR 8 TDI (e7); ! UNPARK to Sync LSPs to backplane port.
! MR0: X000X001
! Now TDIB→register→lsp0→pad→TDOB is the scan chain configuration
```

Revision History

Dec 2009 – Clarification changes only.

Notes

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