CPRI Repeater System

National Semiconductor
Application Note 1821
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1.0 Introduction

This application note implements the Common Public Radio Interface (CPRI) for Remote Radio Heads (RRHs). The designer can use this application note for developing CPRI-based repeater systems in point-to-point or multi-hop configurations. This application note consists of:

- Designs for the CPRI SerDes Repeater Boards for the Radio Equipment (RE) and Radio Equipment Controller (REC) that include CPRI SerDes (SCAN25100) and a clock conditioner (LMK02000 or LMK03000 family). The corresponding schematics describe this design further. Please see Section 3 for more information about the hardware.
- CPRI framer sample code to enable up to four CPRI links. The designer can easily port this IP to popular FPGAs. The corresponding CPRI Framer Design Specification document describes this IP further. Please see Section 4 for more information about the framer IP.

2.0 System Design Overview

Designers can use this application note to implement a repeater design. The overall system can have two possible configurations:

1. **Point-to-Point:** One REC connected to one RE system.
2. **Multi-Hop:** One REC connected to two or more RE systems.

This emulates a multi-hop system by daisy-chaining the REC with a series of RE boards. The data is "looped through" from link 1 to link 2 (and vice versa) inside the FPGA to complete the chain. *Figure 1* illustrates an example of the multi-hop configuration below.

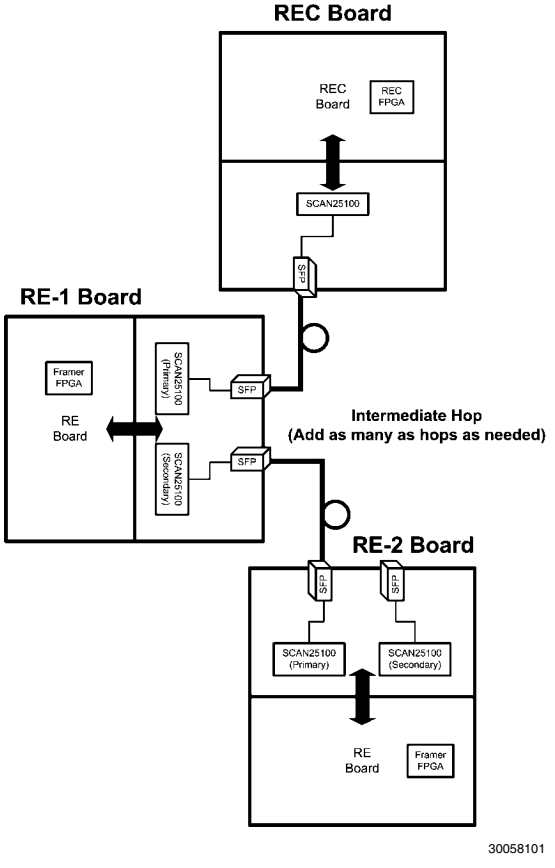

FIGURE 1. Multi-Hop Configuration Example

3.0 CPRI SerDes Repeater Boards (RE and REC) with SCAN25100 SerDes and LMK Clock Conditioners

The repeater boards, which are described in this document, are complete solutions to address the needs of complex repeater designs. The boards feature many parts as optional to enable additional clock outputs, copper connection to SCAN25100, etc. The sections below describe these optional features in further detail. The designer can remove the optional devices, if their functions are deemed unnecessary.

3.1 CPRI SerDes REC BOARD

The REC board interacts with a REC FPGA (*customer-specific*) to process the data and control for a SCAN25100 device. The on-board LMK03001D device cleans the master clock input for distribution. The adjacent RE board sends/receives data to/from the SCAN25100 device via copper or fiber connection.

3.1.1 Features

This board supports multi-hop configuration. It also has selectable High Speed Serial I/O Path via DS25MB100 (optional) for fiber and/or cable connection. The designer can manage the SCAN25100 via FPGA through a MDIO interface. Similarly, the designer can manage the LMK03001D via FPGA through uWire interface. Additional control lines also go to the DS25MB100 (optional) and SFP module.

3.1.2 Devices

Table 1 lists the devices (both required and optional) used in this REC board design.

TABLE 1. REC Board Device List

Device	Quantity	Function	Required/Optional
SCAN25100	2	CPRI SerDes	Required
LMK03001D	1	Clock conditioner for clock distribution and jitter cleaning	Required
LM2852XMXA-1.8	1	Voltage regulator	Required
SFP module	1	To enable fiber connection	Required
DS25MB100	1	Line interface MUX (enables either fiber or copper connection from the same board)	Optional
SMA Headers	As Needed	Used as high-speed test ports. Designer can replace these with a cable connector for a copper cable connection	Optional
DS90LT012A	1	LVCMOS translator, for more LVCMOS clock outputs	Optional

3.1.3 Block Diagram

Figure 2 below illustrates a block diagram of the major components of the REC board along with the data flow on the repeater board. *Note: The diagram shows the DS25MB100 as optional. The designer can install this to switch between fiber and copper connectors. If this option is not needed, the designer can route the SCAN25100 I/O directly to the desired connectors. The designer can install the DS90LT012A to convert any of the LVDS outputs of the LMK03001D to LVCMOS, if desired.*

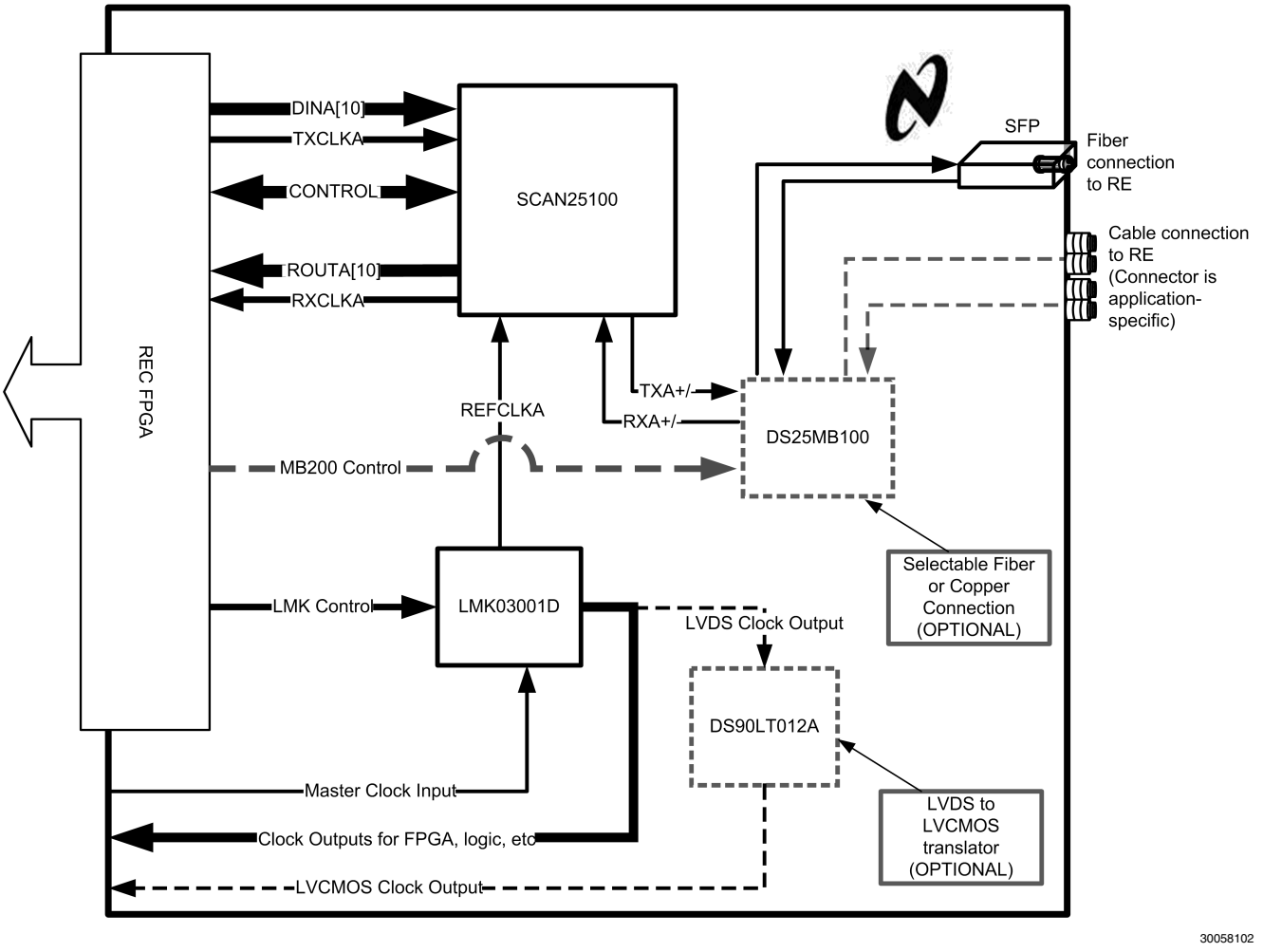

FIGURE 2. REC Board

3.2 CPRI SerDes RE BOARD

The RE board interacts with a CPRI framer FPGA (*customer-specific*) to process the data and control for two SCAN25100 devices. The on-board LMK02000 device cleans the recovered clock for distribution. The adjacent RE and REC boards send/receive data to/from the SCAN25100 device via copper or fiber connections.

3.2.1 Features

This board supports multi-hop configuration. It also has a selectable High Speed Serial I/O Path via DS25MB200 (optional) for fiber and/or cable connection. The designer can manage the SCAN25100 via FPGA through a MDIO interface. Similarly, the designer can manage the LMK02000 and LMK01000 (optional) via FPGA through uWire interface. Additional control lines are onboard for DS10CP154, DS25MB200 (optional), LMX2531 (optional), and SFP module.

3.2.2 Devices

Table 2 below lists the devices (both required and optional) used in this RE board design.

TABLE 2. RE Board Device List

Device	Quantity	Function	Required / Optional
SCAN25100	2	CPRI SerDes	Required
LMK02000	1	Clock conditioner for clock distribution and jitter cleaning	Required
DS10CP154	1	Reference clock distribution	Required
LM2852XMXA-1.8	1	Voltage requlator	Required
SFP module	2	To enable fiber connection	Required
Oscillator	1	30.72 MHz, for start up clock	Required
DS25MB200	1	Line interface MUX (enables either fiber or copper connection from the same board)	Optional
SMA Headers	As needed	Used as high-speed test ports. Designer can replace these with a cable connector for a copper cable connection	Optional
DS90LT012A	1	LVCMOS translator, for more LVCMOS clock outputs	Optional
LMK01000	1	Clock conditioner for clock distribution, providing additional clock outputs	Optional
LMX2531	1	High Performance Frequency Synthesizer, to drive a mixer	Optional
LP38501TS-ADJ	1	LDO for 3 V supply for LMX2531	Optional

3.2.3 Clocking

3.2.3.1 Pre-LOCK Sequence

Figure 3 illustrates the Pre-LOCK clocking sequence below. The on-board oscillator (1) provides a 30.72 MHz clock upon power up. The designer must hardwire the DS10CP154 to route the oscillator output to Start-Up Clock output (2), which goes to the FPGA. Therefore, the Start-Up Clock is the 30.72 MHz local clock provided by the on-board oscillator. The FPGA uses the Start-Up Clock to configure (3) the LMK02000 and LMK01000 (optional). The designer must also hardwire the DS10CP154 to route LMK output (4) to REFCLKA (5) and REFCLKB (6) of the SCAN25100 devices. The SCAN25100 uses this clock to lock onto the incoming data.

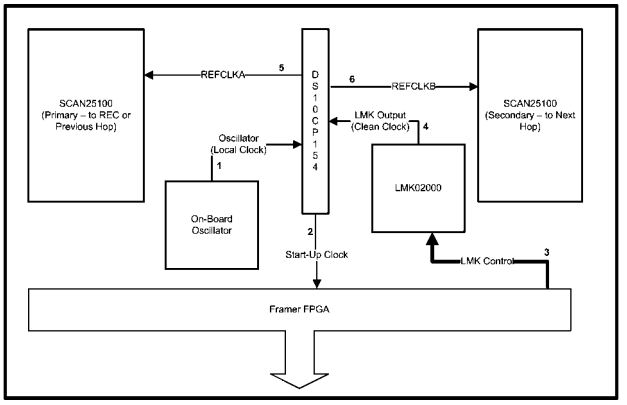

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FIGURE 3. Pre-LOCK Sequence

3.2.3.2 Post-LOCK Sequence

Figure 4 illustrates the Post-LOCK clocking sequence below. Once the SCAN25100 locks to the recovered clock (indicated by the falling edge of LOCK signal), the FPGA then (1) configures the DS10CP154 (2) to route the SYSCLKA, instead of the oscillator, (3) through the LMK02000 for jitter cleaning and (4) back through the DS10CP154, which will distribute this recovered clock as the (5) REFCLKA and (6) REFCLKB to the SCAN25100 devices. Once the DS10CP154 is configured, the FPGA will have completed the initialization of the system. Then, the system begins normal operating conditions.

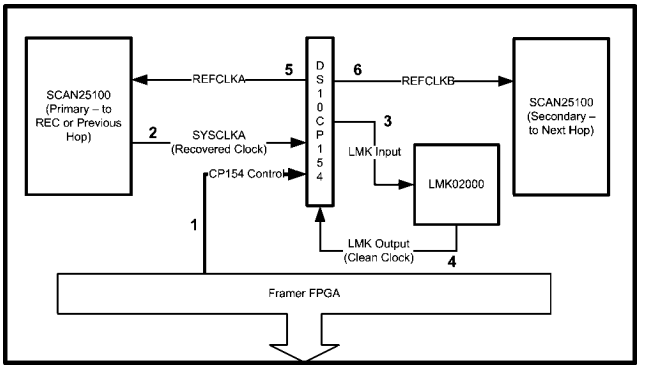

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FIGURE 4. Post-LOCK Sequence

3.2.3.3 Normal Clocking Conditions

Figure 5 illustrates the clocking of this design under normal operating conditions. The DS10CP154 routes SYSCLKA, the recovered clock from the primary SCAN25100, to the LMK02000 to be cleaned. The LMK02000 cleans the clock. Then, the LMK02000 sends one copy to the FPGA and another copy back to the DS10CP154. The DS10CP154 routes the LMK clean clock to REFCLKA, which is the REFCLK input of the primary SCAN25100. Also, the DS10CP154 sends another copy of the LMK clean clock to REFCLKB, which is the REFCLK input of the secondary SCAN25100. The designer can route the remaining outputs of the LMK02000 to the optional devices listed in section, 3.2.2, as shown in the block diagram in following section, 3.2.4.

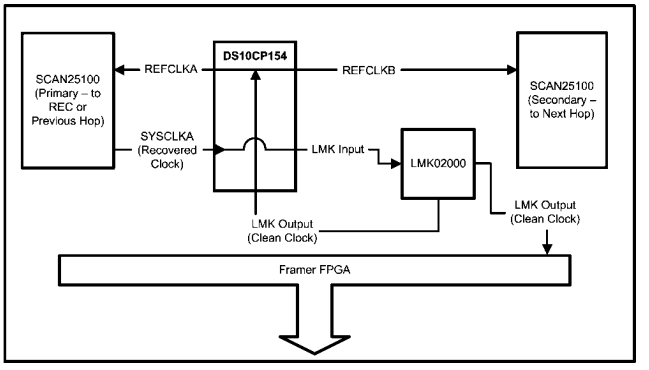

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FIGURE 5. Normal Operating Conditions

3.2.4 Block Diagram

Figure 6 illustrates a block diagram of the major components of the RE board along with the data flow on the repeater board.

Note: The diagram below shows the DS25MB200 as optional. The designer can install this to switch between fiber and copper connectors. If this option is not needed, the designer can route the SCAN25100 I/O directly to the desired connectors. The designer can install the DS90LT012A to convert any of the LVDS outputs of the LMK02000 to LVCMOS, if desired. The designer can add the LMK01000 for additional clock outputs, if necessary. The designer can add the LMX2351 to drive a mixer, if needed.

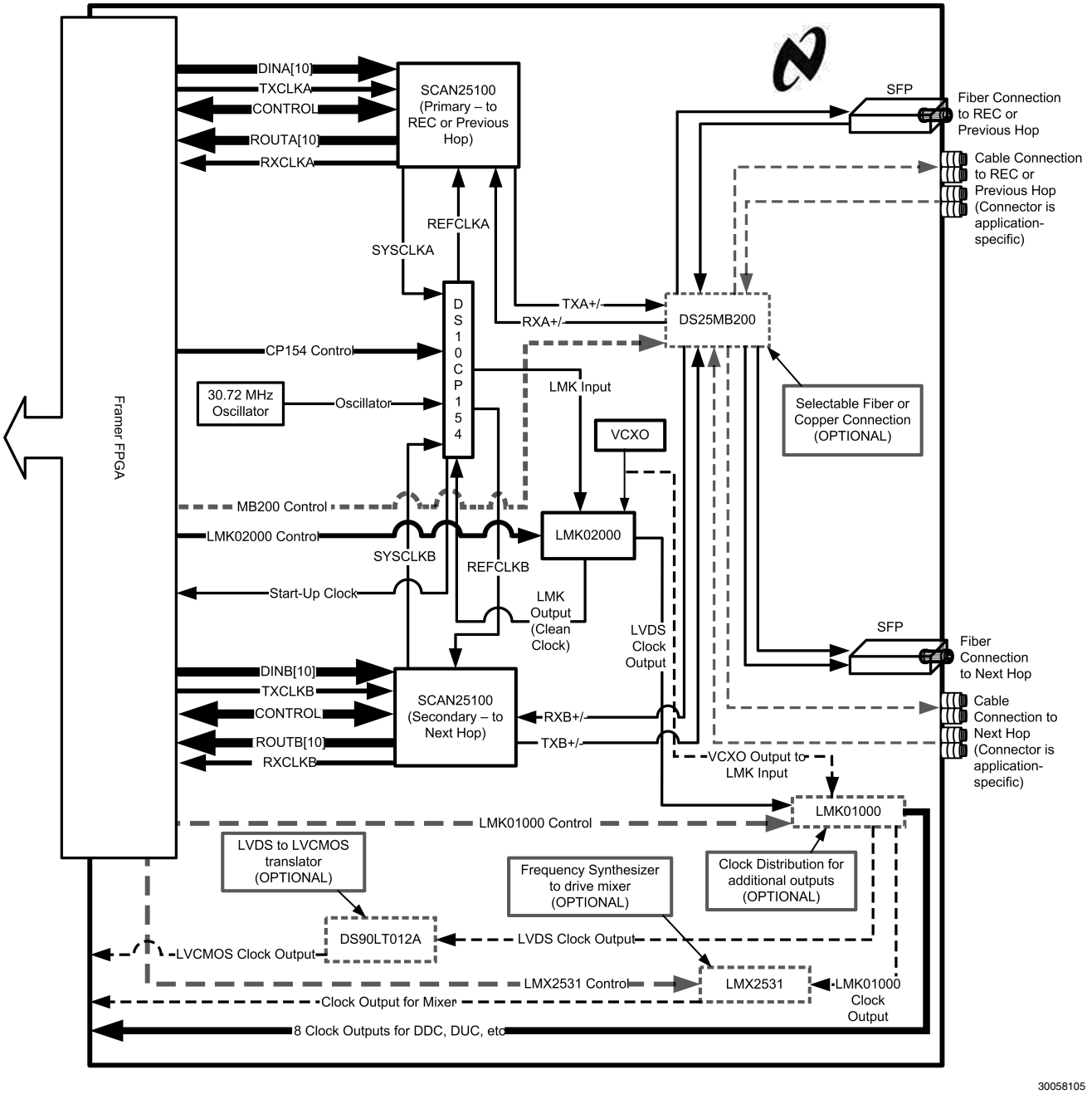


FIGURE 6. RE Board

3.3 HARDWARE

The following tables and figures refer to the hardware design notes, requirements, and specifications of both the RE and REC boards.

3.3.1 PLL Loop Filter

This design includes PLL loops filters for the LMK devices as shown in the schematics for both the RE and REC boards. These loop filters serve as filters between the charge pump and Voltage Controlled Crystal Oscillator (VCXO) to convert the correction pulses from the charge pump to voltages that steer the VCXO accordingly. Some components of these filters are external to the LMK devices so that designers can customize the filter designs for their specific applications and according to the VCXO chosen. The design parameters for the particular loop filter in this design for the LMK03001D is listed below in *Table 3*.

TABLE 3. PLL Loop Filter Design Parameters

Phase Margin	78.08°	**K_φ**	400 µA
Loop Bandwidth	3.68 kHz	**F_{comp}**	15.36 MHz
Crystal Frequency	30.72 MHz	**Output Frequency**	1474.56 MHz
Supply Voltage	3.3 Volts	**VCO Gain**	10 MHz/Volt

The LMK02000 uses a narrow 10 Hz loop bandwidth. Similar to the filter used with the LMK03001D, the design parameters for this loop filter will vary with the VCXO selected.

Details on how to design and customize these filters can be found in Chapter 3 of the Clock Conditioner Owner's Manual (Note 1). The particular loop filter design used for the REC is detailed in the AN-1734 application (Note 2). The designer can also use National Semiconductor's Clock Design Tool for design and simulation of customized PLL loop filters (Note 3).

3.3.2 LMK Device Setup

The LMK02000 on the RE board uses an external VCXO. The designer should set the VCXO frequency to a multiple of 30.72 MHz and in accordance to how the designer programs the corresponding clock conditioner. For more details on the setup of the LMK02000, please view the evaluation board operating instructions (Note 4). No external VCXO is needed for the LMK03001D. For more information on the usage of the LMK03000 family with the SCAN25100, please refer to Application Note AN-1734 (Note 2).

Note 1: http://www.national.com/appinfo/interface/files/clk_conditioner_owners_manual.pdf

Note 2: http://www.national.com/an/AN/AN-1734.pdf

Note 3: http://www.national.com/timing

Note 4: http://www.national.com/appinfo/interface/files/LMK02000EVAL-1.pdf

3.3.3 Phase Noise of LMK Devices

Figure 7 and *Figure 8* are phase noise plots of the LMK devices when used with the SCAN25100.

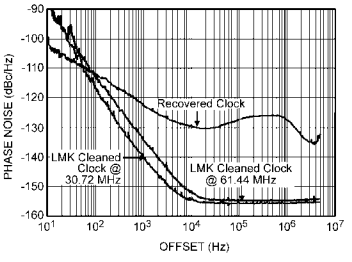


FIGURE 7. LMK02000 Phase Noise Plot

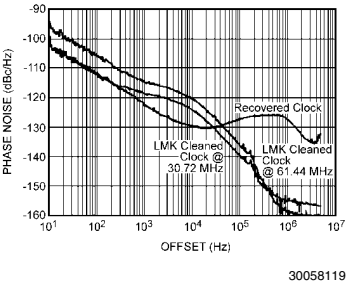


FIGURE 8. LMK03001D Phase Noise Plot

3.3.4 DS10CP154 Crosspoint Switch I/O for RE Board

Figure 9 and *Table 4* below describe the signaling of the DS10CP154 crosspoint switch.

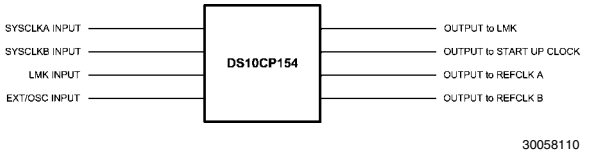


FIGURE 9. DS10CP154 I/O

TABLE 4. Crosspoint Switch Connections

Pins	Position	Input	Output
S31/S30	00	Recovered SYSCLKA	SCAN25100B REFCLK
	01	Recovered SYSCLKB	
	10	Cleaned Input from LMK	
	11	Ext CLK/OSC	
S21/S20	00	Recovered SYSCLKA	SCAN25100A REFCLK
	01	Recovered SYSCLKB	
	10	Cleaned Input from LMK	
	11	Ext CLK/OSC	
S11/S10	00	Recovered SYSCLKA	FPGA Start Up Clock
	01	Recovered SYSCLKB	
	10	Cleaned Input from LMK	
	11	Ext CLK/OSC	
S01/S00	00	Recovered SYSCLKA	LMK Input Clock
	01	Recovered SYSCLKB	
	10	Cleaned Input from LMK	
	11	Ext CLK/OSC	

3.3.5 External Clock Source Input

Figure 10 below shows the typical passive mux layout for the RE board. The designer is recommended to populate C46 and C47 (leave C44 and C45 pads open) for on-board oscillator input to crosspoint. To use the external clock source via SMA connectors, populate C44 and C45, leaving C46 and C47 open. This arrangement allows an external clock source to be muxed into the system for testing.

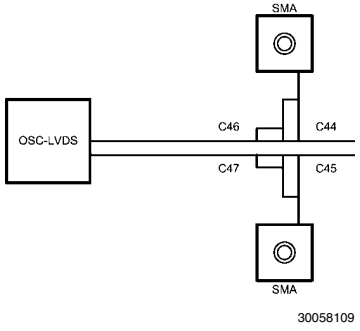


FIGURE 10. External Clock Source/On-board Oscillator Mux Layout

3.3.6 Power Supply Specifications for Major On-Board Devices

Table 5 and *Table 6* below describe the power consumption of the major components on this board.

TABLE 5. Power Specifications for RE Board

Component	Supply Connection	Power Consumption
SCAN25100	3.3 V / 1.8 V	1.2 W
DS10CP154	3.3 V	0.45 W
DS25MB200	3.3 V	1 W
SFP	3.3 V	1 W
LMK02000	3.3 V	0.5 W
LMK01000	3.3 V	0.7 W
LMX2351	3.0 V	0.15 W

TABLE 6. Power Specifications for REC Board

Component	Supply Connection	Power Consumption
SCAN25100	3.3 V / 1.8 V	1.2 W
DS25MB100	3.3 V	0.45 W
SFP	3.3 V	1 W
LMK03001D	3.3 V	0.55 W

4.0 CPRI Framer/Deframer FPGA IP

The CPRI framer module implements the layer-2 subsystem of the CPRI 2.0 specification for interconnecting RE and REC systems. This IP module multiplexes I/Q data with synchronization and timing information to generate CPRI hyperframes. National Semiconductor (NSC) has verified the functionality of this module on an Altera Stratix FPGA (simulation only). NSC developed this sample IP in Verilog HDL and organized it for easy porting to other popular FPGA models. The following section describes the features implemented in this sample IP.

The IP provides CPRI framing and deframing engine, according to CPRI spec v2.0. Please see *CPRI Framer Design Specification* document for more detail. The framing/deframing engines support up to four CPRI links each of which the designer can configured to act as a Master or a Slave port, as shown in *Figure 11* and *Figure 12*.

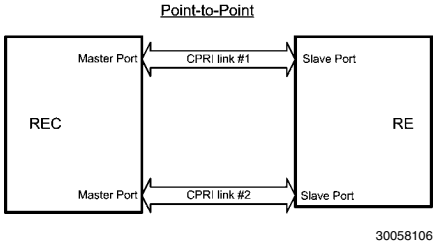


FIGURE 11. Point-to-Point Configuration (shown with 2 CPRI links between nodes)

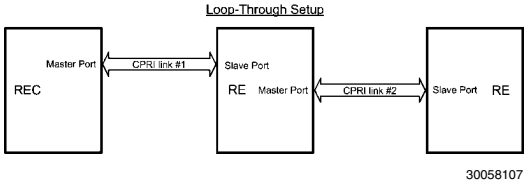


FIGURE 12. Loop-Through Setup (shown with 1 CPRI link between nodes)

The FPGA IP also supports insertion and extraction of the following sub-channel data, as shown in *Table 7* below:

TABLE 7. Sub-Channel Data

Sub-Channel	Control Words Source and Target
L1 inband protocol	Internally generated and validated by FPGA
Synchronization	Internally generated and validated by FPGA
Vendor specific data	External interface either MII or SPI
Fast (Ethernet) based C&M	External MII interface
Slow (HDLC) based C&M	External SPI interface

The IP features automatic start-up and rate negotiation per CPRI 2.0 specification and double rate TBI interface to connect to SCAN25100 devices. It supports 8-bit wide I/Q samples in complex format (total 16-bits). The interface code to the DDC/DUC is a standalone module that the designer can easily configure to suit the output/input requirements of a 3rd party component. It internally configures the SCAN25100 (SerDes) devices for required operational modes using the MDIO master mode. All data source blocks (IQ, Slow C&M, Fast C&M, and Vendor specific) interface to the framing engine via memory map or FIFO type interface with independent clock and strobe signals. It also supports configurable SOF (Start of hyperframe, different from K28.5) byte for custom CPRI implementations. The LCV (Line Code Violations) as reported by the SCAN25100 (SerDes) device are noted and reported in a control register. The sample HDL code is provided in Verilog and simulated on an Altera Stratix FPGA. It supports loop-through multi-hop mode; however, the future version of this IP will implement a more complete multi-hop mode based on node addressing.

5.0 Schematics and Bill Of Materials

The following sections contain the schematics and bill of materials (BOM) for the RE and REC boards.

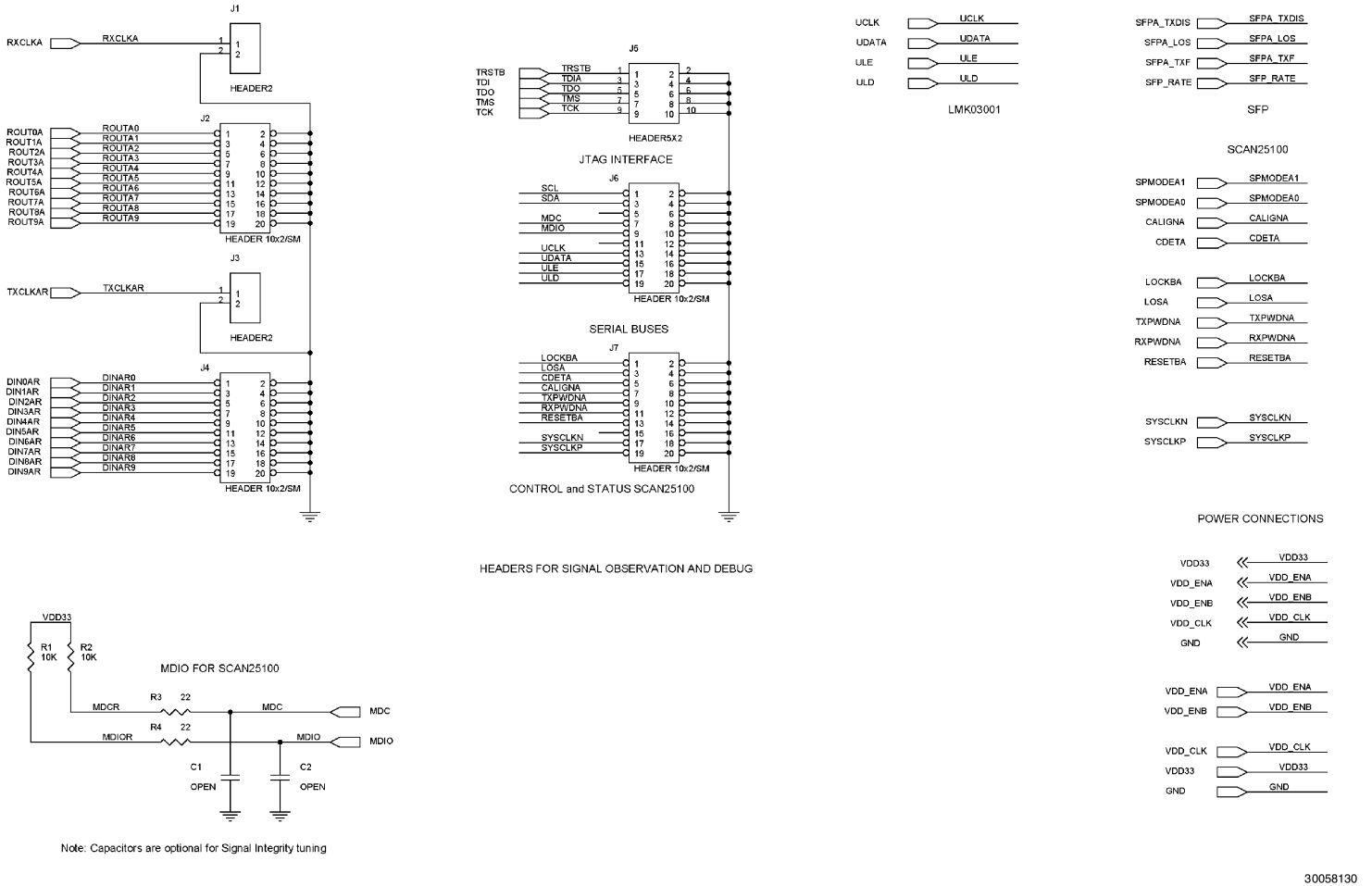


FIGURE 13. REC Schematic Page 1

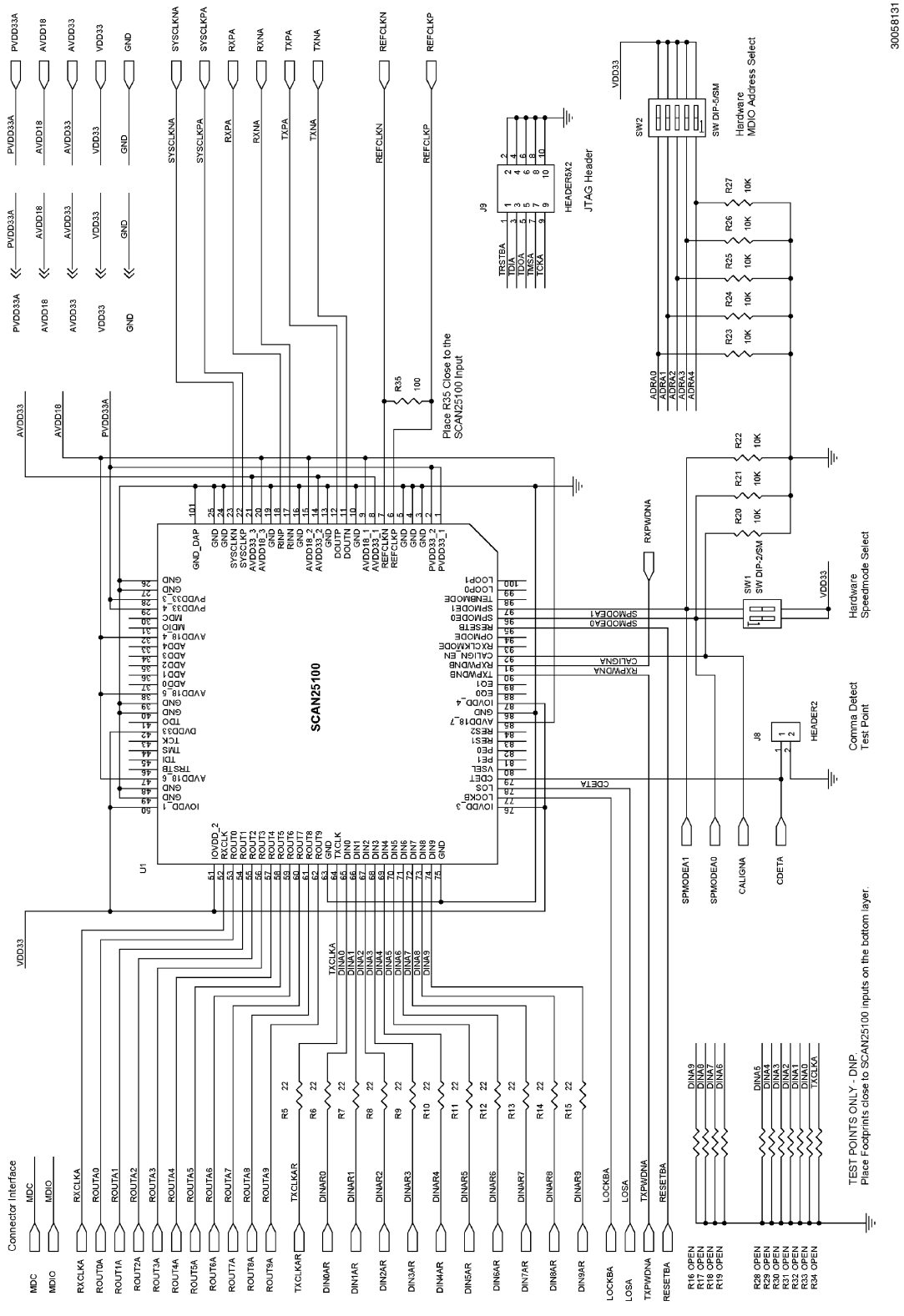


FIGURE 14. REC Schematic Page 2

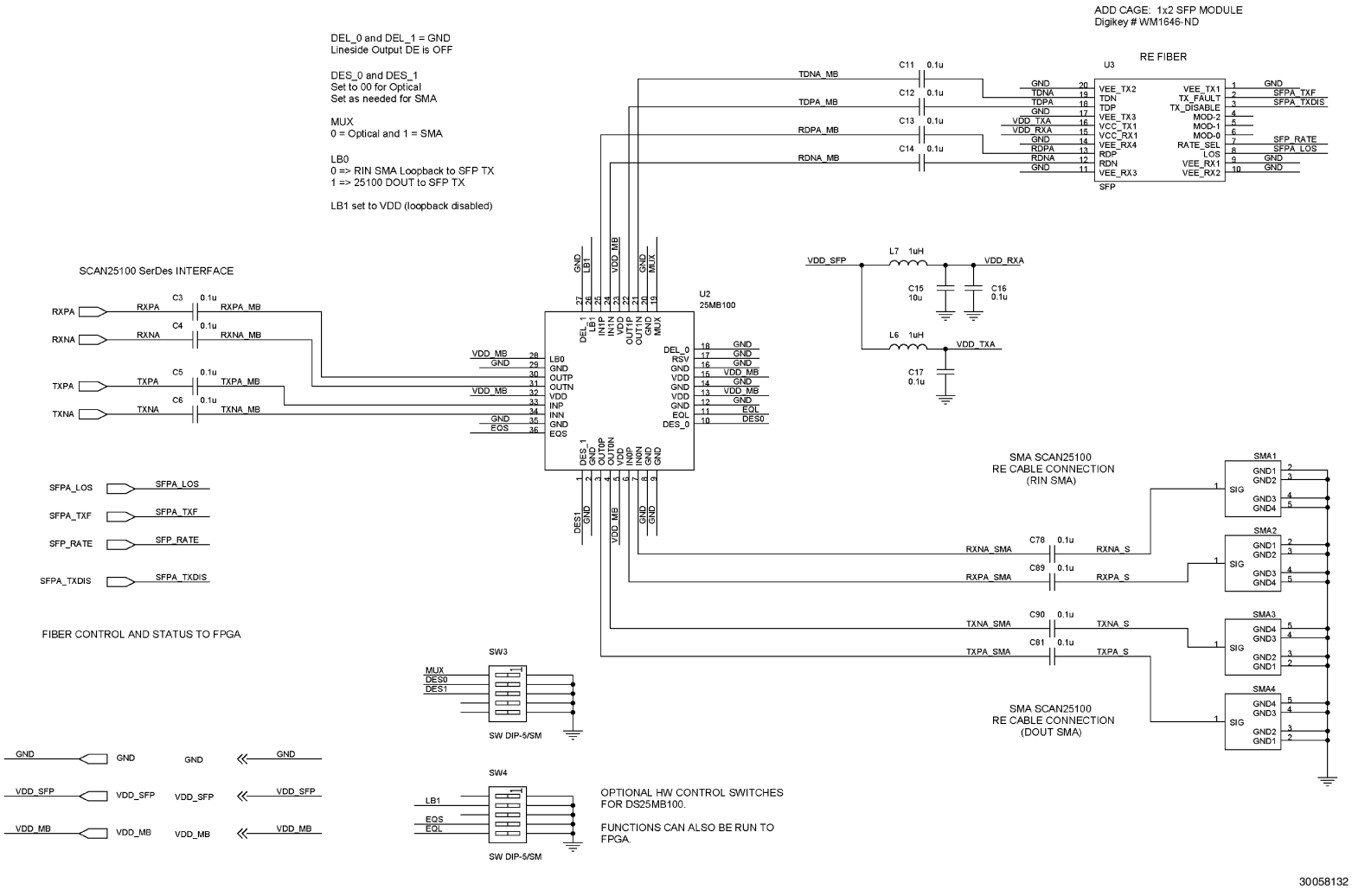


FIGURE 15. REC Schematic Page 3

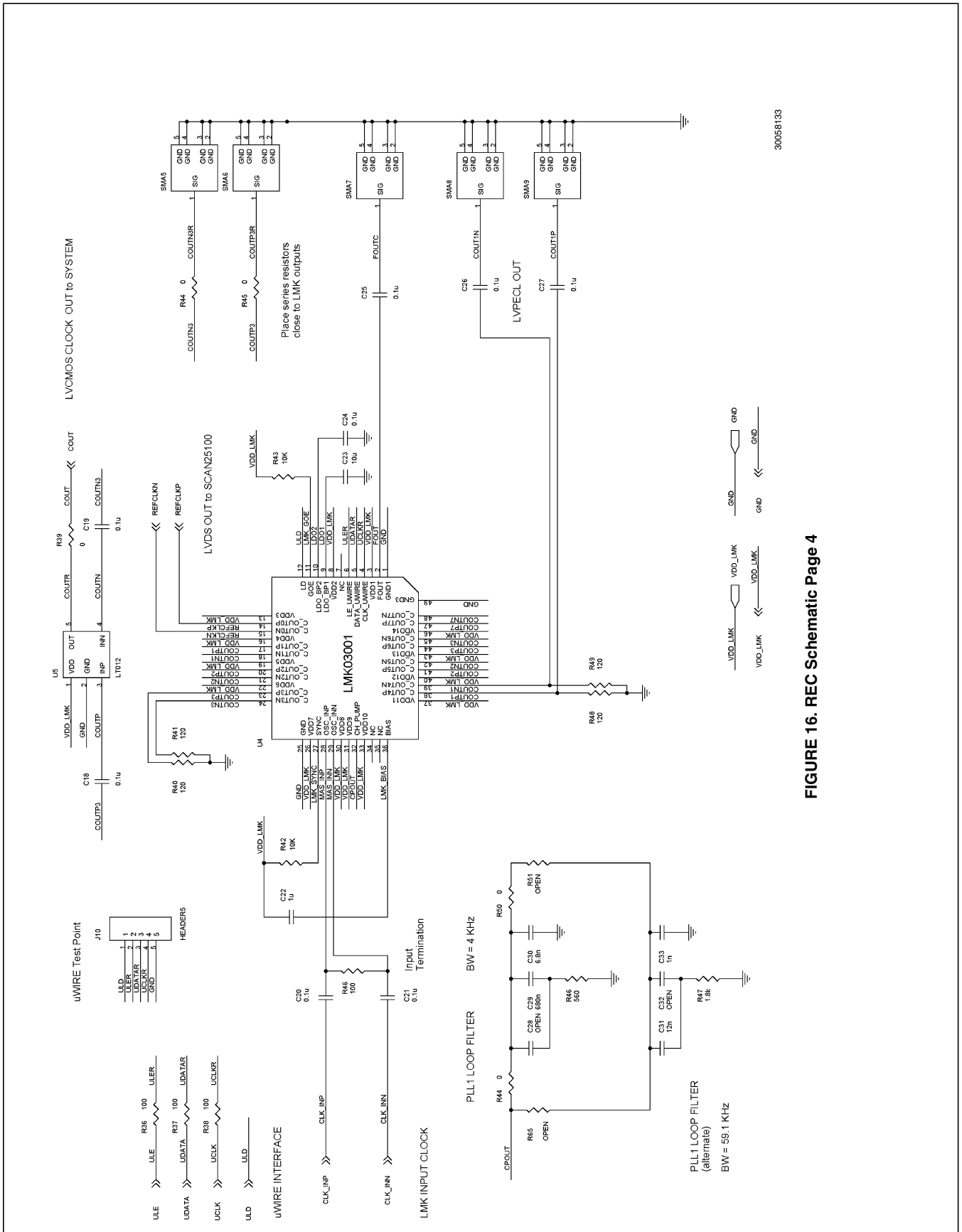
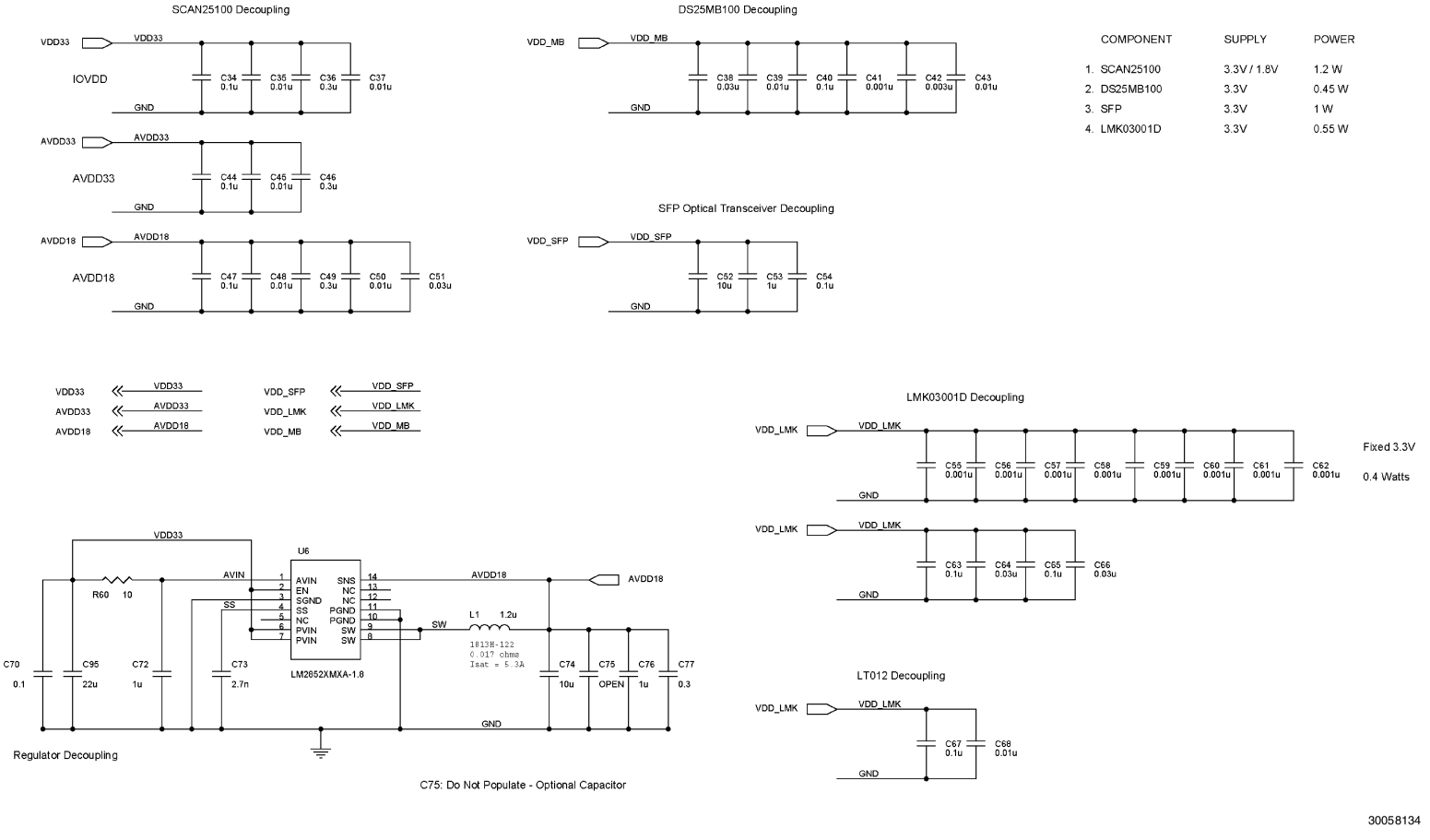


FIGURE 16. REC Schematic Page 4



	COMPONENT	SUPPLY	POWER
1.	SCAN25100	3.3V / 1.8V	1.2 W
2.	DS25MB100	3.3V	0.45 W
3.	SFP	3.3V	1 W
4.	LMK03001D	3.3V	0.55 W

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FIGURE 17. REC Schematic Page 5

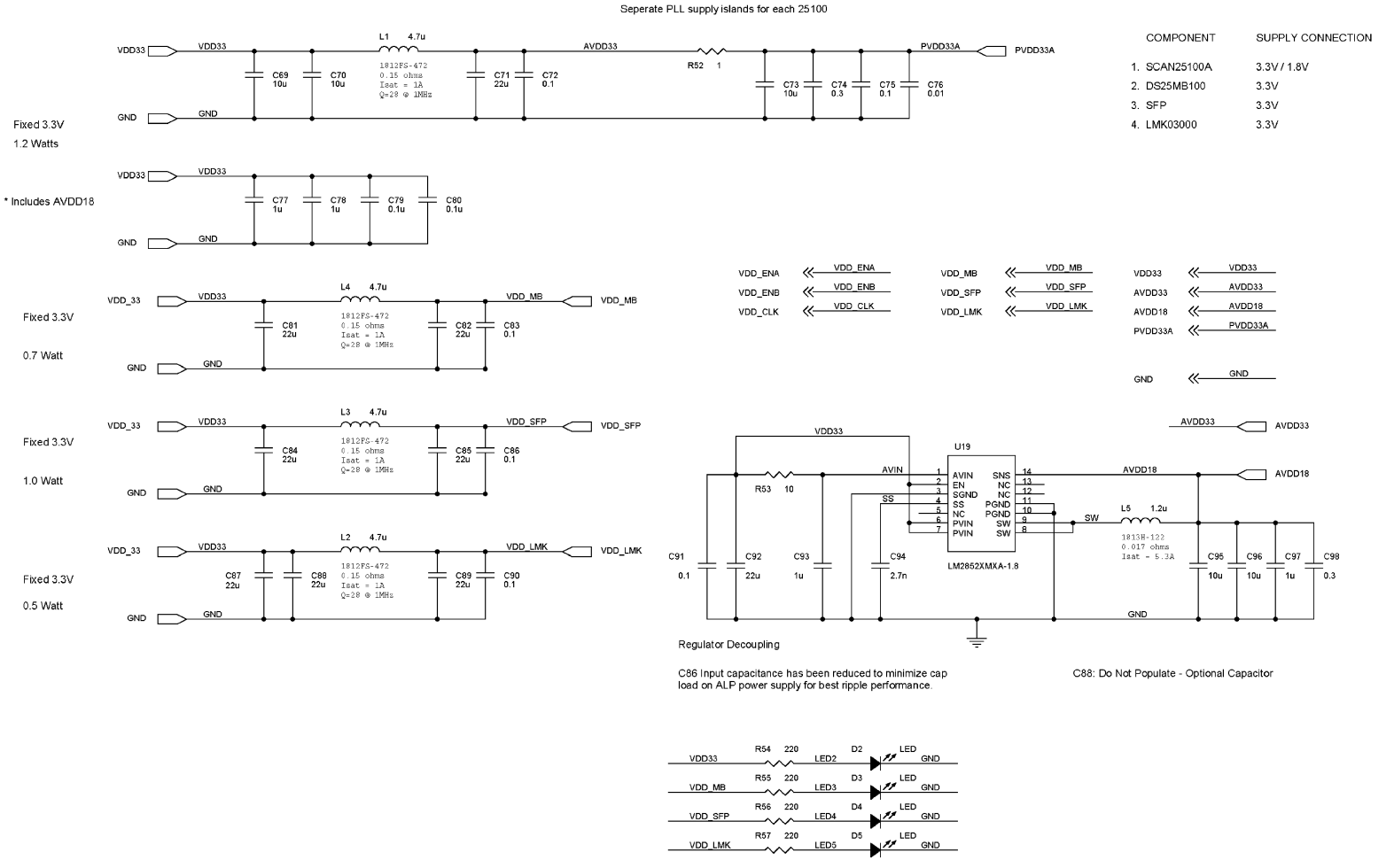

FIGURE 18. REC Schematic Page 6

5.2 REC BILL OF MATERIALS

TABLE 8. REC BOM

Item	Quantity	Reference	Part
1	18	C1, C2, R16, R17, R18, R19, R28, C28, R29, R30, R31, R32, C32, R33, R34, R51, R65, C75	OPEN
2	32	C3, C4, C5, C6, C11, C12, C13, C14, C16, C17, C18, C19, C20, C21, C24, C25, C26, C27, C34, C40, C44, C47, C54, C63, C65, C67, C78, C79, C80, C81, C89, C90	0.1 u
3	9	C15, C23, C52, C69, C70, C73, C74, C95, C96	10 u
4	8	C22, C53, C72, C76, C77, C78, C93, C97	1 u
5	1	C29	680 n
6	1	C30	6.8 n
7	1	C31	12 n
8	1	C33	1 n
9	8	C35, C37, C39, C43, C45, C48, C50, C68	0.01 u
10	3	C36, C46, C49	0.3 u
11	4	C38,C51,C64,C66	0.03 u
12	9	C41, C55, C56, C57, C58, C59, C60, C61, C62	0.001 u
13	1	C42	0.003 u
14	7	C70, C72, C75, C83, C86, C90, C91	0.1
15	10	C71, C81, C82, C84, C85, C87, C88, C89, C92, C95	22 u
16	2	C73, C94	2.7 n
17	3	C74, C77, C98	0.3
18	1	C76	0.01
19	4	D2, D3, D4, D5	LED
20	3	J1, J3, J8	HEADER2
21	4	J2, J4, J6, J7	HEADER 10x2 / SM
22	2	J5, J9	HEADER 5x2
23	1	J10	HEADER5
24	4	L1, L2, L3, L4	4.7 u
25	2	L1, L5	1.2 u
26	2	L6, L7	1 uH
27	12	R1, R2, R20, R21, R22, R23, R24, R25, R26, R27, R42, R43	10 K
28	13	R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15	22
29	5	R35, R36, R37, R38, R46	100
30	4	R39, R44, R45, R50	0
31	4	R40, R41, R48, R49	120
32	1	R46	560
33	1	R47	1.8 k
34	1	R52	1

Item	Quantity	Reference	Part
35	2	R53, R60	10
36	4	R54, R55, R56, R57	220
37	9	SMA1, SMA2, SMA3, SMA4, SMA5, SMA6, SMA7, SMA8, SMA9	SMAedge
38	1	SW1	SW DIP-2/SM
39	3	SW2, SW3, SW4	SW DIP-5/SM
40	1	U1	SCAN25100
41	1	U2	DS25MB100
42	1	U3	SFP
43	1	U4	LMK03001
44	1	U5	LT012
45	2	U6, U19	LM2852XMXA-1.8

5.3 RE SCHEMATICS

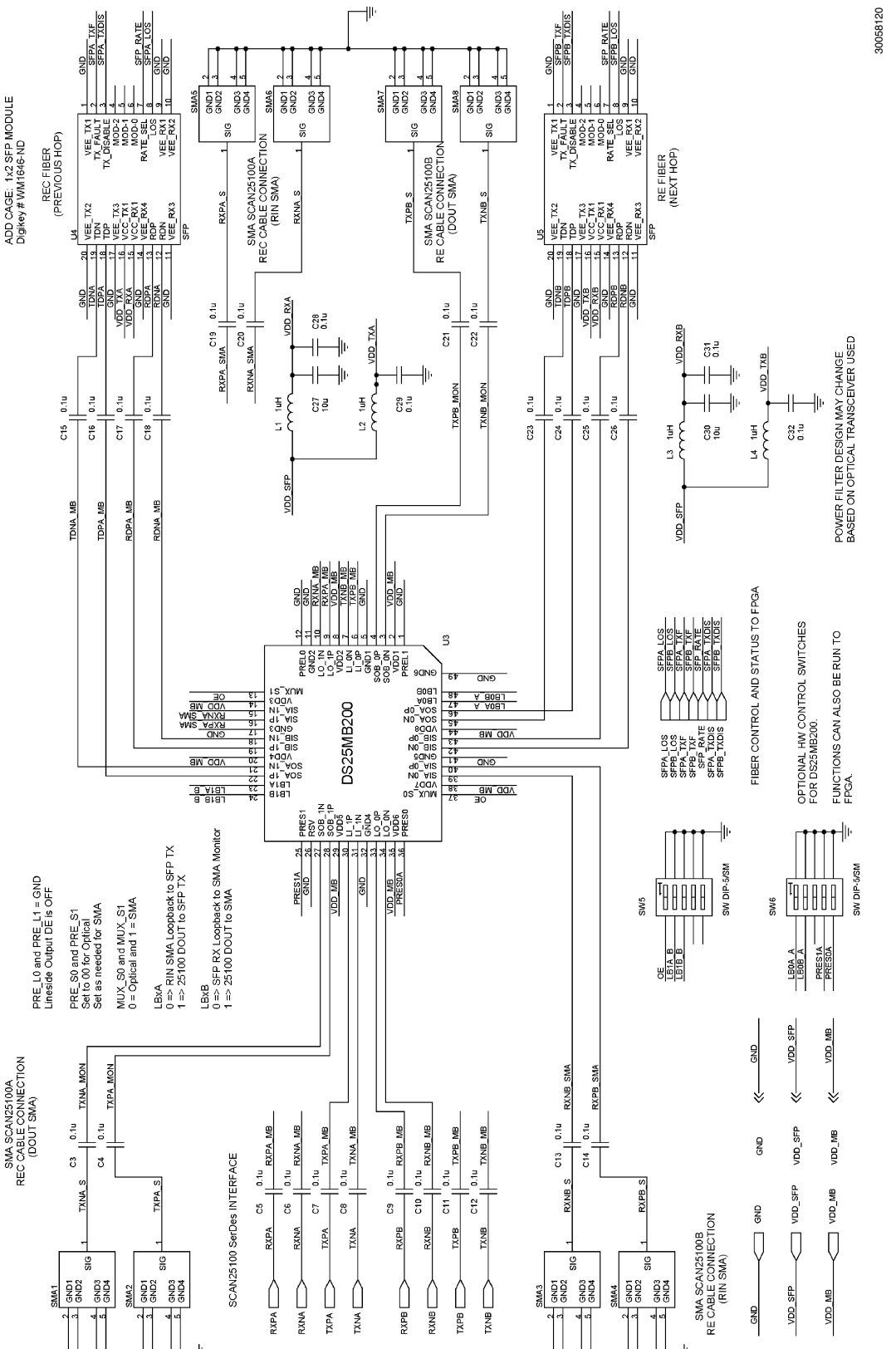

FIGURE 19. RE Schematic Page 1

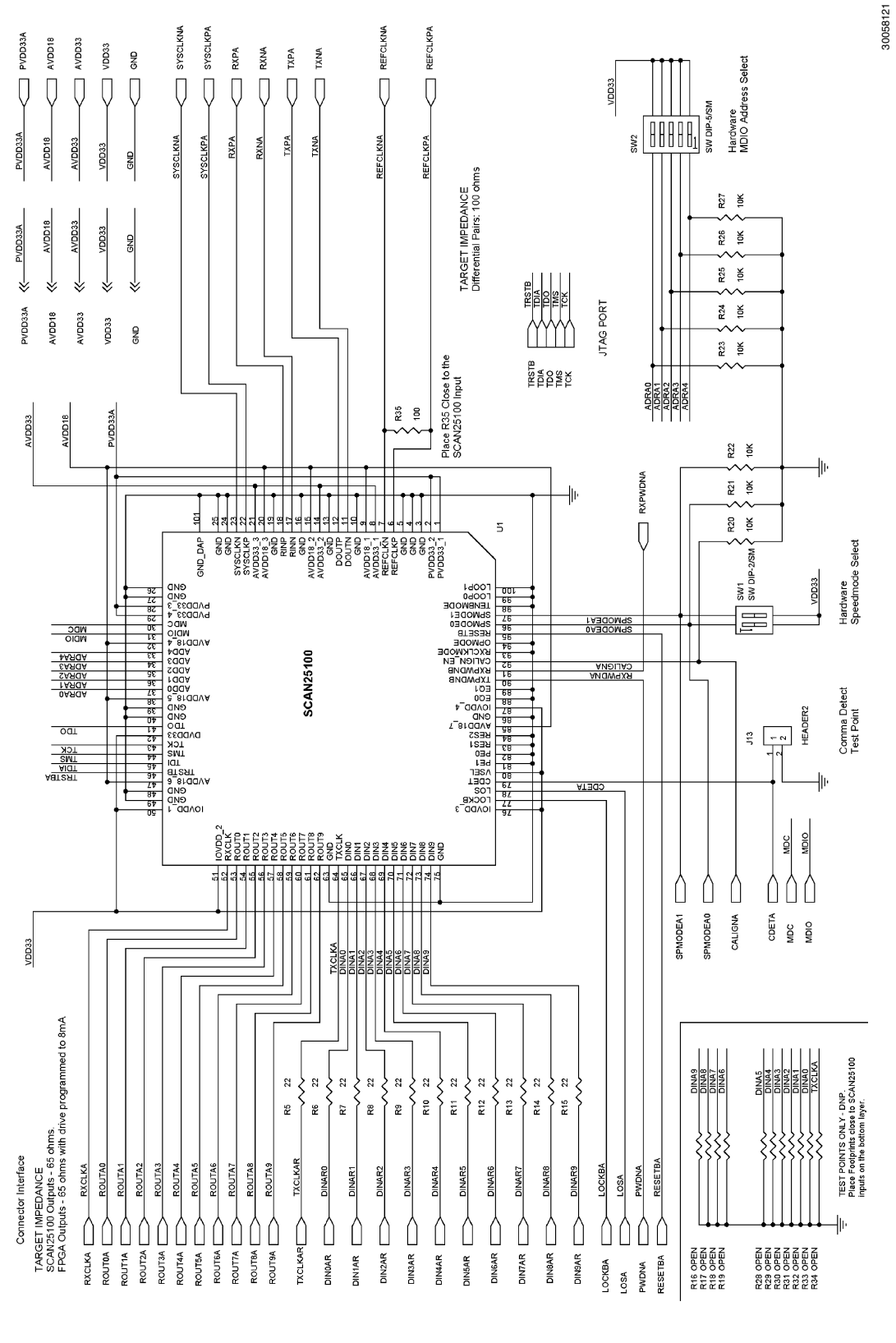

FIGURE 20. RE Schematic Page 2

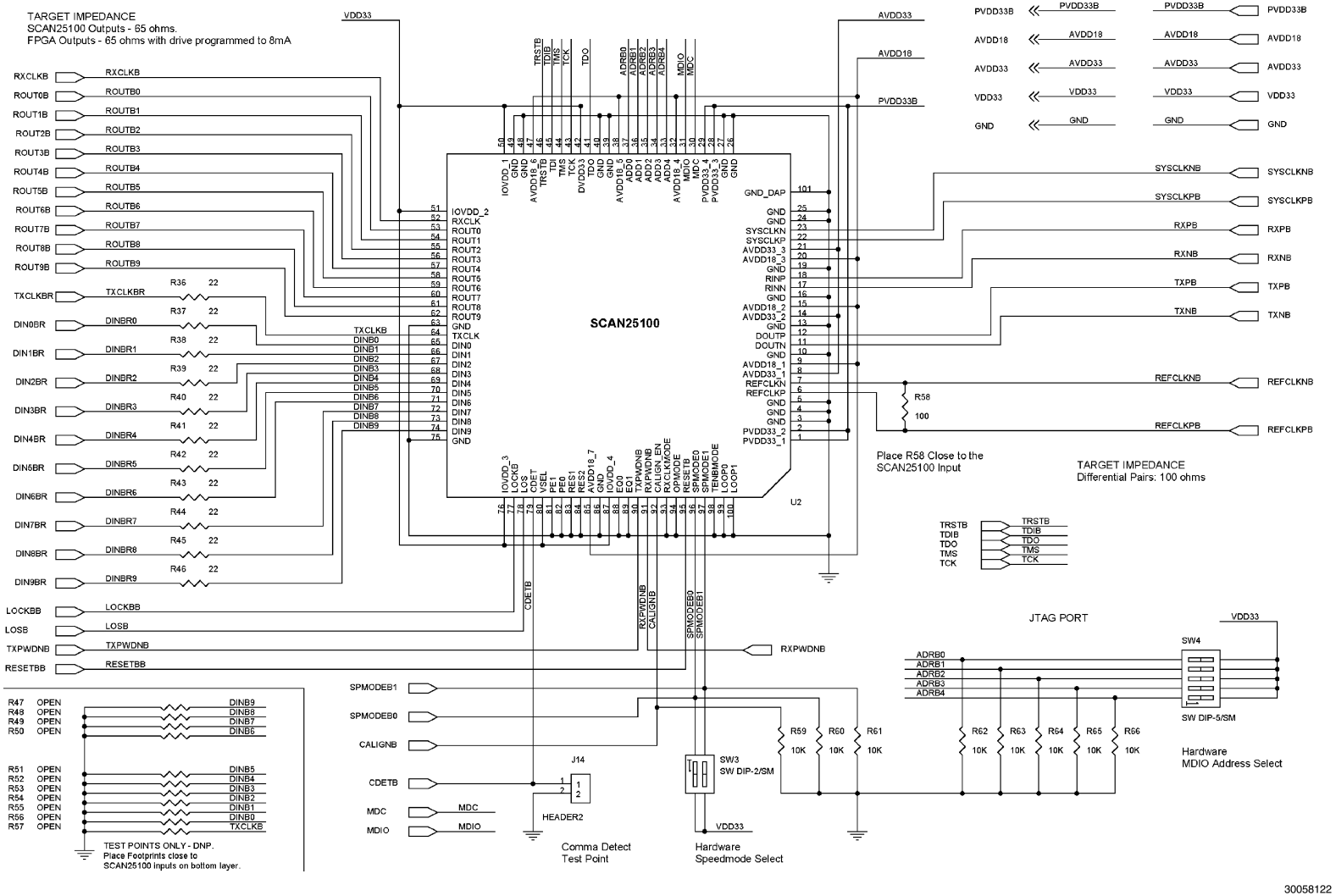

FIGURE 21. RE Schematic Page 3

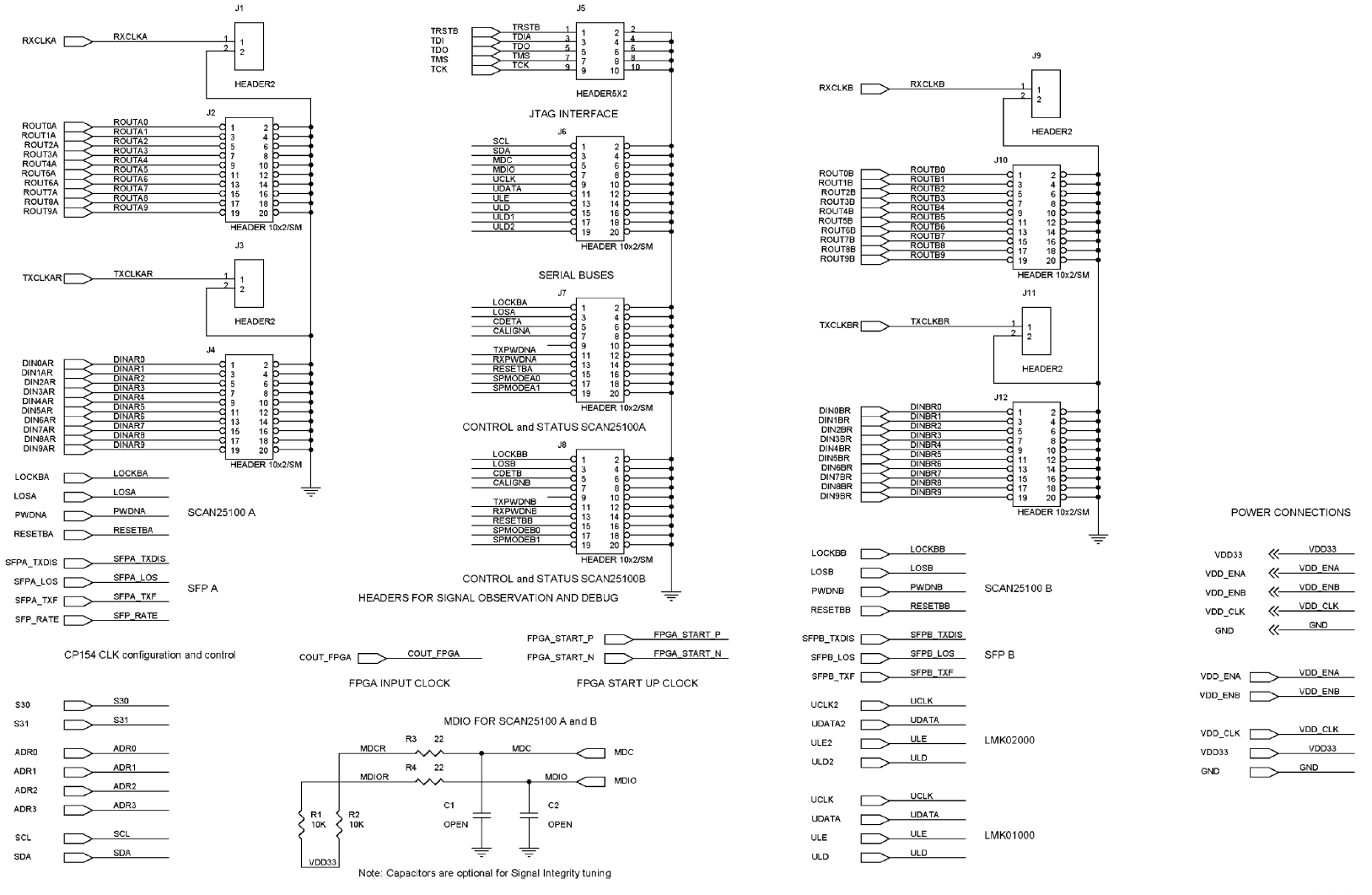

FIGURE 22. RE Schematic Page 4

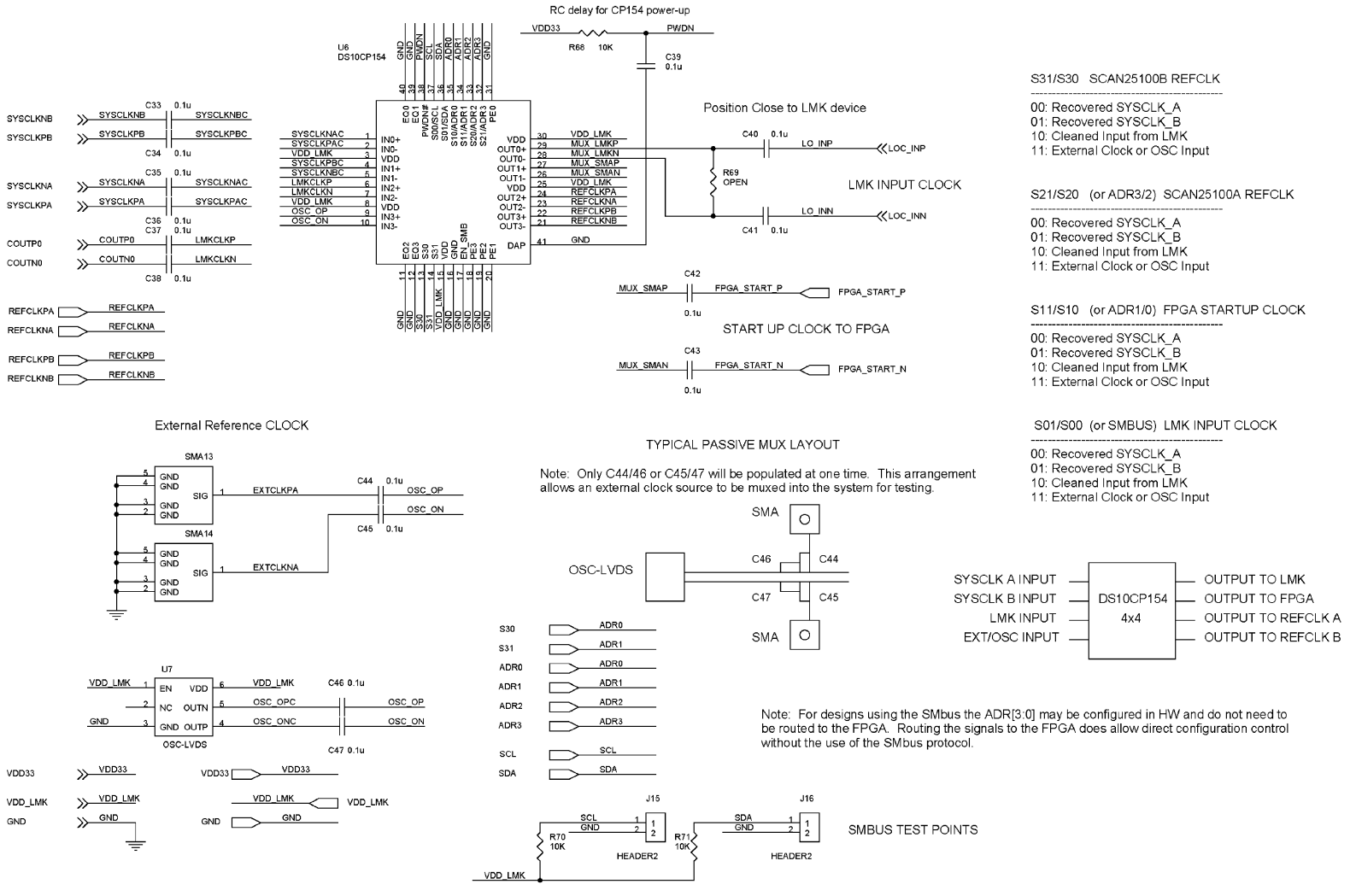

FIGURE 23. RE Schematic Page 5

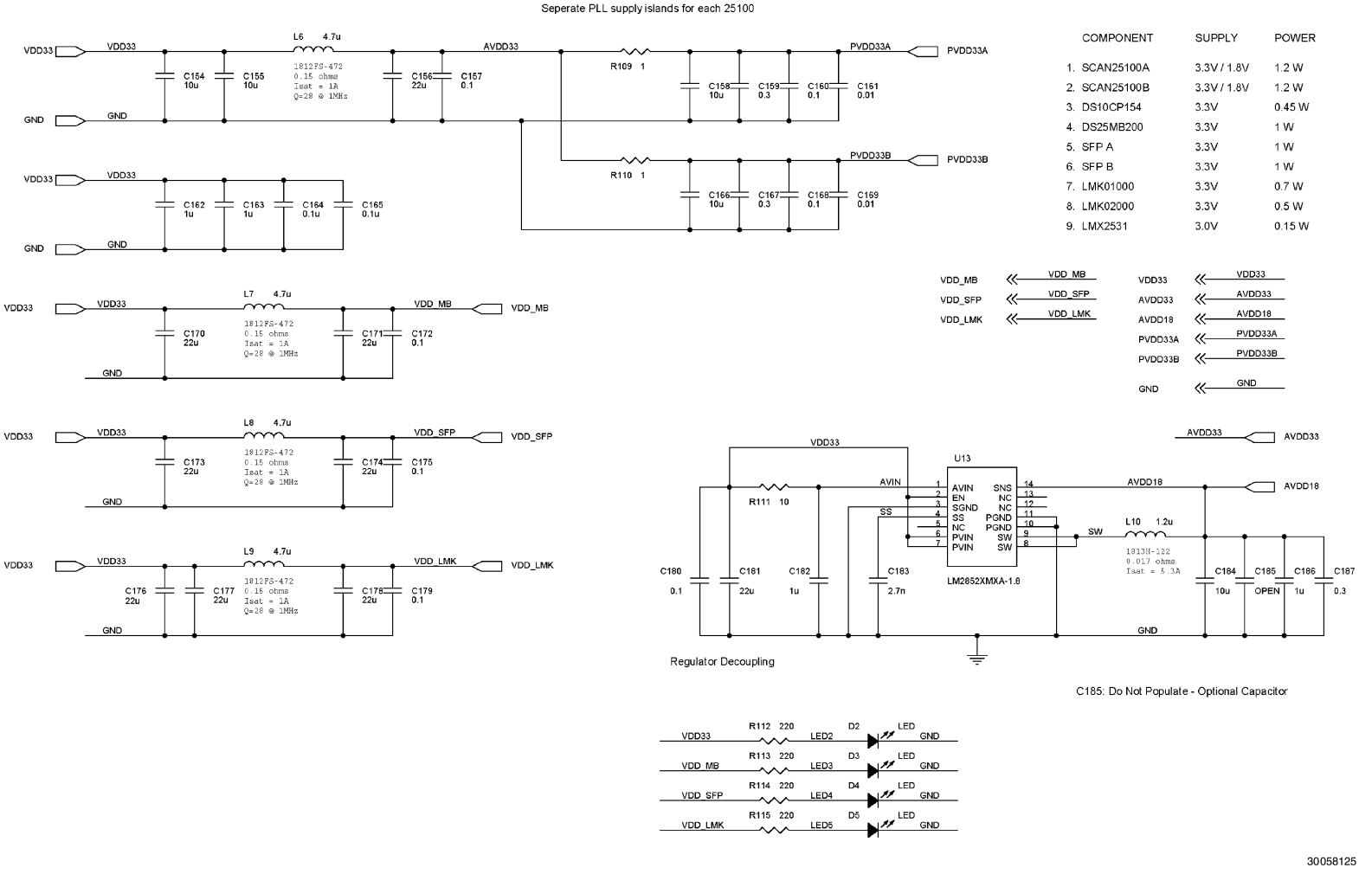

FIGURE 24. RE Schematic Page 6

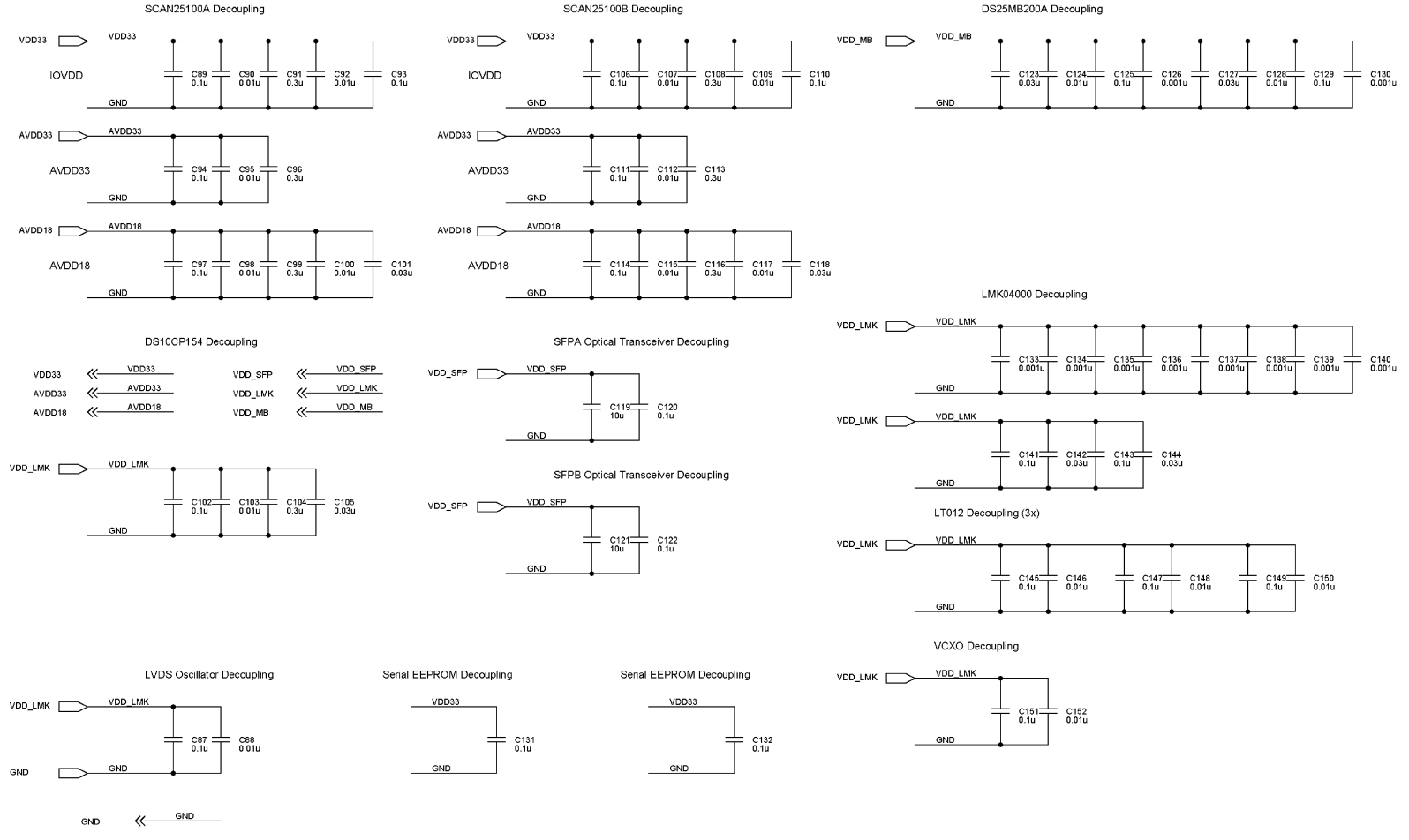

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FIGURE 25. RE Schematic Page 7

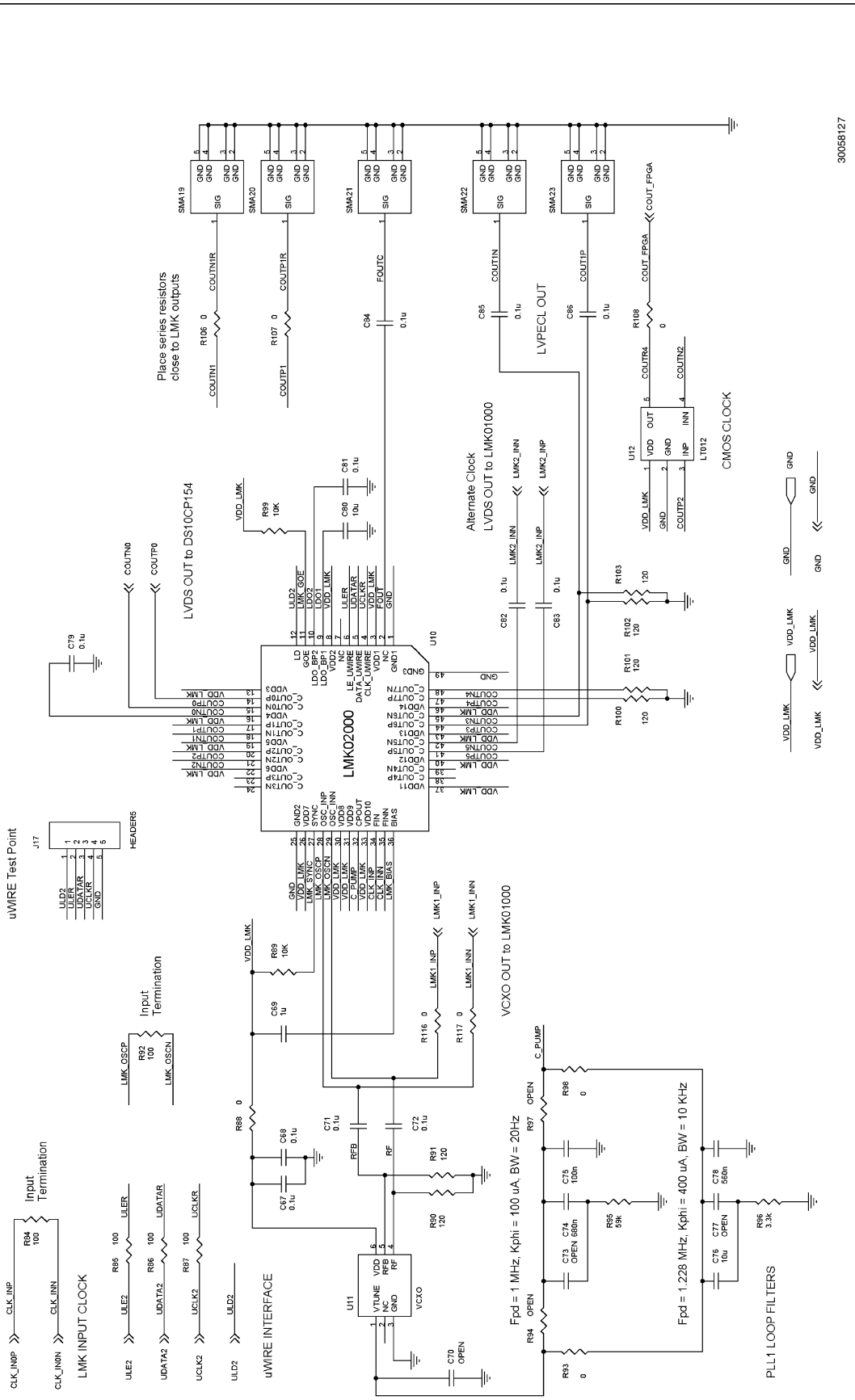

FIGURE 26. RE Schematic Page 8

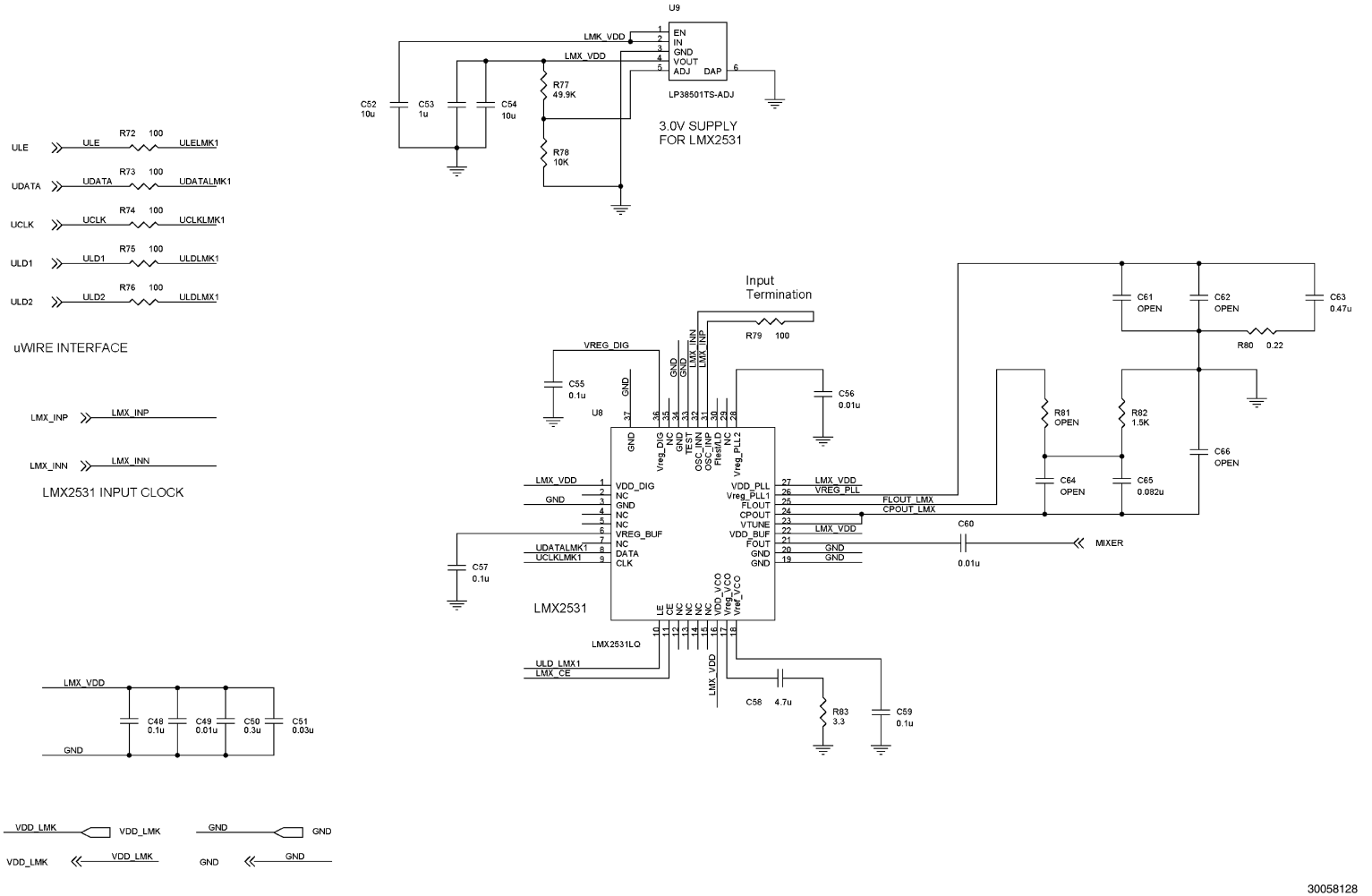

FIGURE 27. RE Schematic Page 9

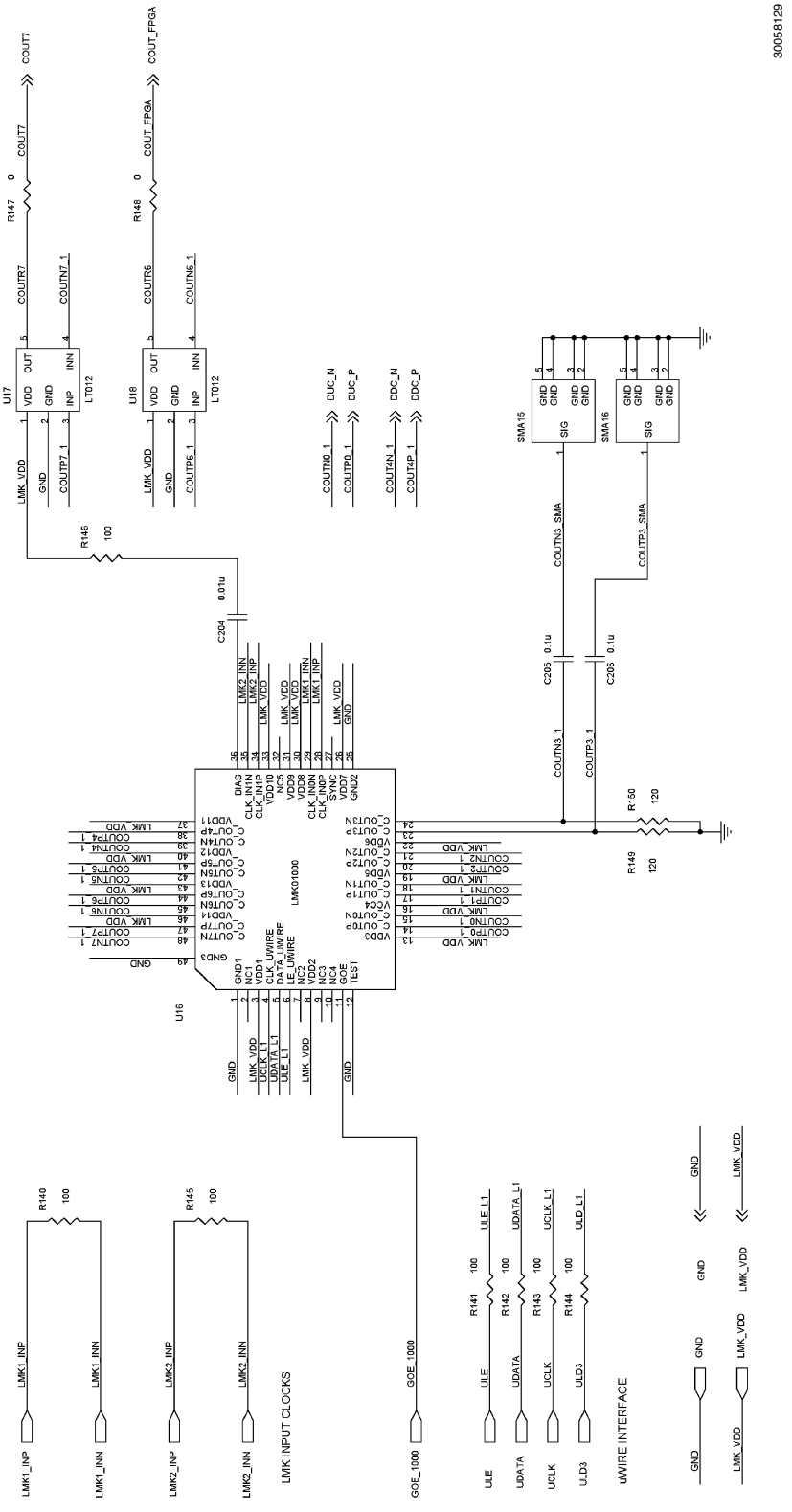

FIGURE 28. RE Schematic Page 10

5.4 RE BILL OF MATERIALS

TABLE 9. RE BOM

Item	Quantity	Reference	Part
1	36	C1, C2, R16, R17, R18, R19, R28, R29, R30, R31, R32, R33, R34, R47, R48, R49, R50, R51, R52, R53, R54, R55, R56, R57, C61, C62, C64, C66, R69, C70, C73, C77, R81, R94, R97, C185	OPEN
2	84	C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C28, C29, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C55, C57, C59, C67, C68, C71, C72, C79, C81, C82, C83, C84, C85, C86, C87, C89, C93, C94, C97, C102, C106, C110, C111, C114, C120, C122, C125, C129, C131, C132, C141, C143, C145, C147, C149, C151, C164, C165, C205, C206	0.1 u
3	13	C27, C30, C52, C54, C76, C80, C119, C121, C154, C155, C158, C166, C184	10 u
4	22	C49, C56, C60, C88, C90, C92, C95, C98, C100, C103, C107, C109, C112, C115, C117, C124, C128, C146, C148, C150, C152, C204	0.01 u
5	8	C50, C91, C96, C99, C104, C108, C113, C116	0.3 u
6	8	C51, C101, C105, C118, C123, C127, C142, C144	0.03 u
7	6	C53, C69, C162, C163, C182, C186	1 u
8	5	L6, L7, L8, L9, C58	4.7 u
9	1	C63	0.47 u
10	1	C65	0.082 u
11	1	C74	680 n
12	1	C75	100 n
13	1	C78	560 n
14	10	C126, C130, C133, C134, C135, C136, C137, C138, C139, C140	0.001 u
15	9	C156, C170, C171, C173, C174, C176, C177, C178, C181	22 u
16	7	C157, C160, C168, C172, C175, C179, C180	0.1
17	3	C159, C167, C187	0.3

Item	Quantity	Reference	Part
18	2	C161, C169	0.01
19	1	C183	2.7 n
20	4	D2, D3, D4, D5, LED	
21	8	J1, J3, J9, J11, J13, J14, J15, J16	HEADER2
22	7	J2, J4, J6, J7, J8, J10, J12	HEADER 10X2 / SM
23	1	J5	HEADER 5X2
24	1	J17	HEADER 5
25	4	L1, L2, L3, L4	1 uH
26	1	L10	1.2 uH
27	24	R1, R2, R20, R21, R22, R23, R24, R25, R26, R27, R59, R60, R61, R62, R63, R64, R65, R66, R68, R70, R71, R78, R89, R99	10 K
28	24	R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R15, R36, R37, R38, R39, R40, R41, R42, R43, R44, R45, R46	22
29	20	R35, R58, R72, R73, R74, R75, R76, R79, R84, R85, R86, R87, R92, R140, R141, R142, R143, R144, R145, R146	100
30	1	R77	49.9 K
31	1	R80	0.22
32	1	R82	1.5 K
33	1	R83	3.3
34	10	R88, R93, R98, R106, R107, R108, R116, R117, R147, R148	0
35	8	R90, R91, R100, R101, R102, R103, R149, R150	120
36	1	R95	59 k
37	1	R96	3.3 k
38	2	R109, R110	1
39	1	R111	10
40	4	R112, R113, R114, R115	220
41	17	SMA1, SMA2, SMA3, SMA4, SMA5, SMA6, SMA7, SMA8, SMA13, SMA14, SMA15, SMA16, SMA19, SMA20, SMA21, SMA22, SMA23	SMAedge
42	2	SW1, SW3	SW DIP-2/SM
43	4	SW2, SW4, SW5, SW6	SW DIP-5/SM
44	2	U1, U2	SCAN25100
45	1	U3	DS25MB200
46	2	U4, U5	SFP
47	1	U6	DS10CP154
48	1	U7	OSC-LVDS
49	1	U8	LMX2531LQ
50	1	U9	LP38501TS-ADJ
51	1	U10	LMK02000
52	1	U11	VCXO

Item	Quantity	Reference	Part
53	3	U12, U17, U18	LT012
54	1	U13	LM2852XMXA-1.8
55	1	U16	LMK01000

Notes

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