Lenco Lucille LCD initialisation sequence

v1.3 06 Feb 2021

LCD 10 pin interface : RST, RS, CS, SCL, SDA, GND, VDD, CAP, CAP, VLCD

RST	Reset, hardware reset.
RS	Register select, select data or command register.
CS	Chip select, active low, transitions on the falling edge of SCL. Held low for
	duration of a byte, or continuously for the duration of a byte sequence.
SCL	Clock, 17uS (21uS between clock pulses), only present during CS period.
SDA	Data, write clocked on rising edge of SCL.
	Sent most-significant-bit first, 8 bit words, 135uS delay between bytes.
GND	0V
VDD	+3.3V, LCD logic power supply.
CAP, VLCD	LCD power, generated higher supply voltage

From the instruction codes sent, it appears to have a Sitronix ST7032 compatible controller.

LCD initialisation:

 39
 1c
 5d
 7c
 6a
 38
 0c
 06
 01
 01

 40
 00
 11
 0e
 0a
 0e
 11
 00
 04
 0e
 11
 11
 11
 11
 16
 00
 00
 50
 0e
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 11
 <t

Initial code, each byte written with a single pulse to the CS line, 1.5mS between writes

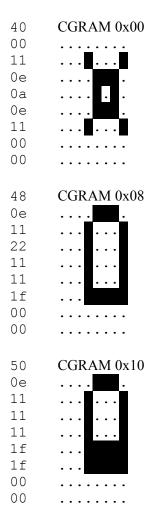
39	Function set -	
	Turn ON extended instruction set,	
	8 bit,	
	2 lines,	
	5x8 font	
1c	Extended instruction - Internal OSC frequency	
	183Hz frame rate,	
	1/4 Bias	
5d	Extended instruction - Power/ICON control/Contrast set	
	ICON display ON,	
	Booster circuit ON,	
	Contrast set (high nibble) = 01	
7c	Extended instruction -	
	Contrast set(low nibble) = $C0$	
6a	Extended instruction - Follower control	
	Turn ON internal follower circuit	
	1.5 follower ratio	
(should be 200mS delay for power to stabilise)		

- 38 Function set -Turn OFF extended instruction set, 8 bit, 2 lines, 5x8 font
 0a Display on surger off blink off
- 0c Display on, cursor off, blink off
- 06 Entry mode increment, shift
- 01 Clear display, set cursor address 0

3mS delay then writes a single byte

01 Clear display, set cursor address 0

Second initialisation sequence after 3mS, 136uS between bytes The following bytes are each written during a CS pulse duration Write to character generator (characters 0, through 7 are written)



58 0e 11 1f 1f 1f 00 00	CGRAM 0x18
60 0e 11 1f 1f 1f 00 00	CGRAM 0x20
68 00 1f 11 11 11 11 11 11 00	CGRAM 0x28
70 00 1f 1f 1f 1f 1f 1f 1f 00	CGRAM 0x30
78 00 04 0e 1f 1f 04 00	CGRAM 0x38

Display startup message

80	DRAM 00 - Position cursor line 1, character 1
"	Welcome to "
20	
20	
20	
57	
65	
6c	
63	
6f	
6d	
65	
20	
74	
6f	
20	
20	
20	

с0 ″	DRAM 40 - Position cursor line 2, character 1 Radio "
20	Radio
20	
20	
20	
20	
52	
61	
64	
69	
6f	
20	
20	
20	
20	
20	

20