Lenco Lucille LCD initialisation sequence

v1.1 28 Oct 2018

LCD 10 pin interface : RST, RS, CS, SCL, SDA, GND, VDD, CAP, CAP, VLCD

RST	Reset, hardware reset.
RS	Register select, select data or command register.
CS	Chip select, active low, transitions on the falling edge of SCL. Held low for duration of a byte, or continuously for the duration of a byte sequence.
SCL	Clock, 17uS (21uS between clock pulses), only present during CS period.
SDA	Data, write clocked on rising edge of SCL. Sent most-significant-bit first, 8 bit words, 135uS delay between bytes.
GND	0V
VDD	+3.3V, LCD logic power supply.
CAP, VLCD	LCD power, generated higher supply voltage

From the instruction codes sent, it appears to have a Sitronix ST7032 compatible controller.

LCD initialisation:

```
39 1C 5D 7C 6A 38 0C 06 01 01
40 00 11 0E 0A 0E 11 00 00 48 0E 11 11 11 11 1F 00 00 50 0E 11 11 11 1F 1F
00 00 58 0E 11 11 1F 1F 1F 00 00 60 0E 11 1F 1F 1F 1F 00 00 68 00 1F 11 11
11 11 1F 00 70 00 1F 1F 1F 1F 1F 1F 00 78 00 04 0E 0E 1F 1F 04 00 80
20 20 20 57 65 6C 63 6F 6D 65 20 74 6F 20 20 20 C0 20 20 20 20 20 52 61 64
69 6F 20 20 20 20 20 20
```

Initial code, each byte written with a single pulse to the CS line, 1.5mS between writes

`39` Function set -
- Turn ON extended instruction set,
- 8 bit,
- 2 lines,
- 5x8 font

`1C` Extended instruction - Internal OSC frequency
- 183Hz frame rate,
- 1/4 Bias

`5D` Extended instruction - Power/ICON control/Contrast set
- ICON display ON,
- Booster circuit ON,
- Contrast set (high nibble) = 01

`7C` Extended instruction -
- Contrast set(low nibble) = C0

`6A` Extended instruction - Follower control
- Turn ON internal follower circuit
- 1.5 follower ratio

(should be 200mS delay for power to stabilise)

38 Function set -
Turn OFF extended instruction set,
8 bit,
2 lines,
5x8 font
0C Display on, cursor off, blink off

06 Entry mode increment, shift

01 Clear display, set cursor address 0

3mS delay then writes a single byte

01 Clear display, set cursor address 0

Second initialisation sequence after 3mS, 136uS between bytes
The following bytes are each written during a CS pulse duration
Write to character generator (characters 0, through 7 are written)

40 CGRAM 0x00

```
........
...#...#
....###.
....#.#.
....###.
...#...#
........
........
```

48 CGRAM 0x08

```
....###.
...#...#
...#...#
...#...#
...#...#
...#####
........
........
```

50 CGRAM 0x10

```
....###.
...#...#
...#...#
...#...#
...#####
...#####
........
........
```

58 CGRAM 0x18

```
....###.
...#...#
...#...#
...#####
...#####
...#####
........
........
```

68 CGRAM 0x28

```
........
...#####
...#...#
...#...#
...#...#
...#...#
...#####
........
```

70 CGRAM 0x30

```
........
...#####
...#####
...#####
...#####
...#####
...#####
........
```

78 CGRAM 0x38

```
........
.....#..
....###.
....###.
...#####
...#####
.....#..
........
```

Display startup message

80 DRAM 00 - Position cursor line 1, character 1

```
20 20 20 57 65 6C 63 6F 6D 65 20 74 6F 20 20 20
```

"   **Welcome to**   "

C0 DRAM 40 - Position cursor line 2, character 1

```
20 20 20 20 20 52 61 64 69 6F 20 20 20 20 20 20
```

"   **Radio**   "