

Epson WF-2530 LCD initialisation sequence

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This printer was manufactured about 2012.

LCD controller similar to ST7567, but some extra instruction codes that are not in preliminary datasheet.

LCD 8 pin interface : CSB, RSTB, A0, SCLK, SDA, VDD, GND, VG

CSB	Chip select. active low, going low before the clock becomes active, and staying low for the whole period while a sequence of bytes is sent.
RSTB	Reset, hardware reset LCD, pulsed low for 85uS once after power on..
A0	Register select, asserted low to write commands, high to write data.
SCLK	Clock, 3MHz during CSB period for LCD controller.
SDA	Data, write bits clocked on rising edge of SCLK. Sent most-significant-bit first, 8 bit words, 420nS delay between bytes (clock stretched).
VDD	3.3V, logic power supply.
GND	0V
VG	LCD generated power.

From the instruction codes sent, it appears to have a Sitronix controller, like ST7567, but some extra commands. A lot of sequences are padded with no-operation (NOP) commands (code 'E3'), maybe this is because the printer uses a 32bit processor and writes out 4 bytes at a time, so pads commands to 32bits with bytes of NOP.

The control lines are also used on other parts of the front panel for controlling the front panel LEDs and scanning for keypresses.

LCD initialisation:

RS low for the whole sequence, CS low during each 4 byte word, then high for 3.25uS between words.

A2 A1 C0 22 E3 81 1F E5 E3 89 02 82 32 3A D3 00 E3 E3 84 2F

A2 Bias Select

A1 Horizontal display direction - reverse

C0 Vertical display direction - normal

22 Regulation Ratio – 4.0

E3 NOP

811F Set EV, adjusts V0 – 0x1F

E5

E3 NOP

89

02 Set Column Address - 02

82

```

32  Set Page Address - 02
3A  Set Page Address - 0A
D3
00  Set Column Address of RAM low byte - 0

E3  NOP
E3  NOP
84
2F  Control power - Booster ON, Regulator ON, Follower ON

```

Delay of 100uS

Sends 4 'pages' of 128 bytes, but display not turned on (unlike later 4 lines that are displayed), so I don't know what this material is.

```

E3 E3 40 00 B0 10 00 E3
E3  NOP
E3  NOP
40  Set display start line - 0
00  Set Column Address of RAM low byte - 0

B0  Set Page Address - 0
10  Set Column Address of RAM hi nibble - 0
00  Set Column Address of RAM low nibble - 0
E3  NOP

```

Delay of 1uS then CS low and RS high for the next 128 bytes of data.

```

00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 02 08 20 09 24 0D 00
00 00 05 D0 00 06 88 0C 02 54 46 03 78 01 01 04
02 01 00 00 04 C8 21 02 64 01 00 7C 06 00 00 00
01 9C D2 02 04 51 01 00 00 01 30 13 01 00 00 01
40 0D 0A 28 0D 02 24 00 01 28 0D 05 3C 5E 04 28
0D 00 00 00 00 6C 00 03 28 0D 00 00 00 09 90 00
00 00 00 0D 90 00 00 00 00 01 18 1A 03 38 41 03

```

CS high, RS low

Delay of 1uS, then 4 byte word with CS low

```

B1 10 00 E3
B1  Set Page Address - 1
10  Set Column Address of RAM hi nibble - 0
00  Set Column Address of RAM low nibble - 0
E3  NOP

```

Delay of 1uS then CS low and RS high for the next 128 bytes of data.

```
74 20 10 28 0D 00 00 00 0D A0 00 02 B8 09 00 FC
07 04 74 07 00 00 00 01 30 8A 02 98 05 00 00 00
02 98 4C 0D 28 0D 00 00 00 05 04 0D 00 00 00 01
24 00 00 00 00 01 20 03 06 28 0D 00 00 00 05 2C
03 02 28 0D 00 00 00 05 24 00 00 00 00 05 48 00
00 00 00 05 48 00 0A 4C 4B 02 88 1B 0A 6C 0B 00
00 00 01 9C 46 1A 28 0D 00 00 00 05 3C 47 00 00
00 01 1C 1D 00 00 00 05 84 0C 0A 28 0D 00 00 00
```

CS high, RS low

Delay of 1uS, then 4 byte word with CS low

B2 10 00 E3

B2 Set Page Address - 2

10 Set Column Address of RAM hi nibble - 0

00 Set Column Address of RAM low nibble - 0

E3 NOP

Delay of 1uS then CS low and RS high for the next 128 bytes of data.

```
09 CC 4D 00 00 00 01 24 06 00 00 00 01 30 0D 00
00 00 01 50 59 00 00 00 09 74 38 00 00 00 01 0C
03 16 C4 8A 00 00 00 01 10 01 07 5C 3E 00 00 00
01 58 7C 02 5D CB 01 84 09 01 00 00 01 30 04 00
00 00 00 04 00 00 C8 06 00 04 06 02 B8 00 01 00
00 05 7C 1C 05 E8 B2 03 74 4B 05 28 E4 02 4C 04
00 00 00 00 08 01 04 8C C7 01 54 01 01 B8 2C 04
6C B0 09 A0 23 02 1C 00 01 B0 15 01 00 00 03 34
```

CS high, RS low

Delay of 1uS, then 4 byte word with CS low

B3 10 00 E3

B3 Set Page Address - 3

10 Set Column Address of RAM hi nibble - 0

00 Set Column Address of RAM low nibble - 0

E3 NOP

Delay of 1uS, then CS low and RS high for the next 128 bytes of data

```
00 01 7C 02 00 78 06 02 50 49 07 1C 00 02 04 50
06 7C 88 02 E0 39 02 28 27 02 3C 51 02 60 E6 02
C4 01 02 64 33 06 D8 52 02 14 04 00 00 00 01 30
00 00 00 00 01 14 63 0A 24 18 01 00 00 04 58 09
```

00 00 00 05 48 50 02 4C 00 00 00 00 01 1C 35 00
00 00 01 A4 31 00 00 00 05 0C 03 00 00 00 02 D0
8B 02 A0 D7 01 34 00 02 AC 01 00 00 00 01 04 8C
00 00 00 02 D0 33 03 CC 05 00 4C 00 02 FC B8 04

CS high, RS low

Delay of 500uS, then CS low, RS low, and 4 commands

81 22 E3 E3

8122 Set EV, adjusts V0 – 0x22

E3 NOP

E3 NOP

CS high, RS low

Delay 40mS, then CS low, RS low the 7 words of 4 bytes

E3 NOP

F0 Test

D5

A2 Bias Select

A1 Set scan direction of SEG - reverse

C0 Vertical display direction - normal

22 Regulation Ratio – 4.0

E3 NOP

81 22 E3 E3

8122 Set EV, adjusts V0 – 0x22

E3 NOP

E3 NOP

E3 A6 A4 EE

E3 NOP

A6 Set LCD normal/reverse - normal

A4 Display all points ON/OFF - OFF

EE Reset Modify-Read mode

AC 00 E5 89

AC00 Set Static Indicator State - OFF

E5

89

02 82 32 3A

02 Set lower nibble of RAM column address - 0x02

82

32

3A

D3 00 84 2F

D3

00 Set lower nibble of RAM column address - 0x00

84

2F Control power - Booster ON, Regulator ON, Follower ON

Delay 150mS, then CS low, RS low

40 E3 E3 E3

40 Set display start line - 0

E3 NOP

E3 NOP

E3 NOP

CS high, RS low

Delay 95uS, CS low, RS low

Display "The date and time " on line 1, takes two pages of 128 bytes.

B0 10 00 E3

B0 Set Page Address - 0

10 Set Column Address of RAM hi nibble - 0

00 Set Column Address of RAM low nibble - 0

E3 NOP

CS high, RS low

Delay 95uS, then CS low RS high

```

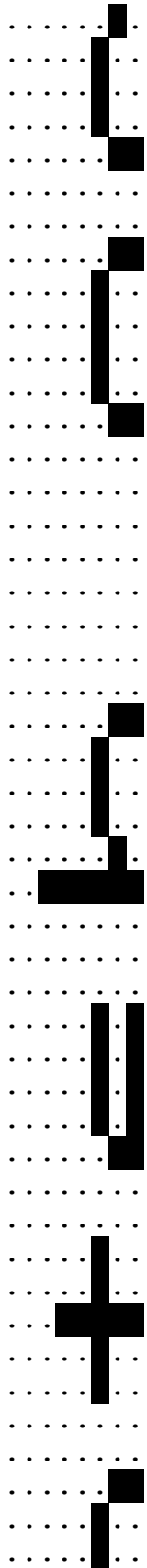
04 04 FC 04 04 00 00 FC 40 20 20 20 C0 00 00 C0
20 20 20 20 C0 00 00 00 00 00 00 00 00 C0 20 20
20 40 FC 00 00 00 A0 A0 A0 A0 C0 00 00 20 20 F8
20 20 00 00 C0 20 20 20 20 C0 00 00 00 00 00 00
00 00 00 A0 A0 A0 A0 C0 00 00 E0 40 20 20 20 C0
00 00 C0 20 20 20 40 FC 00 00 00 00 00 00 00
20 20 F8 20 20 00 00 EC 00 00 E0 20 C0 20 20 C0
00 00 C0 20 20 20 20 C0 00 00 00 00 00 00 00

```

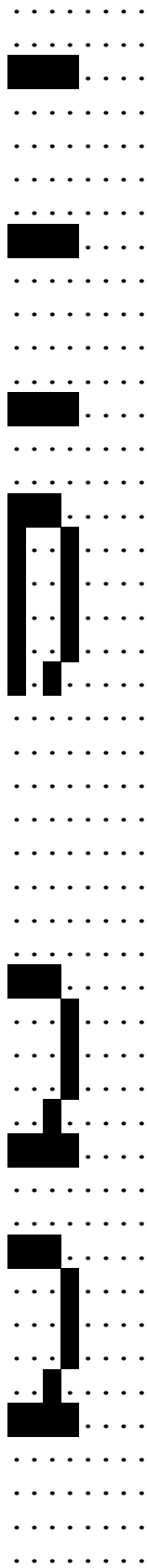
```

.. ██████████ 04
.. ██████████ 04
.. ██████████ FC
.. ██████████ 04
.. ██████████ 04
.. ██████████ 00
.. ██████████ 00
.. ██████████ FC

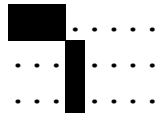
```



40
20
20
20
C0
00
00
C0
20
20
20
20
C0
00
00
00
00
00
00
00
00
00
C0
20
20
20
40
FC
00
00
00
A0
A0
A0
A0
C0
00
00
20
20
F8
20
20
00
00
C0
20
20



00
00
0F
00
00
00
00
0F
00
00
00
00
0F
00
00
07
09
09
09
09
05
00
00
00
00
00
00
00
00
00
07
08
08
08
04
0F
00
00
07
08
08
08
04
0F
00
00
00
00



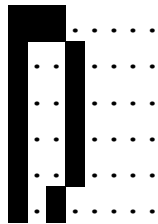
07

08

08

00

00



07

09

09

09

09

05

00

00

00

00

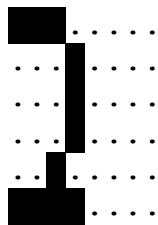
00

00

00

00

07



08

08

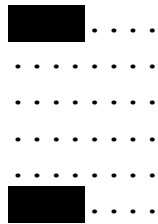
08

04

0F

00

00



0F

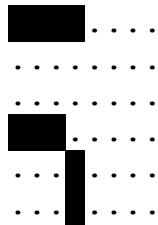
00

00

00

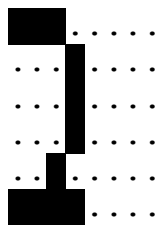
00

0F



00

07



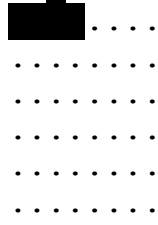
08

08

08

04

0F



00

00

00

00

00

00

.....	00
.....	00
.....	00
.....	00
█.....	07
█.....	08
█.....	08
.....	00
.....	00
█.....	0F
.....	00
.....	00
█.....	0F
.....	00
█.....	0F
.....	00
.....	00
█.....	0F
.....	00
.....	00
█.....	07
█.....	09
█.....	09
█.....	09
█.....	09
█.....	05
.....	00
.....	00
.....	00
.....	00
.....	00
.....	00
.....	00
.....	00
.....	00

AF E3 E3 E3
 AF Display ON/OFF - ON
 E3 NOP
 E3 NOP
 E3 NOP

omit some of the art

Display "1:Yes 2:No " on line 2, takes two pages of 128 bytes.

B2 10 00 E3

B2 Set Page Address - 2
10 Set Column Address of RAM hi nibble - 0
00 Set Column Address of RAM low nibble - 0
E3 NOP

```
00 04 04 FE 00 00 00 00 30 30 00 00 00 0E 30 C0
20 18 06 00 00 E0 90 90 90 90 E0 00 00 60 90 90
90 90 20 00 00 00 00 00 00 00 00 00 0C 82 42 22
1C 00 00 30 30 00 00 00 FE 08 30 C0 00 FE 00 00
E0 10 10 10 10 E0 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
```

.....	00
..	04
..	04
..	FE
.....	00
.....	00
.....	00
.....	00
.....	30
.....	30
.....	00
.....	00
.....	00
.....	0E
.....	30
.....	C0
.....	20
.....	18
.....	06
.....	00
.....	00
.....	E0
.....	90
.....	90
.....	90
.....	90
.....	E0
.....	00
.....	00
.....	60
.....	90
.....	90
.....	90

..... 00

AF E3 E3 E3

AF Display ON/OFF - ON

E3 NOP

E3 NOP

E3 NOP

B3 10 00 E3

B3 Set Page Address - 3

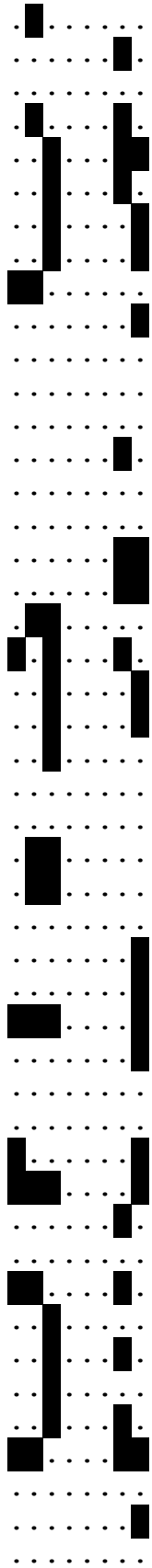
10 Set Column Address of RAM hi nibble - 0

00 Set Column Address of RAM low nibble - 0

E3 NOP

40	00	00	07	40	00	40	40	06	06	00	00	00	00	40	07
40	00	40	00	00	03	04	04	44	44	02	40	00	42	C4	44
84	84	03	80	00	00	00	40	00	00	C0	C0	06	45	84	84
04	00	00	06	06	00	80	80	87	80	00	00	81	87	40	00
43	04	44	04	44	C3	00	80	00	00	00	00	00	00	00	40
00	80	00	00	80	80	00	00	00	00	00	00	00	00	00	00
00	00	00	00	00	00	80	00	80	80	80	80	80	80	00	40
80	00	80	80	80	40	00	00	40	00	00	40	C0	00	00	00

.....█.	40
.....	00
.....	00
█.....	07
.....█.	40
.....	00
.....█.	40
.....	40
█.....	06
.....	06
.....	00
.....	00
.....	00
.....	00
.....	00
.....█.	40
█.....	07
.....█.	40
.....	00
.....█.	40
.....	00
.....	00
█.....	03
.....	04
.....	04
.....	44
█.....█.	44



02
40
00
42
C4
44
84
84
03
80
00
00
00
40
00
00
C0
C0
06
45
84
84
04
00
00
06
06
00
80
80
87
80
00
00
81
87
40
00
43
04
44
04
44
C3
00
80
00

.....█.	40
.....	00
.....	00
.....	00
.....	40
.....█	C0
.....	00
.....	00

AF E3 E3 E3

AF Display ON/OFF - ON

E3 NOP

E3 NOP

E3 NOP

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
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86
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90
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92
93
94
95
96
97
98
99
100

Sequence:

After a sequence of setup commands, 4 'pages' of 128 bytes, are sent but the display is not turned on and nothing is apparent visually. On character based LCD displays I might expect a sequence like this to be defining programmable character dot matrices, but I don't know the purpose here.

Lastly two lines of text are sent and displayed :

line1 - **"The date and time settings have been reset, or are incorrect. Do you want to set them again?"**

line2 - **"1:Yes 2:No"**

Line 1 starts to scroll left after about 2 second pause. Scrolls completely off the left of display then repeats. About 9 or 10 seconds for a character to scroll from one end to the other.

The characters are 14 pixels high, on the second line of data displayed there appears to be extra data in the lower 2 'unused' bits of each displayed byte.